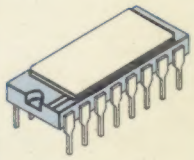
SAMSUNG

Data Book

MOS Memory

1989



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SAMSUNG
DATA BOOK LIST

I. Semiconductor Product Guide

II. Transistor Data Book

Vol. 1: Small Signal TR

Vol. 2: Bipolar Power TR

Vol. 3: TR Pellet

III. Linear IC Data Book

Vol. 1: Audio/Video

Vol. 2: Telecom/Industrial

Vol. 3: Data Converter IC

IV. MOS Product Data Book

V. High Performance CMOS Logic Data Book

VI. MOS Memory Data Book

VII. SFET Data Book

VIII. MPR Data Book

IX. CPL Data Book

X. Dot Matrix Data Book

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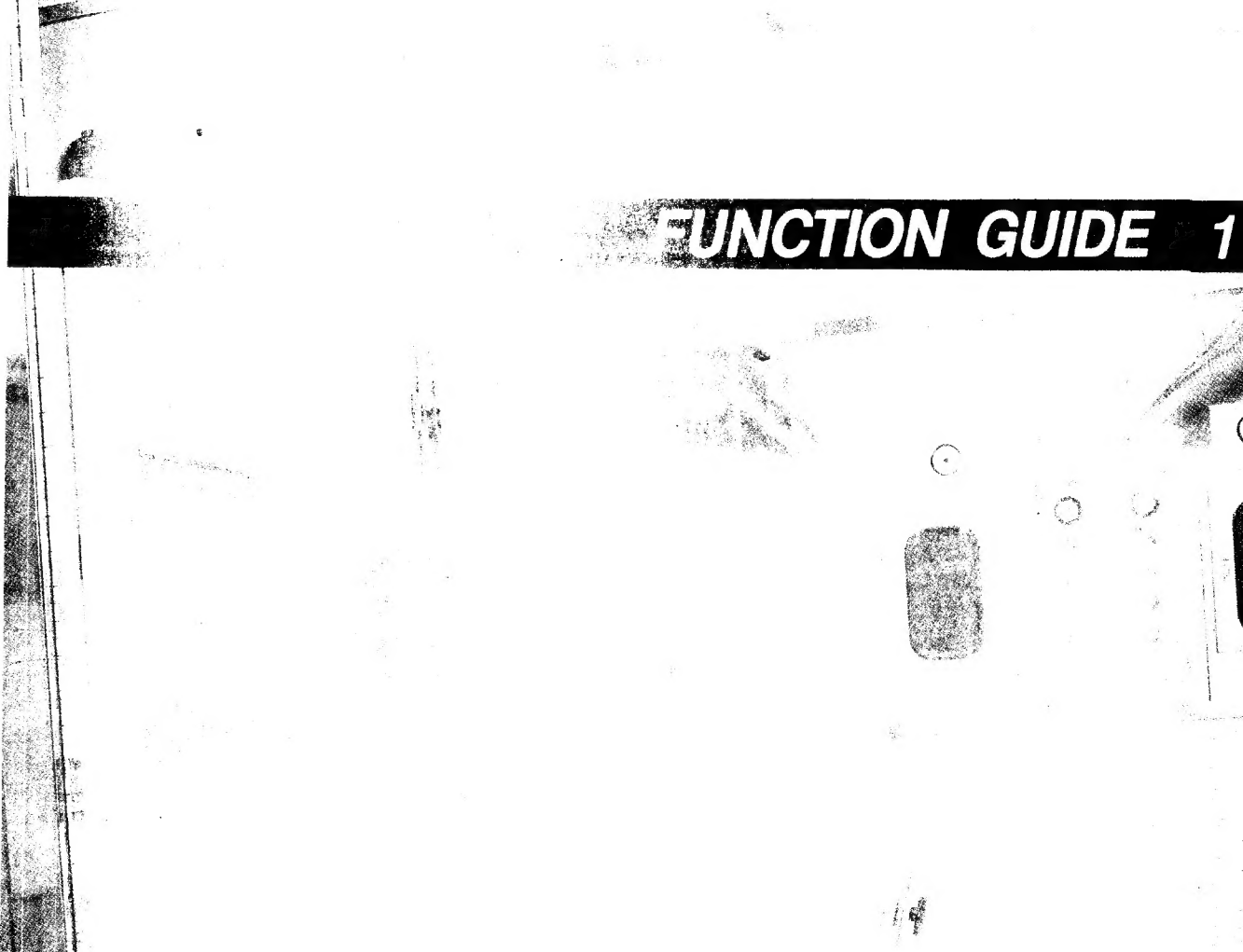
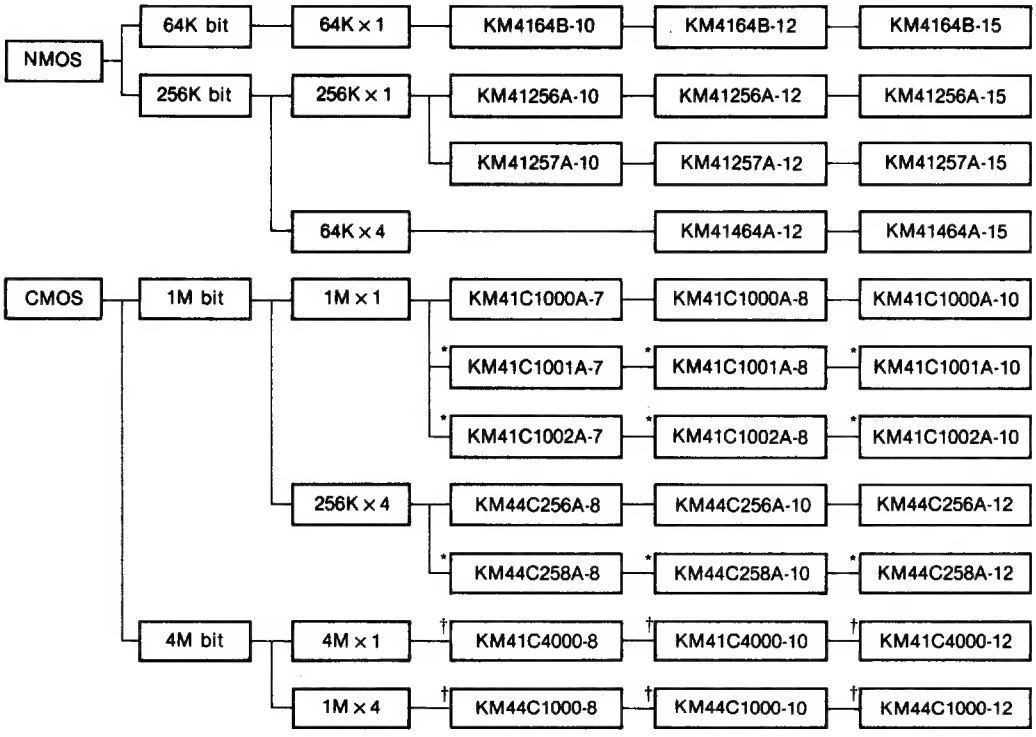
FUNCTION GUIDE 1



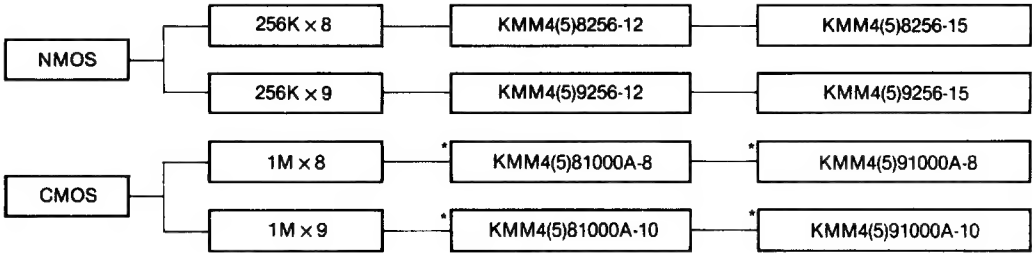
1. Introduction
2. Product Guide
3. Ordering Information

1. INTRODUCTION

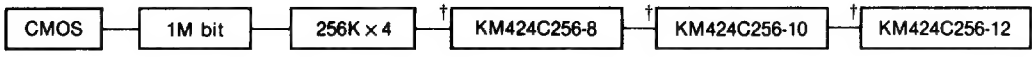
1.1 Dynamic RAM



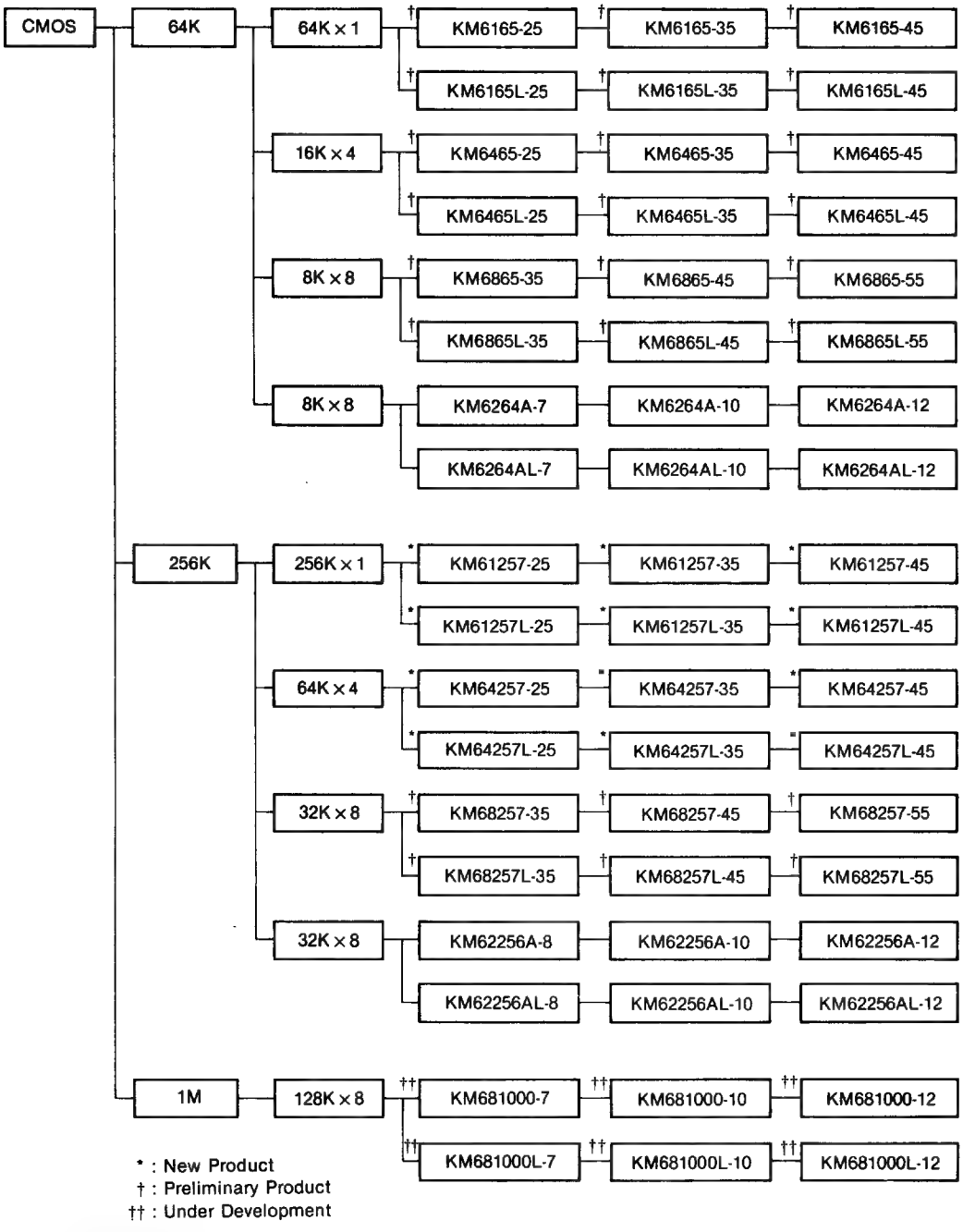
1.2 Memory Module



1.3 Video RAM

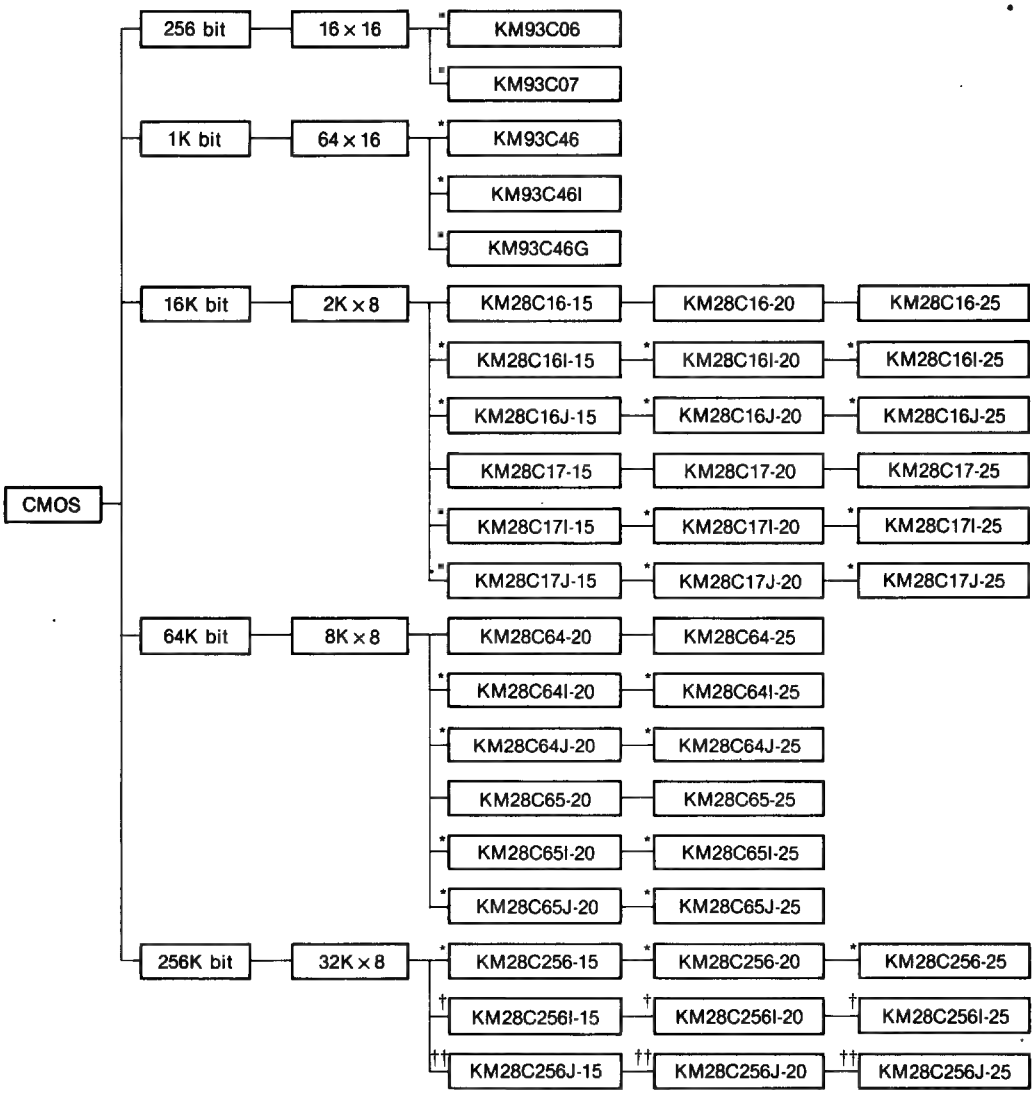


1.4 Static RAM



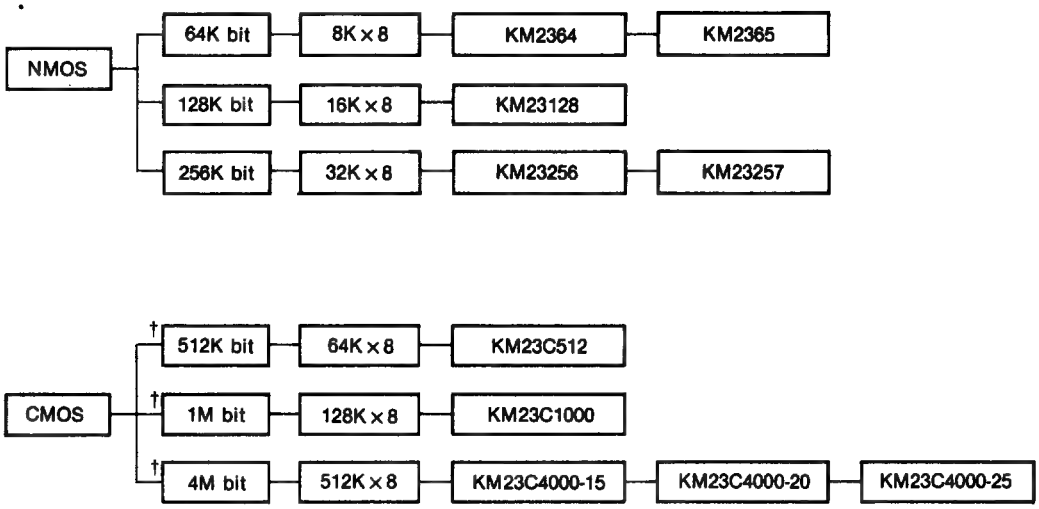
* : New Product
† : Preliminary Product
†† : Under Development

1.5 EEPROM



* : New Product
† : Preliminary Product
†† : Under Development

1.6 MASK ROM



† Preliminary Product: All Product is Volume available within 1989.

2. PRODUCT GUIDE

2.1 Dynamic RAM

Capacity	Part Number	Organization	Speed (ns)	Technology	Features	Packages	Remark
64K bit	KM4164BP	64K × 1	100/120/150	NMOS	Page Mode	16-Pin DIP	Now
256K bit	KM41256AP	256K × 1	100/120/150	NMOS	Page Mode	16-Pin DIP	Now
	KM41256AJ	256K × 1	100/120/150	NMOS	Page Mode	18-Pin PLCC	Now
	KM41256AZ	256K × 1	100/120/150	NMOS	Page Mode	16-Pin ZIP	Now
	KM41257AP	256K × 1	100/120/150	NMOS	Nibble Mode	16-Pin DIP	Now
	KM41257AJ	256K × 1	100/120/150	NMOS	Nibble Mode	18-Pin PLCC	Now
	KM41257AZ	256K × 1	100/120/150	NMOS	Nibble Mode	16-Pin ZIP	Now
	KM41464AP	64K × 4	120/150	NMOS	Page Mode	18-Pin DIP	Now
	KM41464AJ	64K × 4	120/150	NMOS	Page Mode	18-Pin PLCC	Now
	KM41464AZ	64K × 4	120/150	NMOS	Page Mode	20-Pin ZIP	Now
1M bit	KM41C1000AP	1M × 1	70/80/100	CMOS	Fast Page Mode	18-Pin DIP	Now
	KM41C1000AJ	1M × 1	70/80/100	CMOS	Fast Page Mode	20-Pin SOJ	Now
	KM41C1000AZ	1M × 1	70/80/100	CMOS	Fast Page Mode	20-Pin ZIP	Now
	*KM41C1001AP	1M × 1	70/80/100	CMOS	Nibble Mode	18-Pin DIP	Now
	*KM41C1001AJ	1M × 1	70/80/100	CMOS	Nibble Mode	20-Pin SOJ	Now
	*KM41C1001AZ	1M × 1	70/80/100	CMOS	Nibble Mode	20-Pin ZIP	Now
	*KM41C1002AP	1M × 1	70/80/100	CMOS	Static Col. Mode	18-Pin DIP	Now
	*KM41C1002AJ	1M × 1	70/80/100	CMOS	Static Col. Mode	20-Pin SOJ	Now
	*KM41C1002AZ	1M × 1	70/80/100	CMOS	Static Col. Mode	20-Pin ZIP	Now
	KM44C256AP	256K × 4	80/100/120	CMOS	Fast Page Mode	20-Pin DIP	Now
	KM44C256AJ	256K × 4	80/100/120	CMOS	Fast Page Mode	20-Pin SOJ	Now
	KM44C256AZ	256K × 4	80/100/120	CMOS	Fast Page Mode	20-Pin ZIP	Now
	*KM44C258AP	256K × 4	80/100/120	CMOS	Static Col. Mode	20-Pin DIP	Now
	*KM44C258AJ	256K × 4	80/100/120	CMOS	Static Col. Mode	20-Pin SOJ	Now
	*KM44C258AZ	256K × 4	80/100/120	CMOS	Static Col. Mode	20-Pin ZIP	Now
4M bit	†KM41C4000J	4M × 1	80/100/120	CMOS	Fast Page Mode	20-Pin SOJ	TBA
	†KM44C1000J	1M × 4	80/100/120	CMOS	Fast Page Mode	20-Pin SOJ	TBA
Video RAM	†KM424C256P	256K × 4	RAM; 80/100/120 SAM; 20/25/35	CMOS	Fast Page Mode Serial In/Out	28-Pin DIP	TBA
	†KM424C256J	256K × 4	RAM; 80/100/120 SAM; 20/25/35	CMOS	Fast Page Mode Serial In/Out	28-Pin SOJ	TBA
	†KM424C256Z	256K × 4	RAM; 80/100/120 SAM; 20/25/35	CMOS	Fast Page Mode Serial In/Out	28-Pin ZIP	TBA

*: New Product
†: Preliminary Product

2.2 Memory Module

Part Number	Organization	Speed (ns)	Technology	Feature	Package	Remark
KMM48256	256K × 8	120/150	NMOS	Page Mode	30-Pin SIP	Call Factory
KMM58256	256K × 8	120/150	NMOS	Page Mode	30-Pin SIMM (Edge Connector)	Call Factory
KMM49256	256K × 9	120/150	NMOS	Page Mode	30-Pin SIP	Call Factory
KMM59256	256K × 9	120/150	NMOS	Page Mode	30-Pin SIMM (Edge Connector)	Call Factory
*KMM481000A	1M × 8	80/100	CMOS	Fast Page Mode	30-Pin SIP	Call Factory
*KMM581000A	1M × 8	80/100	CMOS	Fast Page Mode	30-Pin SIMM (Edge Connector)	Call Factory
*KMM491000A	1M × 9	80/100	CMOS	Fast Page Mode	30-Pin SIP	Call Factory
*KMM591000A	1M × 9	80/100	CMOS	Fast Page Mode	30-Pin SIMM (Edge Connector)	Call Factory

2.3 Static RAM

Capacity	Part Name	Organization	Speed (ns)	Technology	Current		Package	Remark
					Active, mA Typ (max)	Standby, μA Typ (max)		
64K	†KM6165	64K × 1	25/35/45	CMOS	(100)	(2mA)	SDIP/SOJ	TBA
	†KM6165L	64K × 1	25/35/45	CMOS	(100)	(100)	SDIP/SOJ	TBA
	†KM6465	16K × 4	25/35/45	CMOS	(100)	(2mA)	SDIP	TBA
	†KM6465L	16K × 4	25/35/45	CMOS	(100)	(100)	SDIP	TBA
	†KM6865	8K × 8	35/45/55	CMOS	(120)	(2mA)	SDIP	TBA
	†KM6865L	8K × 8	35/45/55	CMOS	(120)	(100)	SDIP	TBA
	KM6264A	8K × 8	70/100/120	CMOS	(70)	(2mA)	DIP/SOP	Now
	KM6264AL	8K × 8	70/100/120	CMOS	(70)	2(100)	DIP/SOP	Now
256K	*KM61257	256K × 1	25/35/45	CMOS	(100)	(2mA)	SDIP/SOJ	Now
	*KM61257L	256K × 1	25/35/45	CMOS	(100)	(100)	SDIP/SOJ	Now
	*KM64257	64K × 4	25/35/45	CMOS	(120)	(2mA)	SDIP/SOJ	Now
	*KM64257L	64K × 4	25/35/45	CMOS	(120)	(100)	SDIP/SOJ	Now
	†KM68257P	32K × 8	35/45/55	CMOS	(120)	(2mA)	DIP	TBA
	†KM68257LP	32K × 8	35/45/55	CMOS	(120)	(100)	DIP	TBA
	KM62256A	32K × 8	80/100/120	CMOS	(70)	(2mA)	DIP/SOP	Now
	KM62256AL	32K × 8	80/100/120	CMOS	(70)	2(100)	DIP/SOP	Now
1M	††KM681000	128K × 8	70/100/120	CMOS	(70)	(2mA)	DIP/SOP	TBA
	††KM681000L	128K × 8	70/100/120	CMOS	(70)	2(100)	DIP/SOP	TBA

*: New Product
†: Preliminary Product
††: Under Development
TBA: To Be Announced

2.4 EEPROM

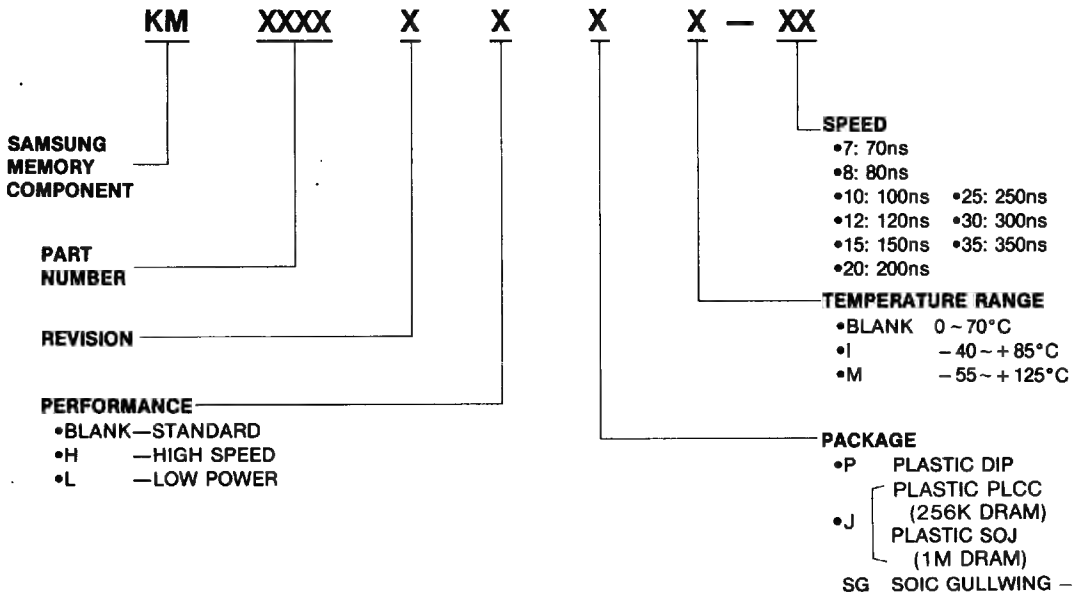
Capacity	Part Number	Organization	Speed (ns)	Technology	Write Cycle Time (ms)	Features	Packages	Remarks
256K bit	*KM93C06	16 × 16	250KHz	CMOS	10	Ext.-timed	8 DIP	Now
	*KM93C07	16 × 16	250KHz	CMOS	10	Self-timed	8 DIP	Now
1K bit	*KM93C46/G	64 × 16	250KHz	CMOS	10	Self-timed	8 DIP/8 SOP	Now
	*KM93C46I	64 × 16	250KHz	CMOS	10	Industrial	8 DIP	Now
16K bit	KM28C16/J	2K × 8	150/200/250	CMOS	2	$\overline{D}$-P, 32 Page Mode	24 DIP/32 PLCC	Now
	*KM28C16I	2K × 8	150/200/250	CMOS	2	Industrial	24 DIP	Now
	KM28C17/J	2K × 8	150/200/250	CMOS	2	$\overline{D}$-P, R/$\overline{B}$	28 DIP/32 PLCC	Now
	*KM28C17I	2K × 8	150/200/250	CMOS	2	Industrial	28 DIP	Now
64K bit	KM28C64/J	8K × 8	200/250	CMOS	5	$\overline{D}$-P, 32 Page Mode	28 DIP/32 PLCC	Now
	*KM28C64I	8K × 8	200/250	CMOS	5	Industrial	28 DIP	Now
	KM28C65/J	8K × 8	200/250	CMOS	5	$\overline{D}$-P, R/$\overline{B}$	28 DIP/32 PLCC	Now
	*KM28C65I	8K × 8	200/250	CMOS	5	Industrial	28 DIP	Now
256K bit	†KM28C256/J	32K × 8	150/200/250	CMOS	5	$\overline{D}$-P, T-$\overline{B}$, 64 Page Mode	28 DIP/32 PLCC	2Q, '89
	†KM28C256I	32K × 8	150/200/250	CMOS	5	Industrial	28 DIP	2Q, '89

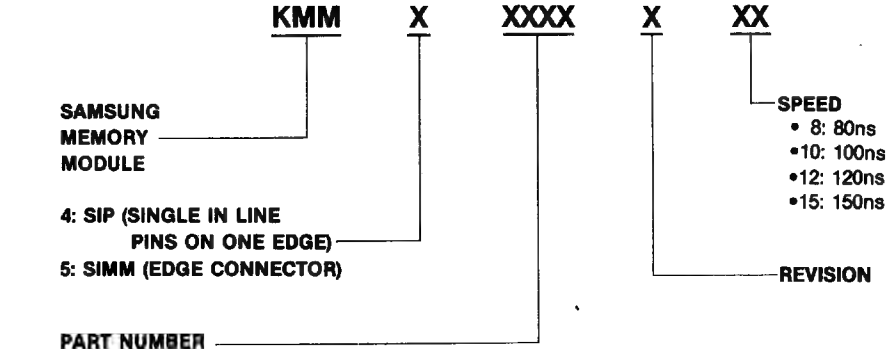
*: D-P: Data-Polling, R/B: Ready/$\overline{Busy}$, T-B: Toggle Bit

2.5 Mask ROM

Capacity	Part Number	Organization	Speed (ns)	Technology	Features	Packages	Remark
64K bit	KM2364	8K × 8	250	NMOS	—	24 DIP	
	KM2365	8K × 8	250	NMOS	Programmable chip select	28 DIP	Now
128K bit	KM23128	16K × 8	250	NMOS	Programmable chip select	28 DIP	Now
256K bit	KM23256	32K × 8	250	NMOS	Programmable chip select	28 DIP	Now
	KM23257	32K × 8	250	NMOS	Programmable chip select	28 DIP	Now
512K bit	KM23C512	64K × 8	250	CMOS	Programmable output enable	28 DIP	4Q, 1989
1M bit	KM23C1000	128K × 8	200 250	CMOS	Programmable chip select	28 DIP	4Q, 1989
4M bit	KM23C4000-15	512K × 8	150	CMOS	Programmable	28 DIP	4Q, 1989
	KM23C4000-20	512K × 8	200	CMOS	chip select &	28 DIP	4Q, 1989
	KM23C4000-25	512K × 8	250	CMOS	output enable	28 DIP	4Q, 1989

3. ORDERING INFORMATION





1. KM4164B
2. KM41256A/KM41257A
3. KM41464A
4. KM41C1000A
5. KM41C1001A
6. KM41C1002A
7. KM44C256A
8. KM44C258A
9. KM41C4000
10. KM44C1000
11. KM424C256
12. KMM4(5)8256/KMM4(5)8257
13. KMM4(5)9256/KMM4(5)9257
14. KMM4(5)81000A
15. KMM4(5)91000A

Dynamic RAM

Capacity	Part Number	Organization	Speed (ns)	Technology	Features	Packages	Remark
64K bit	KM4164BP	64K × 1	100/120/150	NMOS	Page Mode	16-Pin DIP	Now
256K bit	KM41256AP	256K × 1	100/120/150	NMOS	Page Mode	16-Pin DIP	Now
	KM41256AJ	256K × 1	100/120/150	NMOS	Page Mode	18-Pin PLCC	Now
	KM41256AZ	256K × 1	100/120/150	NMOS	Page Mode	16-Pin ZIP	Now
	KM41257AP	256K × 1	100/120/150	NMOS	Nibble Mode	16-Pin DIP	Now
	KM41257AJ	256K × 1	100/120/150	NMOS	Nibble Mode	18-Pin PLCC	Now
	KM41257AZ	256K × 1	100/120/150	NMOS	Nibble Mode	16-Pin ZIP	Now
	KM41464AP	64K × 4	120/150	NMOS	Page Mode	18-Pin DIP	Now
	KM41464AJ	64K × 4	120/150	NMOS	Page Mode	18-Pin PLCC	Now
	KM41464AZ	64K × 4	120/150	NMOS	Page Mode	20-Pin ZIP	Now
1M bit	KM41C1000AP	1M × 1	70/80/100	CMOS	Fast Page Mode	18-Pin DIP	Now
	KM41C1000AJ	1M × 1	70/80/100	CMOS	Fast Page Mode	20-Pin SOJ	Now
	KM41C1000AZ	1M × 1	70/80/100	CMOS	Fast Page Mode	20-Pin ZIP	Now
	KM41C1001AP	1M × 1	70/80/100	CMOS	Nibble Mode	18-Pin DIP	Now
	KM41C1001AJ	1M × 1	70/80/100	CMOS	Nibble Mode	20-Pin SOJ	Now
	KM41C1001AZ	1M × 1	70/80/100	CMOS	Nibble Mode	20-Pin ZIP	Now
	KM41C1002AP	1M × 1	70/80/100	CMOS	Static Col. Mode	18-Pin DIP	Now
	KM41C1002AJ	1M × 1	70/80/100	CMOS	Static Col. Mode	20-Pin SOJ	Now
	KM41C1002AZ	1M × 1	70/80/100	CMOS	Static Col. Mode	20-Pin ZIP	Now
	KM44C256AP	256K × 4	80/100/120	CMOS	Fast Page Mode	20-Pin DIP	Now
	KM44C256AJ	256K × 4	80/100/120	CMOS	Fast Page Mode	20-Pin SOJ	Now
	KM44C256AZ	256K × 4	80/100/120	CMOS	Fast Page Mode	20-Pin ZIP	Now
	KM44C258AP	256K × 4	80/100/120	CMOS	Static Col. Mode	20-Pin DIP	Now
	KM44C258AJ	256K × 4	80/100/120	CMOS	Static Col. Mode	20-Pin SOJ	Now
	KM44C258AZ	256K × 4	80/100/120	CMOS	Static Col. Mode	20-Pin ZIP	Now
4M bit	KM41C4000J	4M × 1	80/100/120	CMOS	Fast Page Mode	20-Pin SOJ	TBA
	KM44C1000J	1M × 4	80/100/120	CMOS	Fast Page Mode	20-Pin SOJ	TBA
Video RAM	KM424C256P	256K × 4	RAM: 80/100/120 SAM: 20/25/35	CMOS	Fast Page Mode Serial In/Out	28-Pin DIP	TBA
	KM424C256J	256K × 4	RAM: 80/100/120 SAM: 20/25/35	CMOS	Fast Page Mode Serial In/Out	28-Pin SOJ	TBA
	KM424C256Z	256K × 4	RAM: 80/100/120 SAM: 20/25/35	CMOS	Fast Page Mode Seria In/Out	28-Pin ZIP	TBA
Module	KMM48256	256K × 8	120/150	NMOS	Page Mode	30-Pin SIP	Call Factory
	KMM58256	256K × 8	120/150	NMOS	Page Mode	30-Pin SIMM (Edge Connector)	Call Factory
	KMM49256	256K × 9	120/150	NMOS	Page Mode	30-Pin SIP	Call Factory
	KMM59256	256K × 9	120/150	NMOS	Page Mode	30-Pin SIMM (Edge Connector)	Call Factory
	KMM481000A	1M × 8	80/100	CMOS	Fast Page Mode	30-Pin SIP	Call Factory
	KMM581000A	1M × 8	80/100	CMOS	Fast Page Mode	30-Pin SIMM (Edge Connector)	Call Factory
	KMM491000A	1M × 9	80/100	CMOS	Fast Page Mode	30-Pin SIP	Call Factory
	KMM591000A	1M × 9	80/100	CMOS	Fast Page Mode	30-Pin SIMM (Edge Connector)	Call Factory

64K x 1 Bit Dynamic RAM with Page Mode

FEATURES

- **Performance range**

	t_{RAC}	t_{CAC}	t_{RC}
KM4164B-10	100ns	55ns	190ns
KM4164B-12	120ns	60ns	220ns
KM4164B-15	150ns	75ns	260ns

- **Page Mode capability**
- **Single +5V ±10% power supply**
- **Common I/O using early write**
- **TTL compatible inputs and output**
- **Schmitt Triggers on all input control lines**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **128 cycle/2ms refresh**
- **Jedec standard pinout in 16-pin DIP**

GENERAL DESCRIPTION

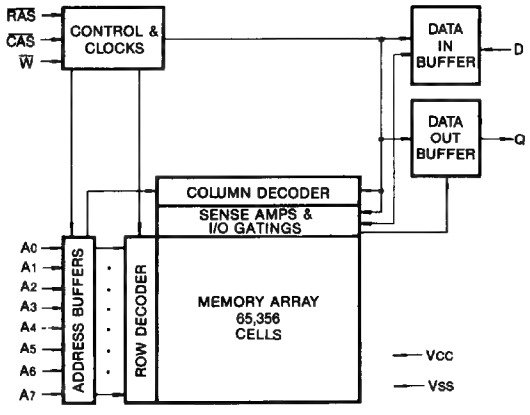
The KM4164B is a fully decoded NMOS Dynamic Random Access Memory organized as 65,536 one-bit words. The design is optimized for high speed, high performance applications such as computer memory, peripheral storage and environments where low power dissipation and compact layout are required.

The KM4164B features page mode which allows high speed random access of up to 256-bits within the same row. Multiplexed row and column address inputs permit the KM4164B to be housed in a standard 16-pin DIP.

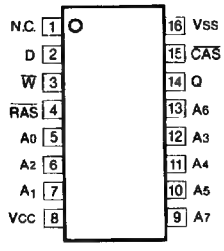
The KM4164B is fabricated using Samsung's advanced silicon gate NMOS process. This process, coupled with single transistor memory storage cells, permits maximum circuit density and minimal chip size.

Clock timing requirements are noncritical, and power supply tolerance is very wide. All inputs and output are TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Pin Name	Pin Function
A_0-A_7	Address inputs
D	Data In
Q	Data Out
$\overline{W}$	Read/Write Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
V_{CC}	Power (+5V)
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Units
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	−2.0 to +7.0	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	−1 to +7.5	V
Storage Temperature	T_{stg}	−65 to +150	°C
Power Dissipation	P_D	1.0	W
Short Circuit Output Current	I_{OS}	50	mA

*Permanent device damage may occur of "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS}, $T_A = 0$ to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	$V_{CC}+1$	V
Input Low Voltage	V_{IL}	−2.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$ and $\overline{CAS}$ cycling; @t_{RC} = min.)	KM4164B-10	I_{CC1}	—	60	mA
	KM4164B-12		—	50	mA
	KM4164B-15		—	45	mA
Standby Current ($\overline{RAS} = \overline{CAS} = V_{IH}$ after 8 $\overline{RAS}$ cycles min.)		I_{CC2}	—	4	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS} = V_{IH}$, $\overline{RAS}$ cycling; @t_{RC} = min.)	KM4164B-10	I_{CC3}	—	50	mA
	KM4164B-12		—	40	mA
	KM4164B-15		—	35	mA
Page Mode Current* ($\overline{RAS} = V_{IL}$, $\overline{CAS}$ cycling; @t_{PC} = min.)	KM4164B-10	I_{CC4}	—	45	mA
	KM4164B-12		—	35	mA
	KM4164B-15		—	30	
Input Leakage Current (Any input $0 \le V_{IN} \le 5.5V$, $V_{CC} = 5.5V$, $V_{SS} = 0V$, all other pins not under test = 0 volts.)		I_{IL}	−10	10	μA
Output Leakage Current (Data out is disabled, $0 \le V_{OUT} \le 5.5V$, $V_{CC} = 5.5V$, $V_{SS} = 0V$)		I_{OL}	−10	10	μA
Output High Voltage Level ($I_{OH} = -5mA$)		V_{OH}	2.4	—	V
Output Low Voltage Level ($I_{OL} = 4.2mA$)		V_{OL}	—	0.4	V

*Note: I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current.

CAPACITANCE ($T_A = 25°C$)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A_0-A_7, D)	C_{IN1}	—	5	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, W)	C_{IN2}	—	7	pF
Output Capacitance (Q)	C_{OUT}	—	6	pF

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC} = 5.0V \pm 10\%$. See notes 1,2.)

Parameter	Symbol	KM4164B-10		KM4164B-12		KM4164B-15		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	190		220		260		ns	
Read-modify-write cycle time	t_{RWC}	215		255		300		ns	
Access time from $\overline{RAS}$	t_{RAC}		100		120		150	ns	3, 4
Access time from $\overline{CAS}$	t_{CAC}		55		60		75	ns	3, 5
Output buffer turn-off delay time	t_{OFF}	0	25	0	30	0	35	ns	6
Transition time (rise and fall)	t_T	3	100	3	100	3	100	ns	
$\overline{RAS}$ precharge time	t_{RP}	80		90		100		ns	
$\overline{RAS}$ pulse width	t_{RAS}	100	10,000	120	10,000	150	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	55		60		75		ns	
$\overline{CAS}$ pulse width	t_{CAS}	55	10,000	60	10,000	75	10,000	ns	
$\overline{CAS}$ hold time	t_{CSH}	100		120		150		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	15	45	20	60	25	75	ns	4
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	0		0		0		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	15		18		20		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	25		30		35		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	70		90		110		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	
Write command set-up time	t_{WCS}	0		0		0		ns	7
Write command hold time	t_{WCH}	30		35		45		ns	
Write command pulse width	t_{WP}	30		35		45		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	25		35		45		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	25		35		45		ns	
Data-in set-up time	t_{DS}	0		0		0		ns	
Data-in hold time	t_{DH}	30		35		40		ns	
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	50		55		65		ns	7

AC CHARACTERISTICS (Continued)

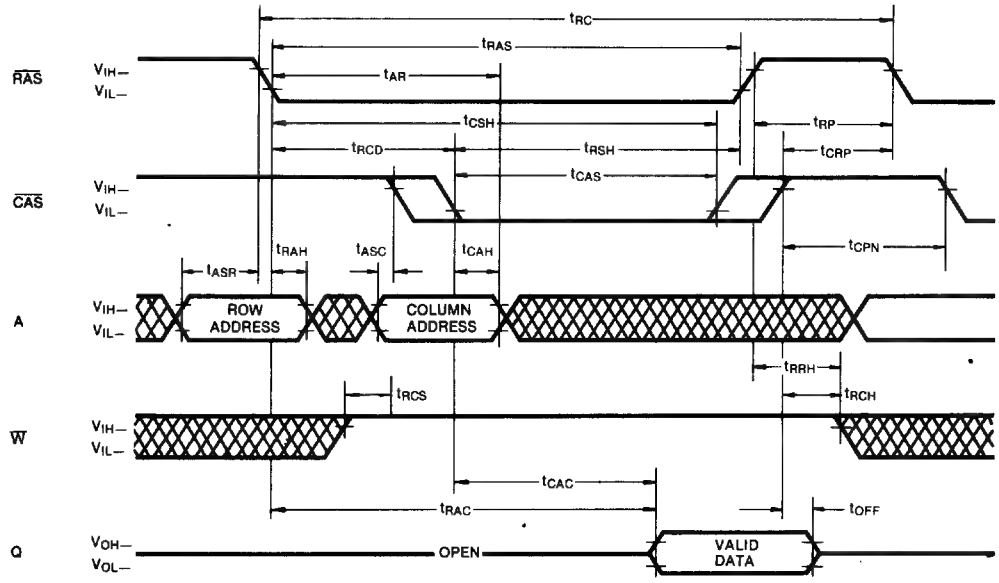
Parameter	Symbol	KM4164B-10		KM4164B-12		KM4164B-15		Units	Notes
		Min	Max	Min	Max	Min	Max		
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	95		115		140		ns	7
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	75		95		120		ns	
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	75		95		115		ns	
Page mode cycle time	t_{PC}	105		120		145		ns	
$\overline{CAS}$ precharge time (page mode only)	t_{CP}	40		45		60		ns	
$\overline{CAS}$ precharge time (all cycles except page mode)	t_{CPN}	25		25		30		ns	
Refresh period	t_{REF}		2		2		2	ms	

NOTES

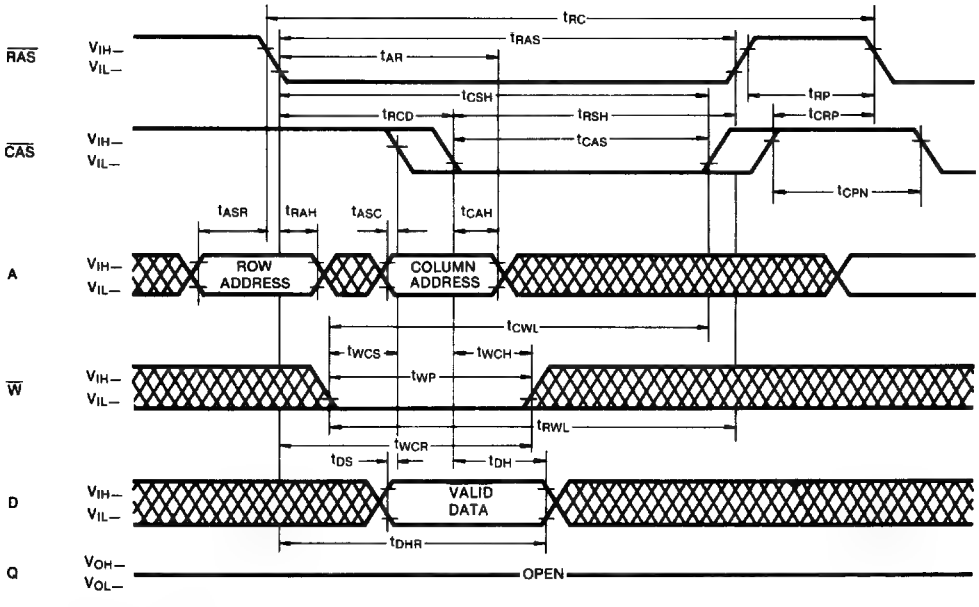
1. An initial pause of 100μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(mas) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met, t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$(max).
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
7. t_{CWD} and t_{RWD} are restrictive operating parameters for the read-modify-write cycle only. If $t_{WCS} \geq t_{WCS}$(min), the cycle is an early write cycle and the data output will remain open circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$(min) and $t_{RWD} > t_{RWD}$(min), the cycle is a late write cycle and the data output will contain data read from the selected cell. If neither of the above conditions are met, the condition of the data out (at access time until $\overline{CAS}$ goes back to V_{IH}) is indeterminate.

TIMING DIAGRAMS

READ CYCLE

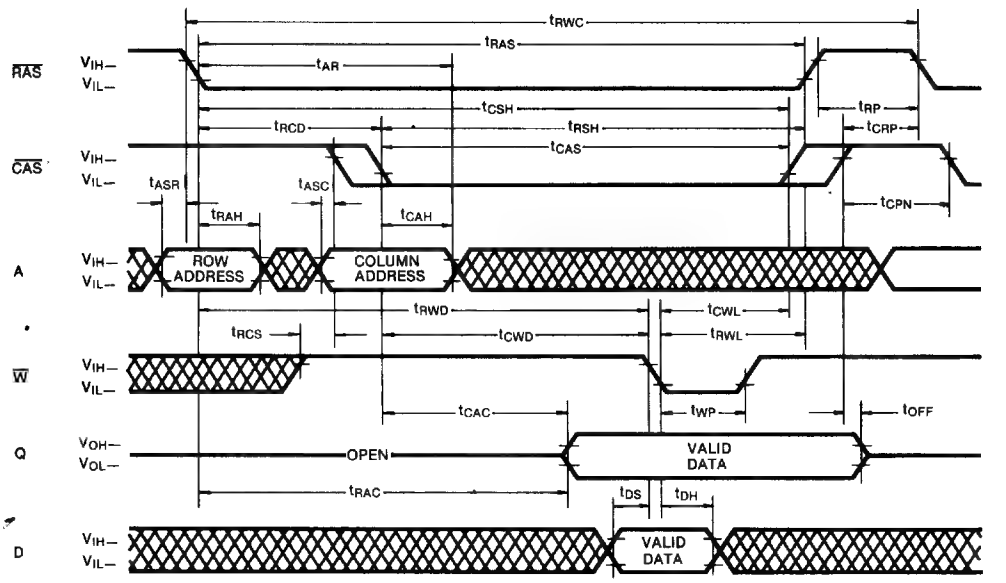


WRITE CYCLE (EARLY WRITE)

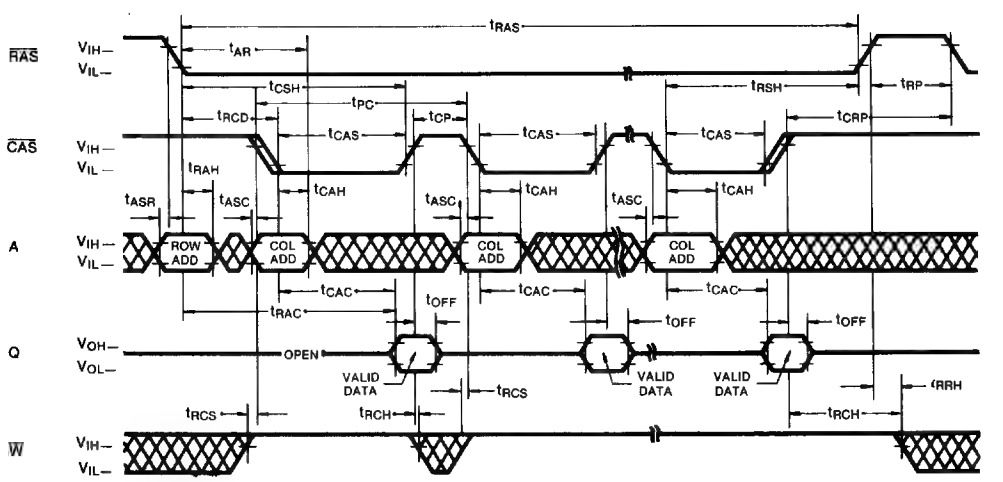


TIMING DIAGRAMS (Continued)

READ-WRITE/READ-MODIFY-WRITE CYCLE



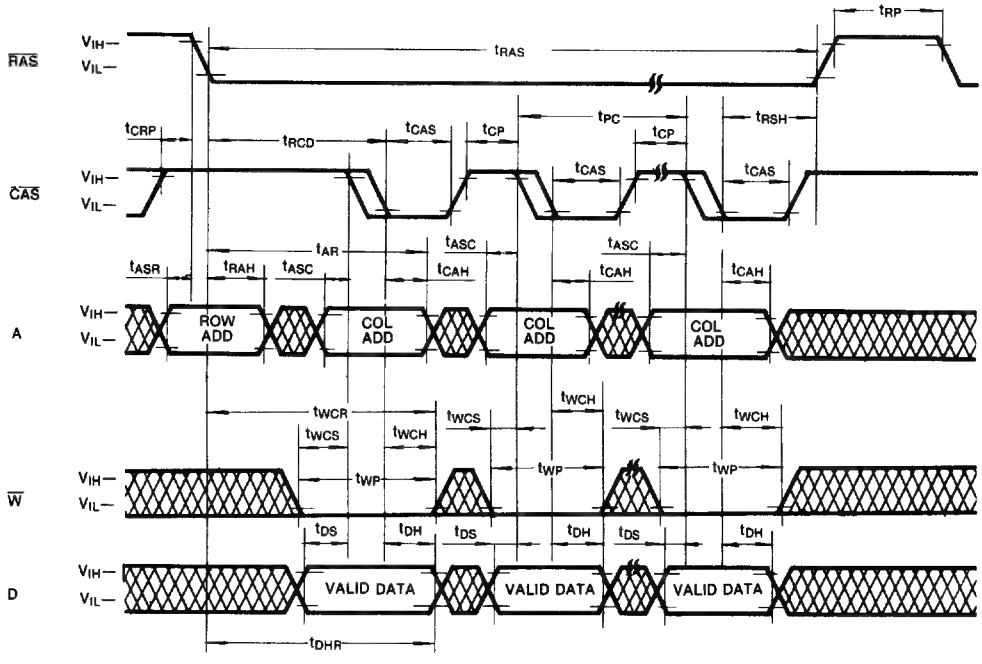
PAGE MODE READ CYCLE



DON'T CARE

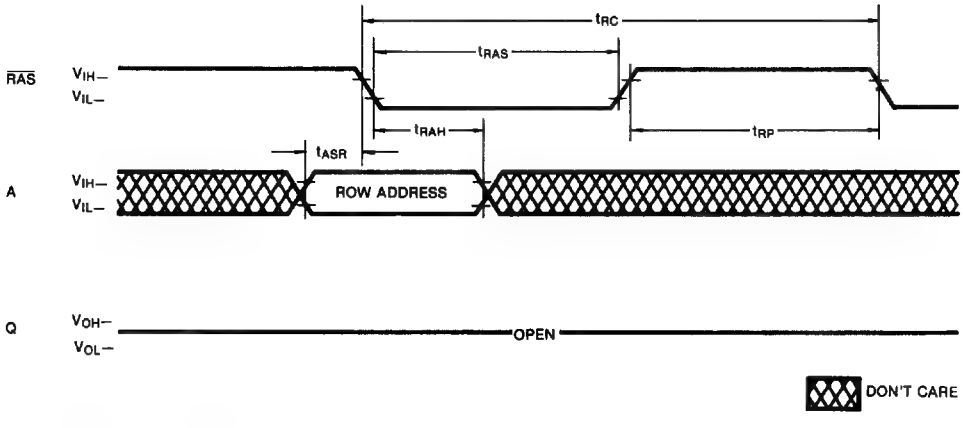
TIMING DIAGRAMS (Continued)

PAGE MODE WRITE CYCLE



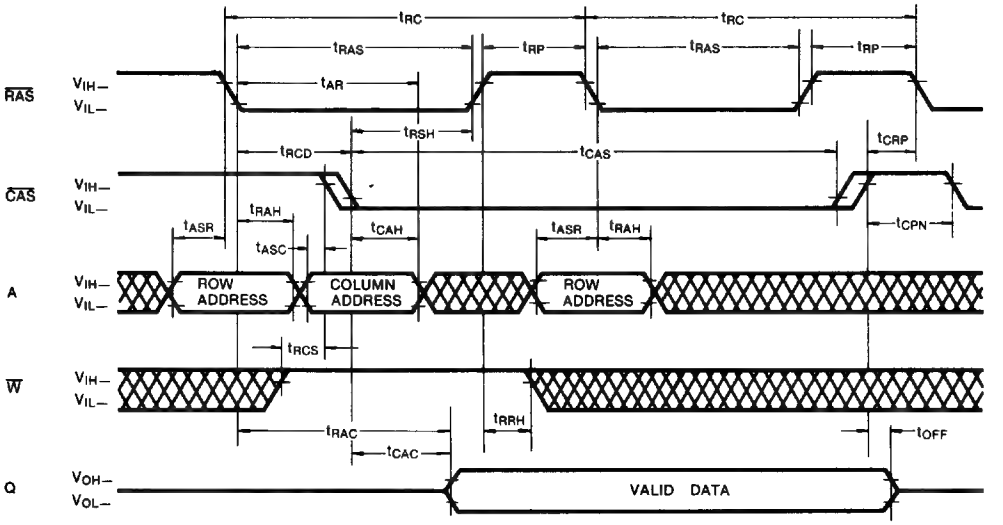
RAS-ONLY REFRESH CYCLE

Note: $\overline{CAS} \fallingdotseq V_{IH}$ $\overline{W}$,D = Don't care



TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE



KM4164B OPERATION

Device Operation

The KM4164B contains 65,536 memory locations. Sixteen address bits are required to address a particular memory location. Since the KM4164B has only 8 address input pins, time multiplexed addressing is used to input 8 row and 8 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{RAS}$), the column address strobe ($\overline{CAS}$) and the valid address inputs.

Operation of the KM4164B begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. Then the address on the 8 address input pins is changed from a row address to a column address and is strobed in by $\overline{CAS}$. This is the beginning of any KM4164B cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both $\overline{RAS}$ and $\overline{CAS}$ have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time (t_{RP}) requirement.

$\overline{RAS}$ and $\overline{CAS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CAS}$ pulse width are specified by t_{RAS}(min) and t_{CAS}(min) respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, t_{RP}, has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM4164B begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input ($\overline{W}$) high during a $\overline{RAS}$/$\overline{CAS}$ cycle. The output of the KM4164B remains in the Hi-Z state until valid data appears at the output. If $\overline{CAS}$ goes low before t_{RCD}(max), the access time to valid data is specified by t_{RAC}. If $\overline{CAS}$ goes low after t_{RCD}(max), the access time is measured

DEVICE OPERATION (Continued)

from $\overline{CAS}$ and is specified by t_{CAC}. In order to achieve the minimum access time, t_{RAC}(min), it is necessary to bring $\overline{CAS}$ low before t_{RCD}(max).

Write

The KM4164B can perform early write, late write and read-modify-write cycles. The difference between these cycles is in the state of data-out and is determined by the timing relationship between $\overline{W}$ and $\overline{CAS}$. In any type of write cycle, Data-in must be valid at or before the falling edge of $\overline{W}$ or $\overline{CAS}$, whichever is later.

Early Write: An early write cycle is performed by bringing $\overline{W}$ low before $\overline{CAS}$. The data at the data input pin (D) is written into the addressed memory cell. Throughout the early write cycle the output remains in the Hi-Z state. This cycle is good for common I/O applications because the data-in and data-out pins may be tied together without bus contention.

Read-Modify-Write: In this cycle, valid data from the addressed cell appears at the output before and during the time that data is being written into the same cell location. This cycle is achieved by bringing $\overline{W}$ low after $\overline{CAS}$ and meeting the data sheet read-modify-write cycle timing requirements. This cycle requires using a separate I/O to avoid bus contention.

Late Write: If $\overline{W}$ is brought low after $\overline{CAS}$, a late write cycle will occur. The late write cycle is very similar to the read-modify-write cycle except that the timing parameters, t_{RWD} and t_{CWD}, are not necessarily met. The state of data-out is indeterminate since the output could be either Hi-Z or contain data depending on the timing conditions. This cycle requires a separate I/O to avoid bus contention.

Data Output

The KM4164B has a tri-state output buffer which is controlled by $\overline{CAS}$ (and $\overline{W}$ for early write).
Whenever $\overline{CAS}$ is high (V_{IH}), the output is in the high impedance (Hi-Z) state, In any cycle in which valid data appears at the output, the output first remains in the Hi-Z state until the data is valid and then the valid data appears at the output. The valid data remains at the output until $\overline{CAS}$ returns high. This is true even if a new $\overline{RAS}$ cycle occurs (as in hidden refresh). Each of the KM4164B operating cycles are listed below after the corresponding output state produced by the cycle.

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Page Mode Read, Page Mode Read-Modify-Write.

Hi-Z Output State: Early Write, $\overline{RAS}$-only Refresh, Page Mode write, $\overline{CAS}$-only cycle.

Indeterminate Output State: Delayed Write

Refresh

The data in the KM4164B is stored on a tiny capacitor within each memory cell. Due to leakage, the data will leak off after a period of time. To maintain data integrity it is necessary to refresh each of the rows every 2 ms. There are several ways to accomplish this.

$\overline{RAS}$-Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{RAS}$ while $\overline{CAS}$ remains high.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the $\overline{CAS}$ active time and strobing in a refresh row address with $\overline{RAS}$.

Other Refresh Methods: It is also possible to refresh the KM4164B by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in that row are automatically refreshed. There are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{RAS}$-only refresh is the preferred method.

Page Mode

Page mode memory cycles provide faster access and lower power dissipation than normal memory cycles. In page mode, it is possible to perform read, write or read-modify-write cycles. As long as the applicable timing requirements are observed it is possible to mix these cycles in any order. A page mode cycle begins with a normal cycle. While $\overline{RAS}$ is kept low to maintain the row address, $\overline{CAS}$ is cycled to strobe in additional column addresses. This eliminates the time required to set up and strobe sequential row addresses for the same page.

Power-up

If $\overline{RAS} = V_{SS}$ during power-up the KM4164B might begin an active cycle. This condition results in higher than necessary current demands from the power supply during power-up. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{CC} during power-up or be held at a valid V_{IH} in order to minimize the power-up current.

An initial pause of 100μsec is required after power-up followed by 8 initialized cycles before proper device

DEVICE OPERATION (Continued)

operation is assured. Eight initialization cycles are also required after any 2 ms period in which there are no $\overline{RAS}$ cycles. An initialization cycle is any cycle in which $\overline{RAS}$ is cycled.

Termination

The lines from the TTL driver circuits to the KM4164B inputs act like unterminated transmission lines resulting in significant positive and negative overshoots at the inputs. To minimize overshoot it is advisable to terminate the input lines and to keep them as short as possible. Although either series or parallel termination may be used, series termination is generally recommended since it is simple and draws no additional power. It consists of a resistor in series with the input line placed close to the KM4164B input pin. The optimum value depends on the board layout. It must be determined experimentally and is usually in the range of 20 to 40 ohms.

Board Layout

It is important to lay out the power and ground lines on memory boards in such a way that switching transient effects are minimized. The recommended methods are gridded power and ground lines or separate power and ground planes. The power and ground lines act like transmission lines to the high frequency transients generated by DRAMS. The impedance is minimized if all the power supply traces to all the DRAMS run both horizontally and vertically and are connected at each intersection or better yet if power and ground planes are used.

Address and control lines should be as short as possible to avoid skew. In boards with many DRAMS these lines should fan out from a central point like a fork or comb rather than being connected in a serpentine pattern. Also the control logic should be centrally located on large memory boards to facilitate the shortest possible address and control lines to all the DRAMS.

Decoupling

The importance of proper decoupling cannot be over emphasized. Excessive transient noise or voltage droop on the V_{CC} line can cause loss of data integrity (soft errors). The total combined voltage changes over time in the V_{CC} to V_{SS} voltage (measured at the device pins) should not exceed 500mV.

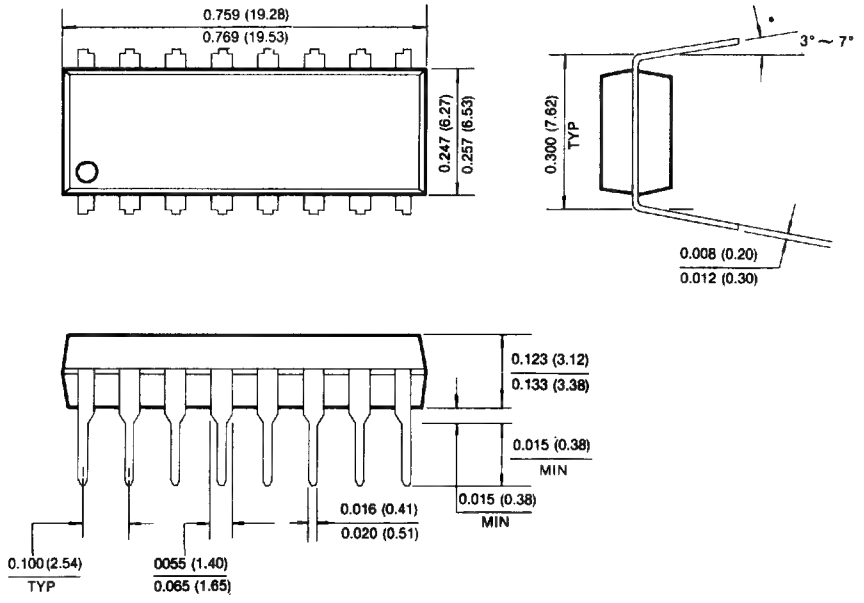
A high frequency 0.1μF ceramic decoupling capacitor should be connected between the V_{CC} and ground pins of each KM4164B using the shortest possible traces. These capacitors act as a low impedance shunt for the high frequency switching transients generated by the KM4164B and they supply much of the current used by the KM4164B during cycling.

In addition, a large tantalum capacitor with a value of 47μF to 100μF should be used for bulk decoupling to recharge the 0.1μF capacitors between cycles, thereby reducing power line droop. The bulk decoupling capacitor should be placed near the point where the power traces meet the power grid or power plane. Even better results may be achieved by distributing more than one tantalum capacitor throughout the memory array.

PACKAGE DIMENSIONS

16-LEAD PLASTIC DUAL IN-LINE PACKAGE

Units: Inches (millimeters)



256K x 1 Bit Dynamic RAM with Page/Nibble Mode

FEATURES

- **Performance range**

	t_{RAC}	t_{CAC}	t_{RC}
KM41256/7A-10	100ns	50ns	200ns
KM41256/7A-12	120ns	60ns	230ns
KM41256/7A-15	150ns	75ns	260ns

- **Page Mode capability-KM41256A**
- **Nibble Mode capability-KM41257A**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **TTL compatible inputs and output**
- **Common I/O using early write**
- **Single +5V±10% power supply**
- **256 cycle/4ms refresh**
- **Jedec standard pinout in 16-pin plastic DIP, 18 lead PLCC and 16-pin plastic ZIP.**

DESCRIPTION

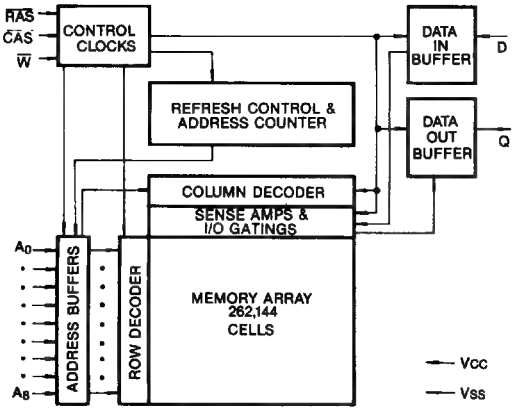
The KM41256/7A is a fully decoded NMOS Dynamic Random Access Memory organized as 262,144 one-bit words. The design is optimized for high speed, high performance applications such as computer memory, buffer memory, peripheral storage and environments where low power dissipation and compact layout are required.

The KM41256A features page mode which allows high speed random access of memory cells within the same row. The KM41257A features nibble mode which allows high speed serial access of up to 4 bits of data. $\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. Multiplexed row and column address inputs permit the KM41256/7A to be housed in a JEDEC standard 16-pin DIP.

The KM41256/7A is fabricated using Samsung's advanced silicon gate NMOS process. This process, coupled with single transistor memory storage cells, permits maximum circuit density and minimal chip size.

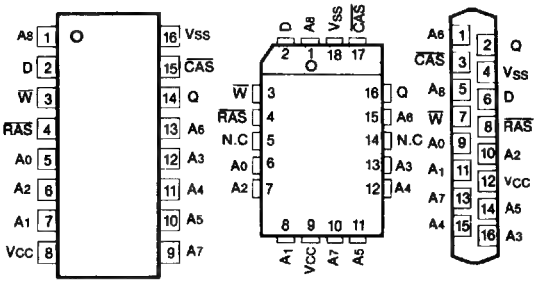
Clock timing requirements are noncritical, and power supply tolerance is very wide. All inputs and output are TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS

- **KM41256/7AP** **•KM41256/7AJ** **•KM41256/7AZ**



Pin Name	Pin Function
A_0-A_8	Address Inputs
D	Data In
Q	Data Out
$\overline{W}$	Read/Write Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
V_{CC}	Power (+5V)
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Units
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7.0	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	−1 to +7.0	V
Storage Temperature	T_{stg}	−55 to +150	°C
Power Dissipation	P_D	1.0	W
Short Circuit Output Current	I_{OS}	50	mA

*Permanent device damage may occur of ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS}, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC}+1	V
Input Low Voltage	V_{IL}	−1	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$ and $\overline{CAS}$ cycling; @t_{RC} = min.)	KM41256/7A-10	I_{CC1}	—	85	mA
	KM41256/7A-12		—	75	mA
	KM41256/7A-15		—	65	mA
Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		I_{CC2}	—	4.5	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS}$ = V_{IH}, $\overline{RAS}$ cycling; @t_{RC} = min.)	KM41256/7A-10	I_{CC3}	—	70	mA
	KM41256/7A-12		—	65	mA
	KM41256/7A-15		—	60	mA
Page Mode Current* ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling; @t_{PC} = min.)	KM41256A-10	I_{CC4}	—	65	mA
	KM41256A-12		—	55	mA
	KM41256A-15		—	45	mA
Nibble Mode Current* ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling; @t_{NC} = min.)	KM41257A-10	I_{CC5}	—	65	mA
	KM41257A-12		—	55	mA
	KM41257A-15		—	45	mA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ cycling @t_{RC} = min.)	KM41256/7A-10	I_{CC6}	—	70	mA
	KM41256/7A-12		—	65	mA
	KM41256/7A-15		—	60	mA
Input Leakage Current (Any input $0 \leq V_{IN} \leq 5.5V$, V_{CC} = 5.5V, V_{SS} = 0V, all other pins not under test = 0 volts.)		I_{IL}	−10	10	μA

DC AND OPERATING CHARACTERISTICS (Continued)

Parameter	Symbol	Min	Max	Units
Output Leakage Current (Data out is disabled, $0V \leq V_{OUT} \leq 5.5V$, $V_{CC} = 5.5V$, $V_{SS} = 0V$)	I_{OL}	−10	10	μA
Output High Voltage Level ($I_{OH} = -5mA$)	V_{OH}	2.4	—	V
Output Low Voltage Level ($I_{OL} = 4.2mA$)	V_{OL}	—	0.4	V

*Note: I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current.

CAPACITANCE ($T_A = 25°C$)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A_0-A_8, D)	C_{IN1}	—	7	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{W}$)	C_{IN2}	—	10	pF
Output Capacitance (Q)	C_{OUT}	—	7	pF

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC} = 5.0V \pm 10\%$. See notes 1,2)

KM41256/7A STANDARD OPERATION

Parameter	Symbol	KM41256A-10 KM41257A-10		KM41256A-12 KM41257A-12		KM41256A-15 KM41257A-15		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	200		230		260		ns	
Read-modify-write cycle time	t_{RWC}	245		265		310		ns	
Access time from $\overline{RAS}$	t_{RAC}		100		120		150	ns	3,4
Access time from $\overline{CAS}$	t_{CAC}		50		60		75	ns	3,5
Output buffer turn-off delay time	t_{OFF}	0	25	0	30	0	40	ns	6
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	
$\overline{RAS}$ precharge time	t_{RP}	90		100		100		ns	
$\overline{RAS}$ pulse width	t_{RAS}	100	10,000	120	10,000	150	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	50		60		75		ns	
$\overline{CAS}$ precharge time (all cycles except page mode)	t_{CPN}	45		50		60		ns	
$\overline{CAS}$ pulse width	t_{CAS}	50	10,000	60	10,000	75	10,000	ns	
$\overline{CAS}$ hold time	t_{CSH}	110		120		150		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	50	25	60	25	75	ns	4
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	15		15		15		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		20		25		ns	

KM41256/7A STANDARD OPERATION (Continued)

Parameter	Symbol	KM41256A-10 KM41257A-10		KM41256A-12 KM41257A-12		KM41256A-15 KM41257A-15		Units	Notes
		Min	Max	Min	Max	Min	Max		
Column address hold time referenced to $\overline{RAS}$	t_{AR}	65		80		100		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	20		20		20		ns	
Write command set-up time	t_{WCS}	0		0		0		ns	7
Write command hold time	t_{WCH}	35		40		45		ns	
Write command pulse width	t_{WP}	35		40		45		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	40		40		45		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	40		40		45		ns	
Data-in set-up time	t_{DS}	0		0		0		ns	
Data-in hold time	t_{DH}	35		40		45		ns	
$\overline{CAS}$ to write enable delay time	t_{CWD}	50		60		75		ns	7
$\overline{RAS}$ to write enable delay time	t_{RWD}	100		120		150		ns	7
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	90		100		120		ns	
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	85		100		120		ns	
Refresh period (256 cycles)	t_{REF}		4		4		4	ms	

KM41256/7A $\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH

$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	20		25		30		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	50		55		60		ns	
Refresh counter test cycle time	t_{RTC}	330		375		430		ns	
Refresh counter test $\overline{CAS}$ precharge time	t_{CPT}	50		60		70		ns	
Refresh counter test $\overline{RAS}$ pulse width	t_{TRAS}	230		265		320		ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ hold time	t_{RPC}	20		20		20		ns	

KM41257A NIBBLE MODE

Nibble mode read/write cycle time	t_{NC}	50		60		75		ns	
Nibble mode read-write cycle time	t_{NRWC}	75		90		105		ns	
Nibble mode access time	t_{NCAC}		20		30		40	ns	
Nibble mode $\overline{CAS}$ pulse width	t_{NCAS}	20		30		40		ns	
Nibble mode $\overline{CAS}$ precharge time	t_{NCP}	20		25		30		ns	
Nibble mode $\overline{RAS}$ hold time	t_{NRSH}	30		40		50		ns	
Nibble mode $\overline{CAS}$ hold time referenced to $\overline{RAS}$	t_{RNH}	20		20		20		ns	
Nibble mode $\overline{CAS}$ to $\overline{W}$ delay time	t_{NCWD}	30		30		35		ns	
Nibble mode $\overline{W}$ to $\overline{CAS}$ lead time	t_{NCWL}	25		25		30		ns	

KM41256A PAGE MODE (Continued)

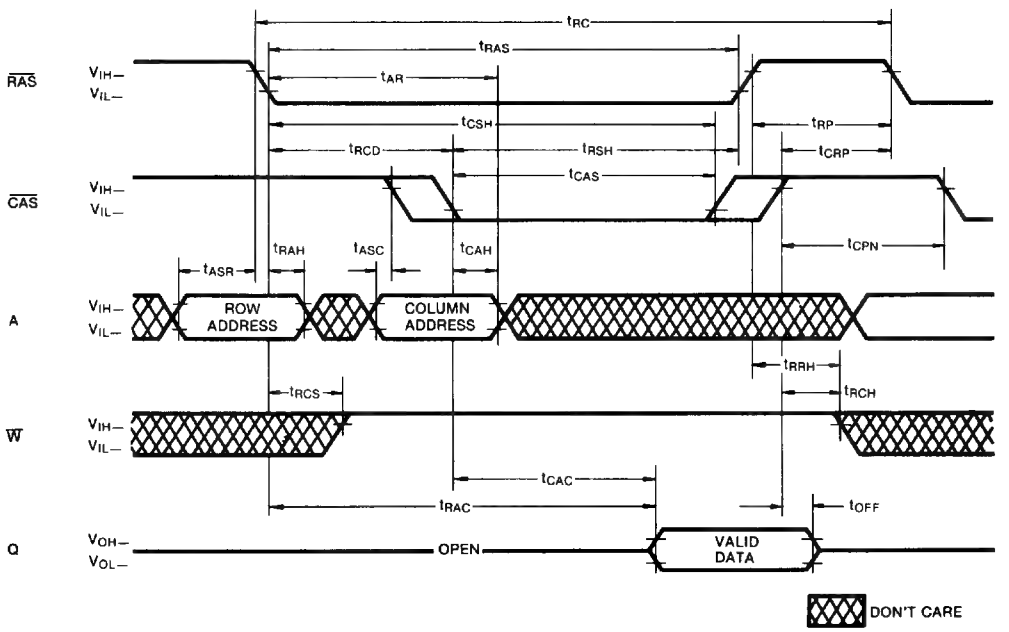
Parameter	Symbol	KM41256A-10		KM41256A-12		KM41256A-15		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Page mode cycle time	t_{PC}	100		120		145		ns	
$\overline{CAS}$ precharge time (page mode only)	t_{CP}	45		50		60		ns	

NOTES

1. An initial pause of 100μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$(max).
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
7. t_{CWD} and t_{RWD} are restrictive operating parameters for the read-modify-write cycle only. If $t_{WCS} \geq t_{WCS}$(min), the cycle is an early write cycle and the data output will remain open circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$(min) and $t_{RWD} > t_{RWD}$(min), the cycle is a late write cycle and the data output will contain data read from the selected cell. If neither of the above conditions are met, the condition of the data out (at access time until $\overline{CAS}$ goes back to V_{IH}) is indeterminate.

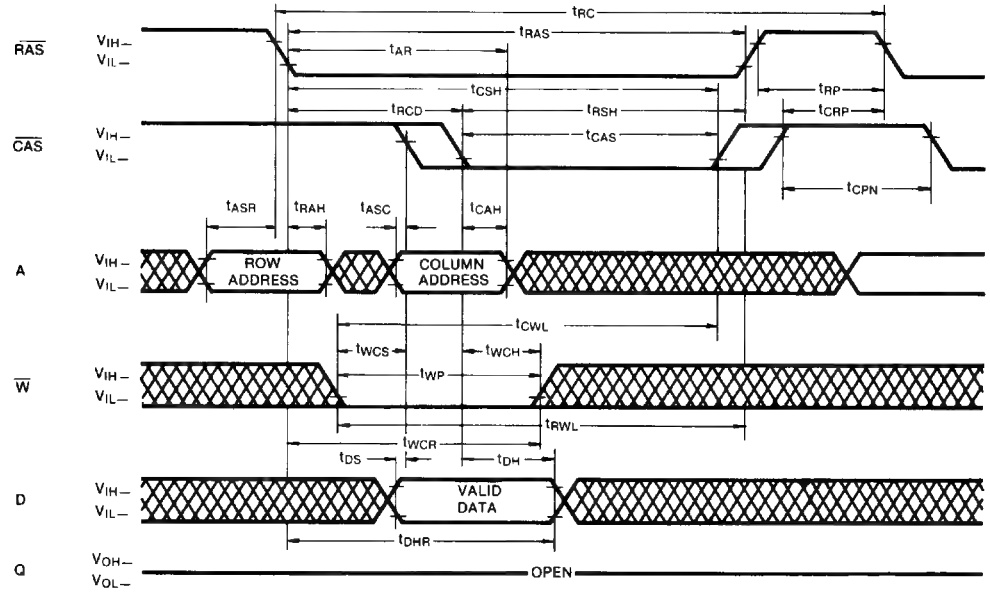
TIMING DIAGRAMS

READ CYCLE

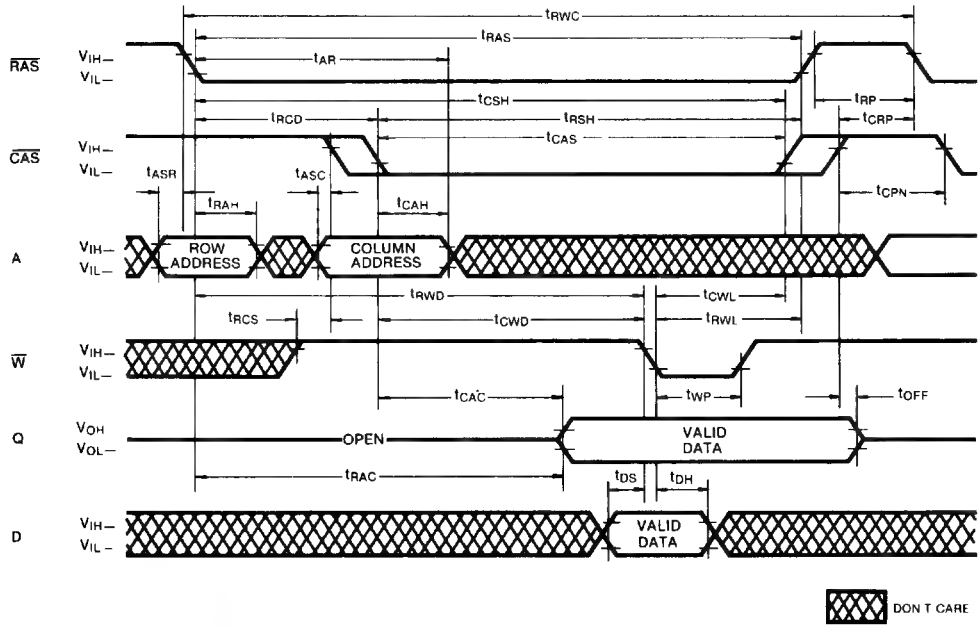


TIMING DIAGRAMS (Continued)

WRITE CYCLE (EARLY WRITE)

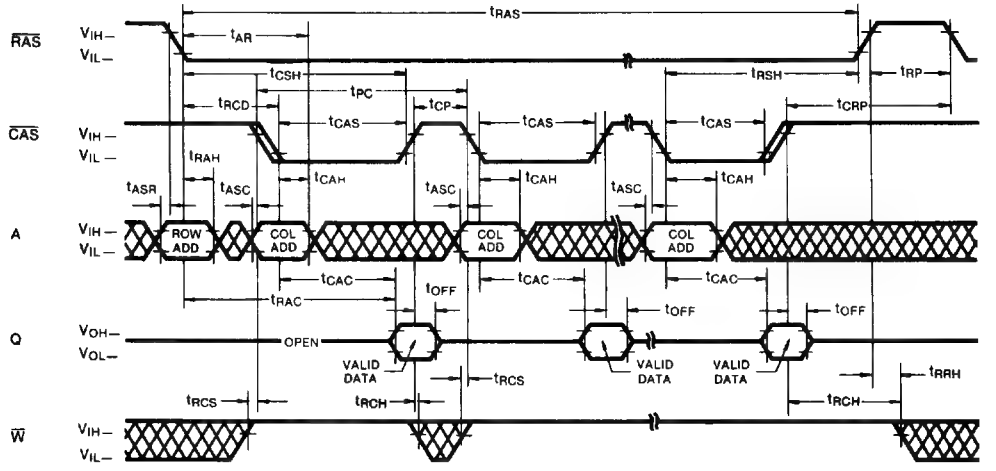


READ-WRITE/READ-MODIFY-WRITE CYCLE

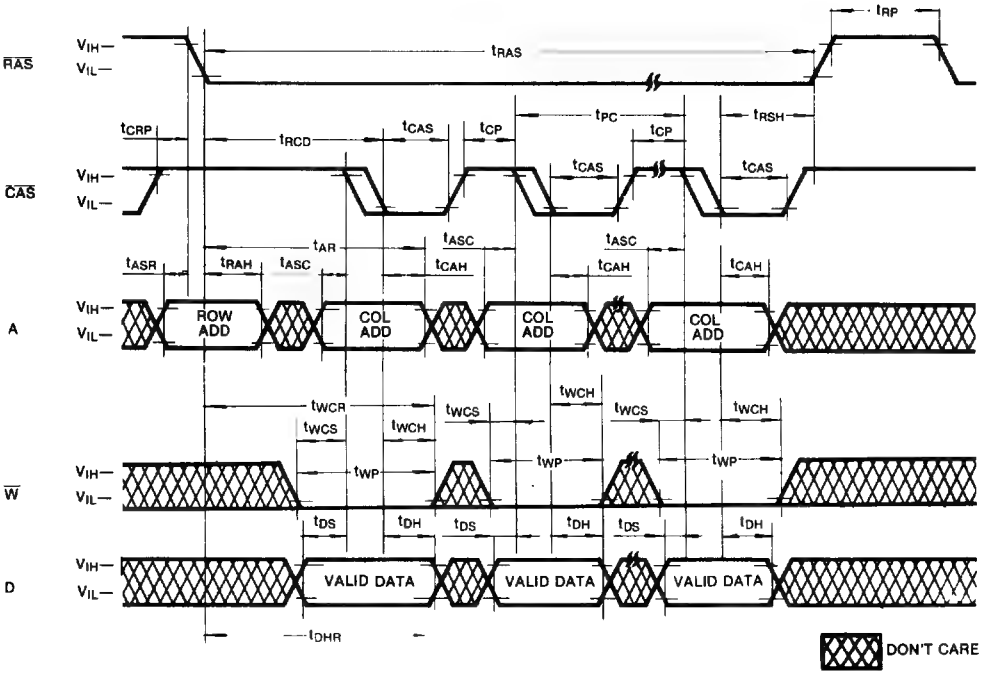


TIMING DIAGRAMS (Continued)

PAGE MODE READ CYCLE (KM41256A)

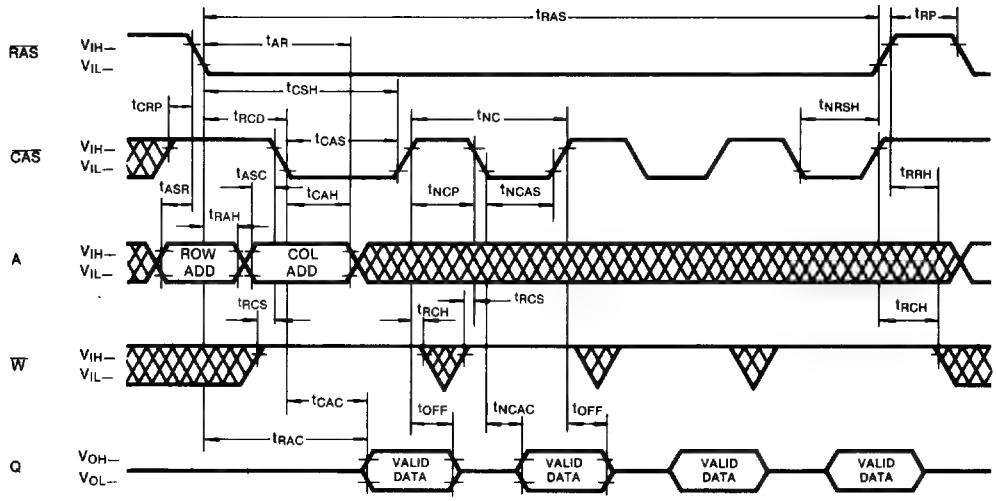


PAGE MODE WRITE CYCLE (KM41256A)

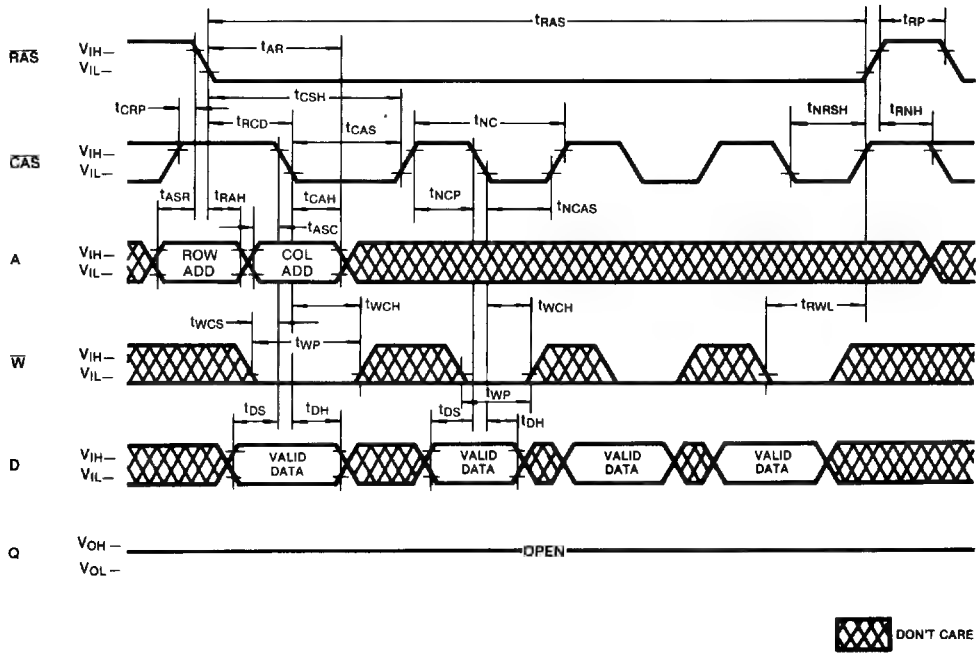


TIMING DIAGRAMS (Continued)

NIBBLE MODE READ CYCLE (KM41257A)

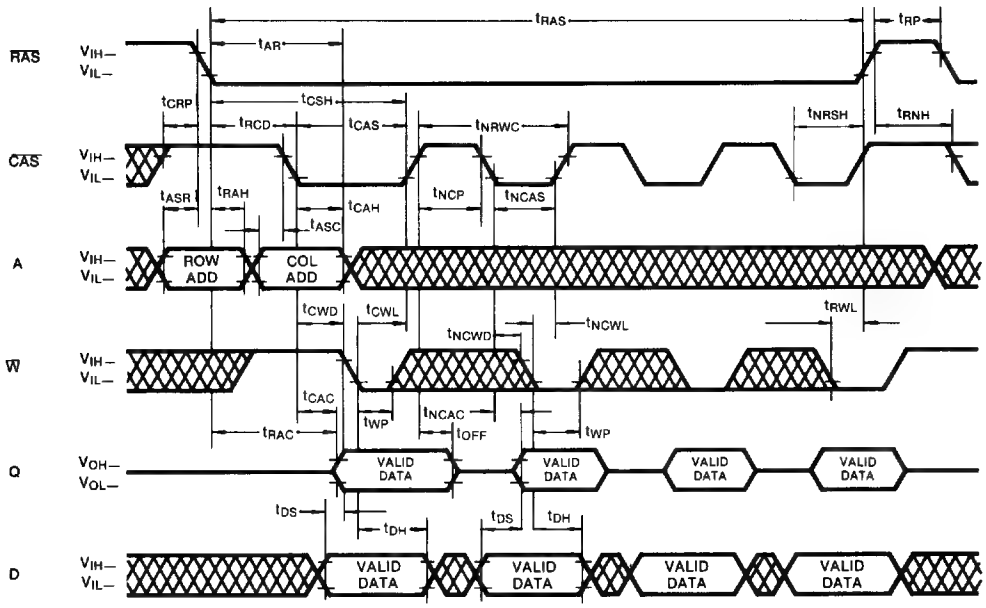


NIBBLE MODE WRITE CYCLE (KM41257A)



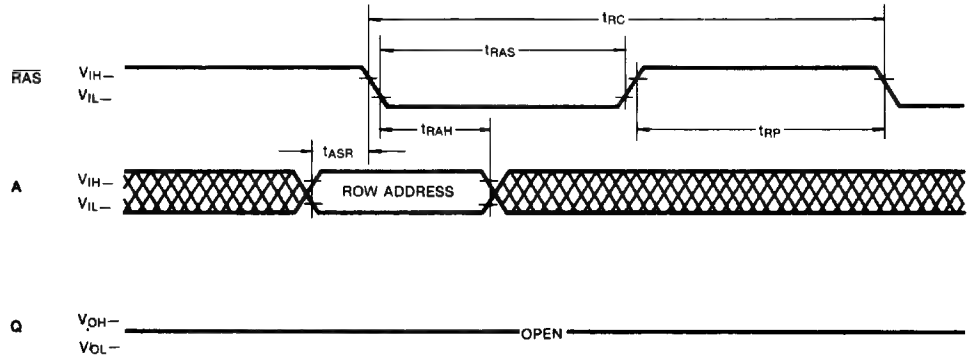
TIMING DIAGRAMS (Continued)

NIBBLE MODE READ-WRITE CYCLE (KM41257A)



RAS-ONLY REFRESH CYCLE

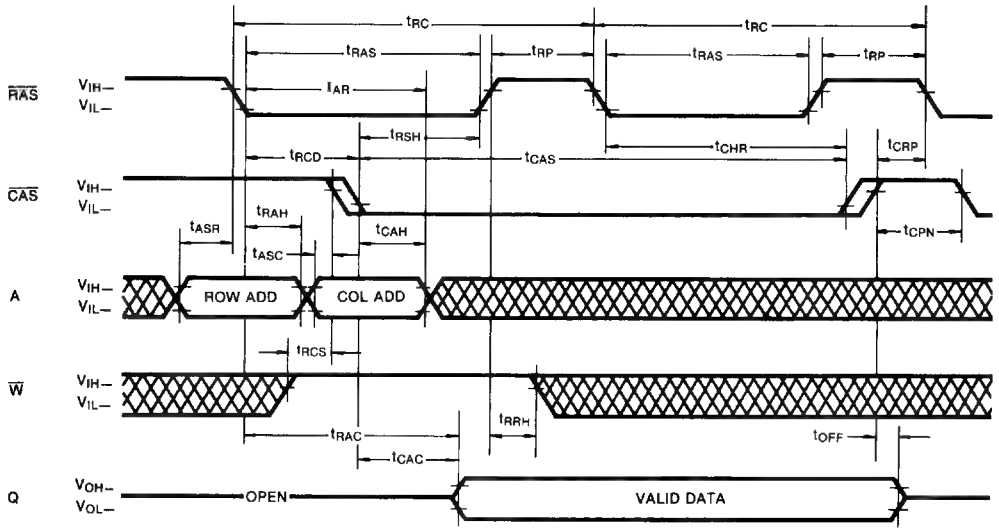
NOTE: $\overline{CAS}$ = V_{IH}, $\overline{W}$, D = Don't Care



DON'T CARE

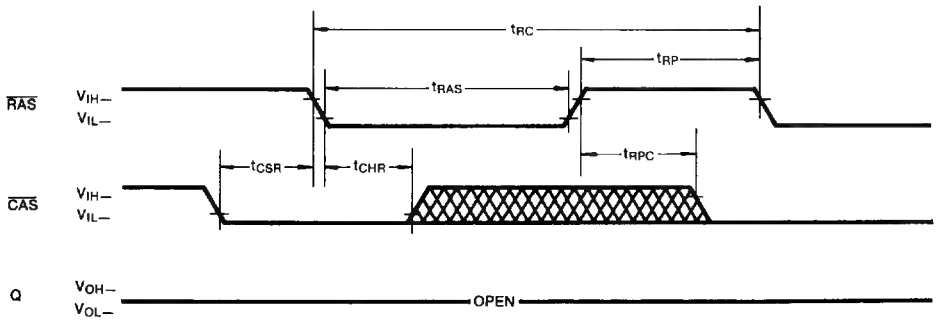
TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE



CAS-BEFORE-RAS REFRESH CYCLE

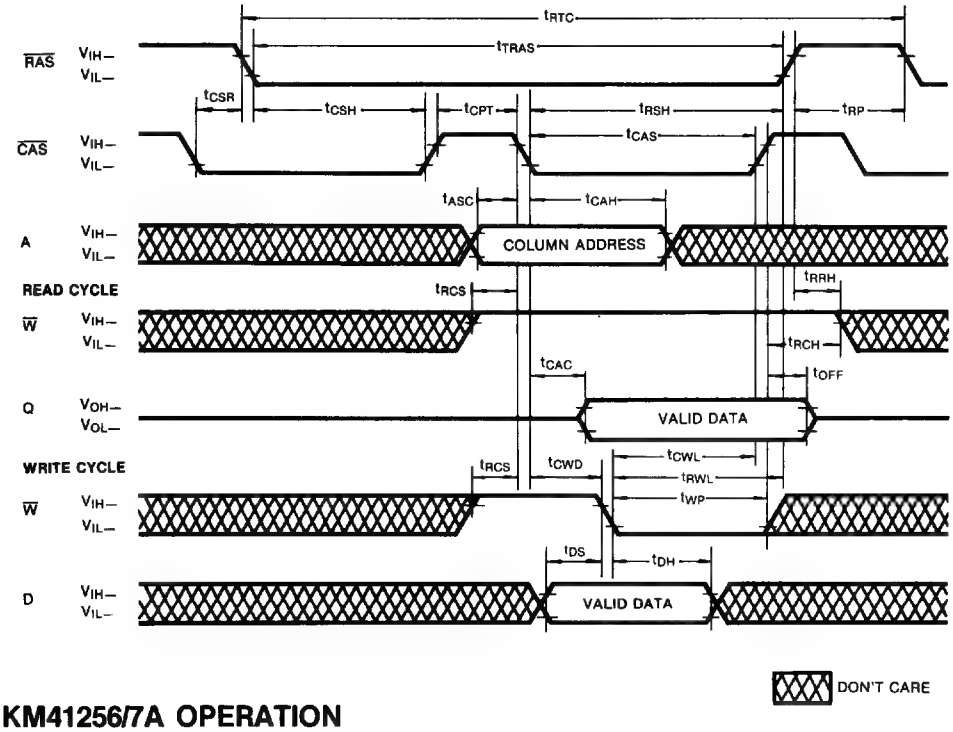
NOTE: Address, W, D = Don't Care



DON'T CARE

TIMING DIAGRAMS (Continued)

CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



KM41256/7A OPERATION

Device Operation

The KM41256/7A contains 262,144 memory locations. Eighteen address bits are required to address a particular memory location. Since the KM41256/7A has only 9 address input pins, time multiplexed addressing is used to input 9 row and 9 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{RAS}$), the column address strobe ($\overline{CAS}$) and the valid address inputs.

Operation of the KM41256/7A begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. Then the address on the 9 address input pins is changed from a row address to a column address and is strobed in by $\overline{CAS}$. This is the beginning of any KM41256/7A cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both $\overline{RAS}$ and $\overline{CAS}$ have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time (t_{RP}) requirement.

$\overline{RAS}$ and $\overline{CAS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CAS}$ pulse width are specified by t_{RAS}(min) and t_{CAS}(min) respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, t_{RP}, has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM41256/7A begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

DEVICE OPERATION (Continued)

Read

A read cycle is achieved by maintaining the write enable input ($\overline{W}$) high during a $\overline{RAS}$/$\overline{CAS}$ cycle. The output of the KM41256/7A remains in the Hi-Z state until valid data appears at the output. If $\overline{CAS}$ goes low before t_{RCD}(max), the access time to valid data is specified by t_{RAC}. If $\overline{CAS}$ goes low after t_{RCD}(max), the access time is measured from $\overline{CAS}$ and is specified by t_{CAC}. In order to achieve the minimum access time, t_{RAC}(min), it is necessary to bring $\overline{CAS}$ low before t_{RCD}(max).

Write

The KM41256/7A can perform early write, late write and read-modify-write cycles. The difference between these cycles is in the state of data-out and is determined by the timing relationship between $\overline{W}$ and $\overline{CAS}$. In any type of write cycle, Data-in must be valid at or before the falling edge of $\overline{W}$ or $\overline{CAS}$, whichever is later.

Early Write: An early write cycle is performed by bringing $\overline{W}$ low before $\overline{CAS}$. The data at the data input pin (D) is written into the addressed memory cell. Throughout the early write cycle the output remains in the Hi-Z state. This cycle is good for common I/O applications because the data-in and data-out pins may be tied together without bus contention.

Read-Modify-Write: In this cycle, valid data from the addressed cell appears at the output before and during the time that data is being written into the same cell location. This cycle is achieved by bringing $\overline{W}$ low after $\overline{CAS}$ and meeting the data sheet read-modify-write cycle timing requirements. This cycle requires using a separate I/O to avoid bus contention.

Late Write: If $\overline{W}$ is brought low after $\overline{CAS}$, a late write cycle will occur. The late write cycle is very similar to the read-modify-write cycle except that the timing parameters, t_{RWD} and t_{CWD}, are not necessarily met. The state of data-out is indeterminate since the output could be either Hi-Z or contain data depending on the timing conditions. This cycle requires a separate I/O to avoid bus contention.

Data Output

The KM41256/7A has a tri-state output buffer which is controlled by $\overline{CAS}$ (and $\overline{W}$ for early write).
Whenever $\overline{CAS}$ is high (V_{IH}), the output is in the high impedance (Hi-Z) state, In any cycle in which valid data appears at the output, the output first remains in the Hi-Z state until the data is valid and then the valid data appears at the output. The valid data remains at the output until $\overline{CAS}$ returns high. This is true even if a new $\overline{RAS}$ cycle occurs (as in hidden refresh). Each of the KM41256/7A operating cycles is listed below after the corresponding output state produced by the cycle.

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Page Mode Read, Page Mode Read-Modify-Write. Nibble Mode Read, Nibble Mode Read-Modify-Write.

Hi-Z Output State: Early Write, $\overline{RAS}$-only Refresh, Page Mode Write, Nibble Mode Write, $\overline{CAS}$-before-$\overline{RAS}$ Refresh, $\overline{CAS}$-only cycle.

Indeterminate Output State: Delayed Write

Refresh

The data in the KM41256/7A is stored on a tiny capacitor within each memory cell. Due to leakage, the data will leak off after a period of time. To maintain data integrity it is necessary to refresh each of the rows every 4 ms. There are several ways to accomplish this.

$\overline{RAS}$-Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{RAS}$ while $\overline{CAS}$ remains high.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh: The KM41256/7A has $\overline{CAS}$-before-$\overline{RAS}$ on-chip refreshing capability that eliminates the need for external refresh addressed. If $\overline{CAS}$ is held low for the specified set up time (t_{CSR}) before $\overline{RAS}$ goes low, the on-chip refresh circuitry is enabled. An internal refresh operation automatically occurs and the on-chip refresh address counter is internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the $\overline{CAS}$ active time and strobing in a refresh row address with $\overline{RAS}$. The KM41256/7A hidden refresh cycle is actually a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter. This eliminates the need for the external row address that is required in hidden refresh cycles by DRAMS that do not have $\overline{CAS}$-before-$\overline{RAS}$ refresh capability.

Other Refresh Methods: It is also possible to refresh the KM41256/7A by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in that row are automatically refreshed. There are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{RAS}$-only refresh is the preferred method.

DEVICE OPERATION (Continued)

Page Mode (KM41256A)

The KM41256A has page mode capability. Page mode memory cycles provide faster access and lower power dissipation than normal memory cycles. In page mode, it is possible to perform read, write or read-modify-write cycles. As long as the applicable timing requirements are observed it is possible to mix these cycles in any order. A page mode cycle begins with a normal cycle. While $\overline{RAS}$ is kept low to maintain the row address, $\overline{CAS}$ is cycled to strobe in additional column addresses. This eliminates the time required to set up and strobe sequential row addresses for the same page.

Nibble Mode (KM41257A)

The KM41257A has nibble mode capability. Nibble mode operation allows high speed serial read, write or read-modify-write access of 4 consecutive bits. The first of 4 bits is accessed in the usual manner. The remaining nibble bits are accessed by toggling $\overline{CAS}$ high then low while $\overline{RAS}$ remains low.

The 4 bits of data that may be accessed during nibble mode are determined by the lower 8 row address bits (RA_0-RA_7) and 8 column address bits (CA_0-CA_7). The two address bits, $RA_8$and CA_8, are used to select 1 of the 4 nibble bits for initial access. The remaining nibble bits are accessed by toggling $\overline{CAS}$ with $\overline{RAS}$ held low. Each high-low $\overline{CAS}$ transition will internally increment the nibble address (RA_8, CA_8) as shown in the following diagram.

If more than 4 bits are accessed during nibble mode, the address sequence will begin to repeat. If any bit is written during nibble mode, the new data will be read on any subsequent access. If the write operation is executed again on a subsequent access, the new data will be written into the selected cell location.

A nibble cycle can be a read, write, or read-modify-write cycle. Any combinations of reads and writes or read-modify-writes are allowed.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter test cycle

A special timing sequence using the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle provides a convenient method of verifying the functionality of the $\overline{CAS}$-before-$\overline{RAS}$ refresh activated circuitry.

After the $\overline{CAS}$-before-$\overline{RAS}$ refresh operation, if $\overline{CAS}$ goes high and then low again while $\overline{RAS}$ is held low, the read and write operations are enabled.

This is shown in the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle timing diagram. A memory cell can be addressed with 9 row address bits and 9 column address bits defined as follows:

Row Address—Bits A0 through A7 are supplied by the on-chip refresh counter. The A8 bit is set high internally.

Column Address—Bits A0 through A8 are strobed-in by the falling edge of $\overline{CAS}$ as in a normal memory cycle.

Suggested $\overline{CAS}$-before-$\overline{RAS}$ Counter Test Procedures

The $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle timing is used in each of the following steps:

1. Initialize the internal refresh counter by performing 8 cycles.
2. Write a test pattern of "lows" into the memory cells at a single column address and 256 row addresses. (The row addresses are supplied by the on-chip refresh counter.)
3. Using read-modify-write cycles, read the "lows" written during step 2 and write "highs" into the same memory locations. Perform this step 256 times so that highs are written into the 256 memory cells.
4. Read the "highs" written during step 3.
5. Compliment the test pattern and repeat steps 2, 3 and 4.

Power-up

If $\overline{RAS}$=V_{SS} during power-up the KM41256/7A might begin an active cycle. This condition results in higher than necessary current demands from the power supply during power-up. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{CC} during power-up or be held at a valid V_{IH} in order to minimize the power-up current.

An initial pause of 100μsec is required after power-up followed by 8 initialized cycles before proper device operation is assured. Eight initialization cycles are also required after any 4 msec period in which there are no $\overline{RAS}$ cycles. An initialization cycle is any cycle in which $\overline{RAS}$ is cycled.

Termination

The lines from the TTL driver circuits to the KM41256/7A inputs act like unterminated transmission lines resulting in significant positive and negative overshoots at the inputs. To minimize overshoot it is advisable to terminate the input lines and to keep them as short as possible. Although either series or parallel termination may be us-

DEVICE OPERATION (Continued)

ed, series termination is generally recommended since it is simple and draws no additional power. It consists of a resistor in series with the input line placed close to the KM41256/7A input pin. The optimum value depends on the board layout. It must be determined experimentally and is usually in the range of 20 to 40 ohms.

Board Layout

It is important to lay out the power and ground lines on memory boards in such a way that switching transient effects are minimized. The recommended methods are gridded power and ground lines or separate power and ground planes. The power and ground lines act like transmission lines to the high frequency transients generated by DRAMS. The impedance is minimized if all the power supply traces to all the DRAMS run both horizontally and vertically and are connected at each intersection or better yet if power and ground planes are used.

Address and control lines should be as short as possible to avoid skew. In boards with many DRAMS these lines should fan out from a central point like a fork or comb rather than being connected in a serpentine pattern. Also the control logic should be centrally located on large memory boards to facilitate the shortest possible address and control lines to all the DRAMS.

Decoupling

The importance of proper decoupling cannot be over emphasized. Excessive transient noise or voltage droop on the V_{CC} line can cause loss of data integrity (soft errors). The total combined voltage changes over time in the V_{CC} to V_{SS} voltage (measured at the device pins) should not exceed 500mV.

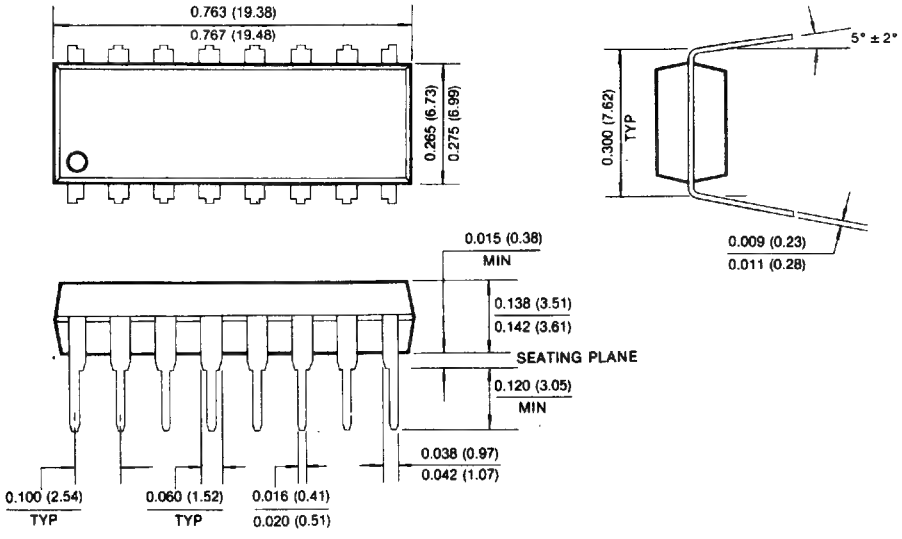
A high frequency 0.3μF ceramic decoupling capacitor should be connected between the V_{CC} and ground pins of each KM41256/7A using the shortest possible traces. These capacitors act as a low impedance shunt for the high frequency switching transients generated by the KM41256/7A and they supply much of the current used by the KM41256/7A during cycling.

In addition, a large tantalum capacitor with a value of 47μF to 100μF should be used for bulk decoupling to recharge the 0.3μF capacitors between cycles, thereby reducing power line droop. The bulk decoupling capacitor should be placed near the point where the power traces meet the power grid or power plane. Even better results may be achieved by distributing more than one tantalum capacitor throughout the memory array.

PACKAGE DIMENSIONS

16-LEAD PLASTIC DUAL IN-LINE PACKAGE

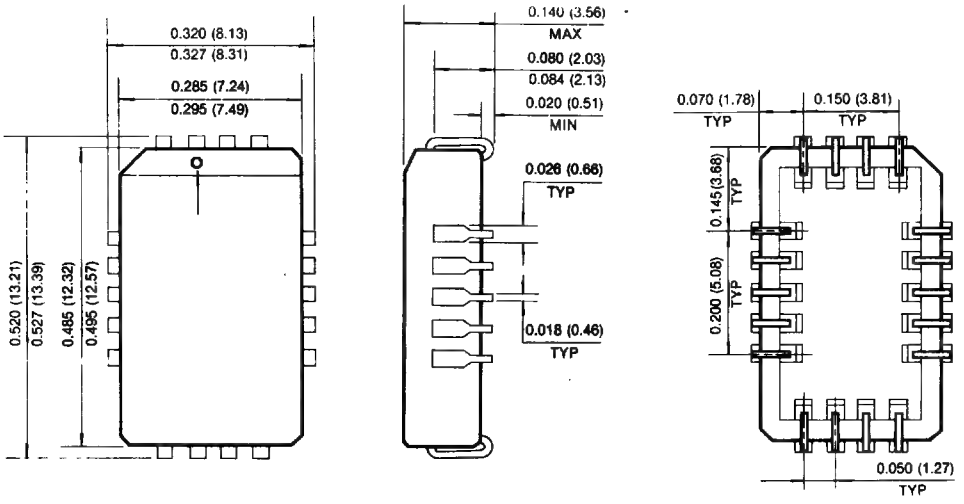
Units: Inches (millimeters)



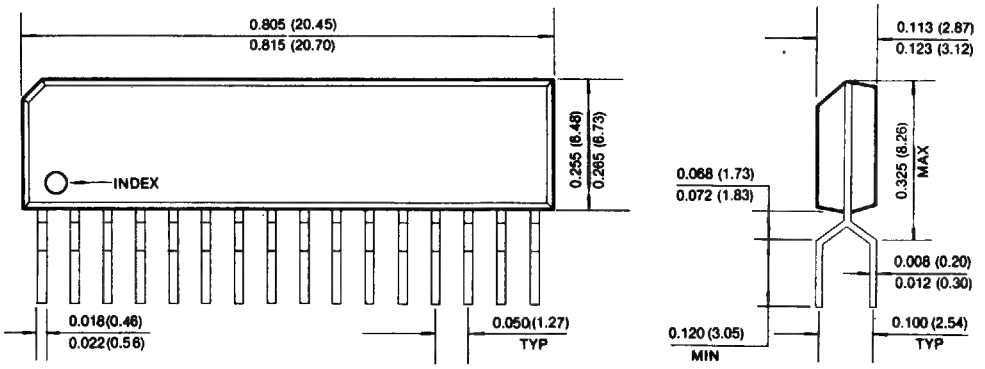
PACKAGE DIMENSIONS (Continued)

18- LEAD PLASTIC CHIP CARRIER

Units: Inches (millimeters)



16-LEAD PLASTIC ZIG-ZAG IN-LINE PACKAGE



64K x 4 Bit Dynamic RAM with Page Mode

FEATURES

- **Performance range**

	t_{RAC}	t_{CAC}	t_{RC}
KM41464A-10	100ns	50ns	190ns
KM41464A-12	120ns	60ns	220ns
KM41464A-15	150ns	75ns	260ns

- **Page Mode capability**
- **$\overline{CAS}$-before-$\overline{RAS}$ Refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **TTL compatible inputs and outputs**
- **Early Write or Output Enable Controlled Write**
- **Single +5V±10% power supply**
- **256 cycle/4ms refresh**
- **JEDEC standard pinout in 18-pin DIP, 18-lead PLCC and 20-pin ZIP.**

GENERAL DESCRIPTION

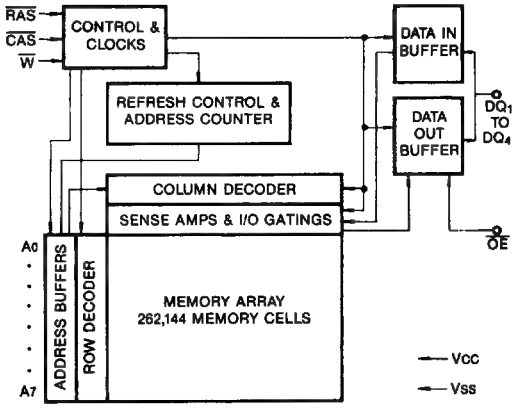
The KM41464A is a fully decoded 65,536 x 4 NMOS Dynamic Random Access Memory. The design is optimized for high speed, high performance applications such as computer memory, buffer memory, peripheral storage and environments where low power dissipation and compact layout are required.

The KM41464A features page mode which allows high speed random access of memory cells within the same row. $\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. Multiplexed row and column address inputs permit the KM41464A to be housed in a standard 18-pin DIP.

The KM41464A is fabricated using Samsung's advanced silicon gate NMOS process. This process, coupled with single transistor memory storage cells, permits maximum circuit density and minimal chip size.

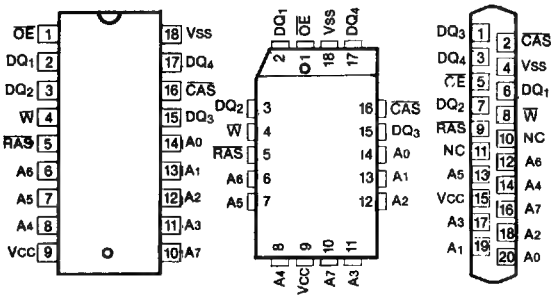
Clock timing requirements are noncritical, and power supply tolerance is very wide. All inputs and outputs are TTL complible.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION

- **KM41464AP**
- **KM41464AJ**
- **KM41464AZ**



Pin Name	Pin Function
A_0-A_7	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Output Enable
DQ_1-DQ_4	Data In/Out
V_{CC}	Power (+5V)
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Units
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7.0	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	−1 to +7.0	V
Storage Temperature	T_{stg}	−55 to +150	°C
Power Dissipation	P_D	1.0	W
Short Circuit Output Current	I_{OS}	50	mA

*Note: Permanent device damage may occur of ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS}, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC}+1	V
Input Low Voltage	V_{IL}	−1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Min	Max	Units
OPERATING CURRENT* ($\overline{RAS}$ and $\overline{CAS}$ cycling; @t_{RC} = min.)	KM41464A-12 KM41464A-15	I_{CC1}	— —	75 65	mA mA
STANDBY CURRENT ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH} after 8 $\overline{RAS}$ cycles min.)		I_{CC2}	—	4.5	mA
$\overline{RAS}$-ONLY REFRESH CURRENT* ($\overline{CAS}$ = V_{IH}, $\overline{RAS}$ cycling; @t_{RC} = min.)	KM41464A-12 KM41464A-15	I_{CC3}	— —	65 60	mA mA
PAGE MODE CURRENT* ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling; @t_{PC} = min.)	KM41464A-12 KM41464A-15	I_{CC4}	— —	55 45	mA mA
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CURRENT ($\overline{RAS}$ cycling; @t_{RC} = min.)	KM41464A-12 KM41464A-15	I_{CC5}	— —	65 60	mA mA
INPUT LEAKAGE CURRENT (Any input $0 \le V_{IN} \le 5.5V$, V_{CC} = 5.5V, V_{SS} = 0V, all other pins not under test = 0 volts.)		I_{IL}	−10	10	μA
OUTPUT LEAKAGE CURRENT (Data out is disabled, $0V \le V_{OUT} \le 5.5V$		I_{DOL}	−10	10	μA
OUTPUT HIGH VOLTAGE LEVEL (I_{OH} = −5mA)		V_{OH}	2.4	—	V
OUTPUT LOW VOLTAGE LEVEL (I_{OL} = 4.2mA)		V_{OL}	—	0.4	V

*Note: I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current.

CAPACITANCE ($T_A = 25°C$)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A_0-A_7)	C_{IN1}	—	7	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{OE}$)	C_{IN2}	—	10	pF
Output Capacitance (DQ_1-DQ_4)	C_{DQ}	—	7	pF

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC} = 5.0V \pm 10\%$. See notes 1,2)

KM41464A STANDARD OPERATION

Parameter	Symbol	KM41464A-12		KM41464A-15		Unit	Notes
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	220		260		ns	
Read-modify-write cycle time	t_{RWC}	305		355		ns	
Access time from $\overline{RAS}$	t_{RAC}		120		150	ns	3, 4
Access time from $\overline{CAS}$	t_{CAC}		60		75	ns	3, 5
Output buffer turn-off delay time	t_{OFF}	0	30	0	40	ns	6
Transition time (rise and fall)	t_T	3	50	3	50	ns	
$\overline{RAS}$ precharge time	t_{RP}	90		100		ns	
$\overline{RAS}$ pulse width	t_{RAS}	120	10,000	150	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	60		65		ns	
$\overline{CAS}$ precharge time (all cycles except page mode)	t_{CPN}	30		35		ns	
$\overline{CAS}$ pulse width	t_{CAS}	60	10,000	75	10,000	ns	
$\overline{CAS}$ hold time	t_{CSH}	120		150		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	25	60	25	75	ns	4
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		ns	
Row address set-up time	t_{ASR}	0		0		ns	
Row address hold time	t_{RAH}	15		15		ns	
Column address set-up time	t_{ASC}	0		0		ns	
Column address hold time	t_{CAH}	20		25		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	80		100		ns	
Read command set-up time	t_{RCS}	0		0		ns	
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	20		20		ns	
Write command set-up time	t_{WCS}	0		0		ns	7
Write command hold time	t_{WCH}	40		45		ns	
Write command pulse width	t_{WP}	40		45		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	40		45		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	40		45		ns	

KM41464A STANDARD OPERATION (Continued)

Parameter	Symbol	KM41464A-12		KM41464A-15		Units	Notes
		Min	Max	Min	Max		
Data-in set-up time	t_{DS}	0		0		ns	
Data-in hold time	t_{DH}	40		45		ns	
$\overline{CAS}$ to write enable delay time	t_{CWD}	100		120		ns	7
$\overline{RAS}$ to write enable delay time	t_{RWD}	160		195		ns	7
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	100		120		ns	
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	100		120		ns	
Access time from $\overline{OE}$	t_{OEA}		30		40	ns	
$\overline{OE}$ to Data in delay time	t_{OED}	30		40		ns	
Output Buffer turn off delay from $\overline{OE}$	t_{OEZ}	0	30	0	40	ns	
$\overline{OE}$ hold time referenced to $\overline{W}$	t_{OEH}	25		25		ns	
$\overline{OE}$ to $\overline{RAS}$ inactive setup time	t_{OES}	0		0		ns	
Din to $\overline{CAS}$ delay time	t_{DZC}	0		0		ns	8
Din to $\overline{OE}$ delay time	t_{DZO}	0		0		ns	8
Refresh period (256 cycles)	t_{REF}		4		4	ms	

KM41464A $\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH

$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ Refresh)	t_{CSR}	25		30		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ Refresh)	t_{CHR}	55		60		ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{PRC}	20		20		ns	

KM41464A PAGE MODE

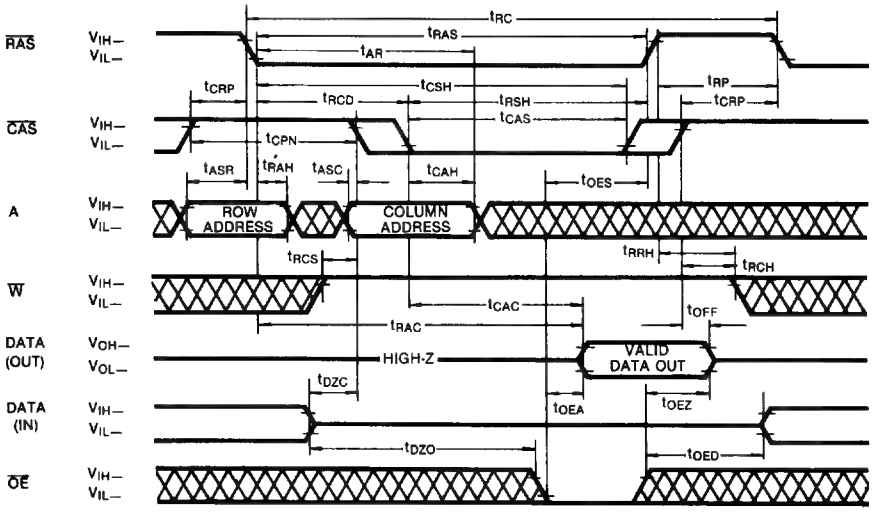
Page mode cycle time	t_{PC}	120		145		ns	
$\overline{CAS}$ precharge time (page mode only)	t_{CP}	50		60		ns	

NOTES

1. An initial pause of 100μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$(max).
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
7. t_{CWD} and t_{RWD} are restrictive operating parameters for the read-modify-write cycle only. If $t_{WCS} \geq t_{WCS}$(min), the cycle is an early write cycle and the data output will remain open circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$(min) and $t_{RWD} > t_{RWD}$(min), the cycle is a late write cycle and the data output will contain data read from the selected cell. If neither of the above conditions are met, the condition of the data out (at access time until $\overline{CAS}$ goes back to V_{IH}) is indeterminate.
8. Either t_{DZC} or t_{DZO} must be satisfied for all cycles.

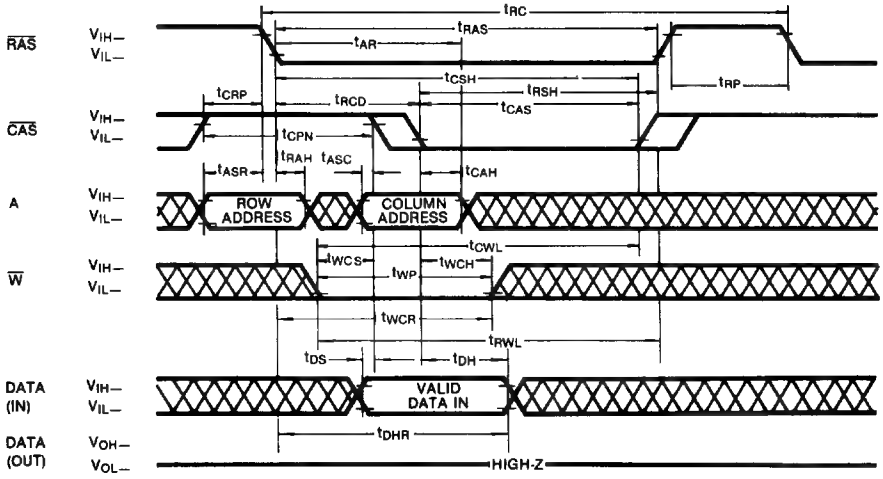
TIMING DIAGRAMS

READ CYCLE



WRITE CYCLE (EARLY WRITE)

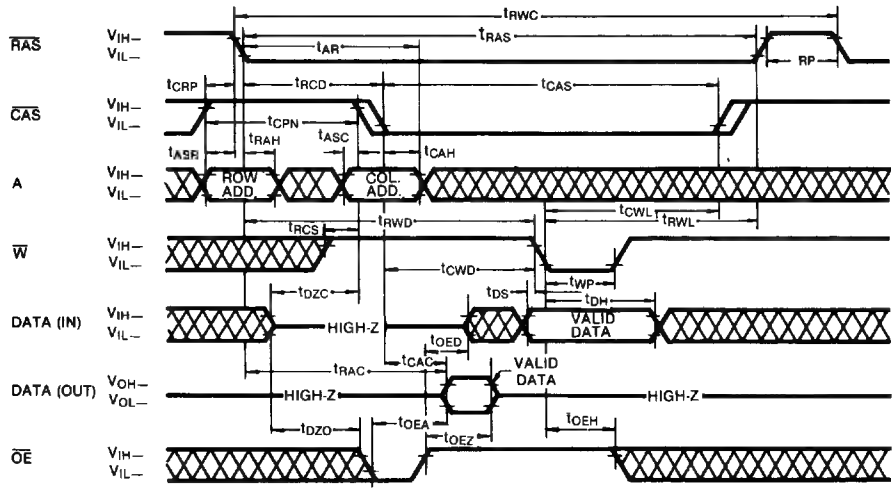
$\overline{OE}$ = Don't Care



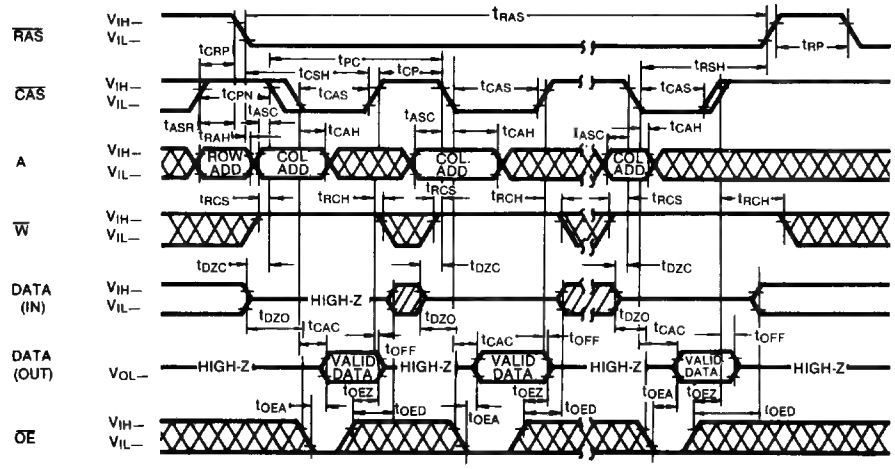
DON'T CARE

TIMING DIAGRAMS (Continued)

READ-WRITE/READ-MODIFY-WRITE CYCLE



PAGE MODE READ CYCLE

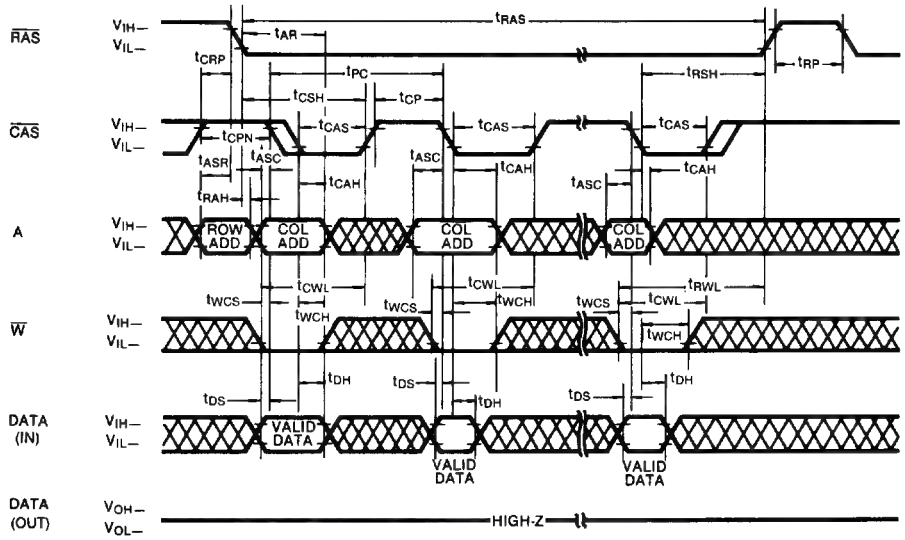


DON'T CARE

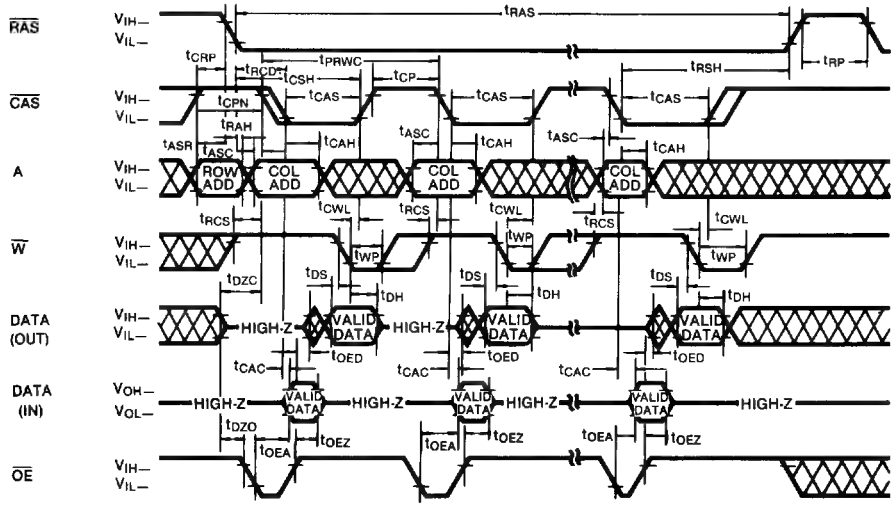
TIMING DIAGRAMS (Continued)

PAGE MODE WRITE CYCLE

$\overline{OE}$ = Don't Care



PAGE MODE READ-MODIFY-WRITE CYCLE

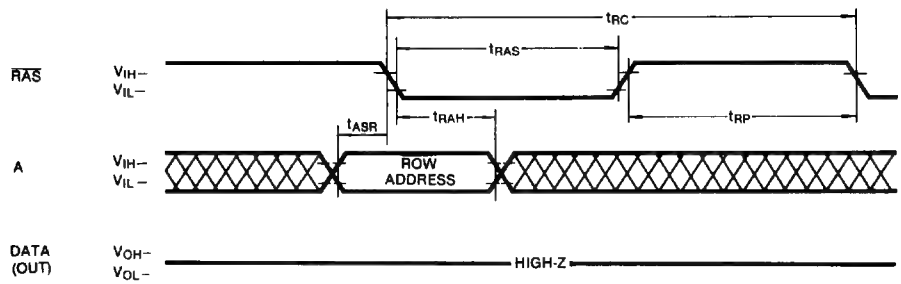


DON'T CARE

TIMING DIAGRAMS (Continued)

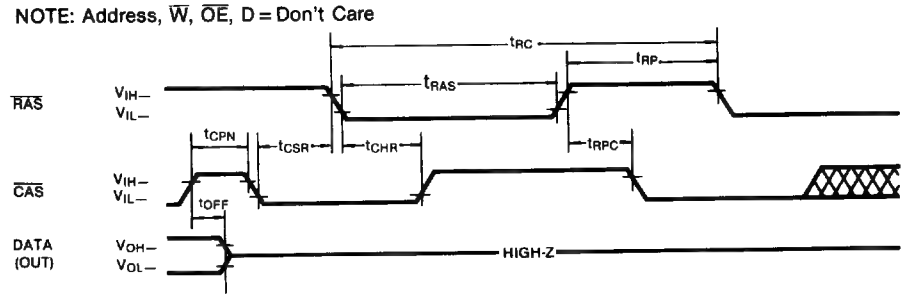
$\overline{RAS}$-ONLY REFRESH CYCLE

NOTE: $\overline{CAS} = V_{IH}$; $\overline{W}$, $\overline{OE}$, D = Don't Care

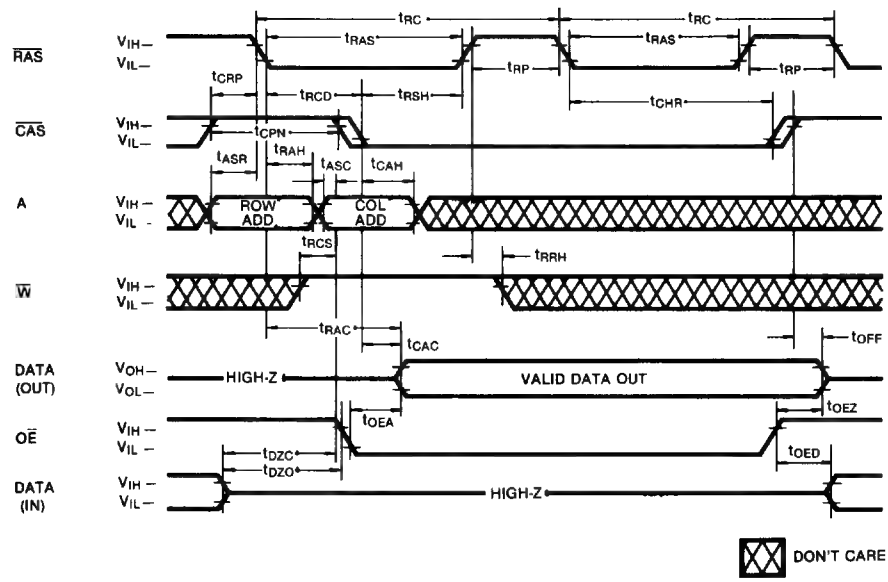


$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

NOTE: Address, $\overline{W}$, $\overline{OE}$, D = Don't Care



HIDDEN REFRESH CYCLE



KM41464A OPERATION

Device Operation

The KM41464A contains 262,144 memory locations organized as 65,536 × 4-bit words. Sixteen address bits are required to address a particular 4-bit word in the memory array. Since the KM41464A has only 8 address input pins, time multiplexed addressing is used to input 8 row and 8 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{RAS}$), the column address strobe ($\overline{CAS}$) and the valid address inputs.

Operation of the KM41464A begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. Then the address on the 8 address input pins is changed from a row address to a column address and is strobed in by $\overline{CAS}$. This is the beginning of any KM41464A cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both $\overline{RAS}$ and $\overline{CAS}$ have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time (t_{RP}) requirement.

$\overline{RAS}$ and $\overline{CAS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CAS}$ pulse width are specified by t_{RAS}(min) and t_{CAS}(min) respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, t_{RP}, has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM41464A begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input ($\overline{W}$) high during a $\overline{RAS}$/$\overline{CAS}$ cycle. The four outputs of the KM41464A remains in the Hi-Z state until valid data appears at the output. The KM41464A has common data I/O pins. For this reason an output enable control input ($\overline{OE}$) has been provided so the output buffer can be precisely controlled. For data to appear at the outputs, $\overline{OE}$ must be low for the period of time defined by t_{OEA} and t_{OEZ}. If $\overline{CAS}$ goes low before t_{RCD}(max), the access time to valid data is specified by t_{RAC}. If $\overline{CAS}$ goes low after t_{RCD}(max), the access time is measured from $\overline{CAS}$ and is specified by t_{CAC}. In order to achieve the minimum access time, t_{RAC}(min), it is necessary to bring $\overline{CAS}$ low before t_{RCD}(max).

Write

The KM41464A can perform early write, and read-modify-write cycles. The difference between these cycles is in the state of data-out and is determined by the timing relationship between $\overline{W}$, $\overline{OE}$ and $\overline{CAS}$. In any type of write cycle, Data-in must be valid at or before the falling edge of $\overline{W}$ or $\overline{CAS}$, whichever is later.

Early Write: An early write cycle is performed by bringing $\overline{W}$ low before $\overline{CAS}$. The 4-bit wide data at the data input pins is written into the addressed memory cells. Throughout the early write cycle the outputs remain in the Hi-Z state regardless of the state of the $\overline{OE}$ input.

Read-Modify-Write: In this cycle, valid data from the addressed cell appears at the outputs before and during the time that data is being written into the same cell locations. This cycle is achieved by bringing $\overline{W}$ low after $\overline{CAS}$ and meeting the data sheet read-modify-write timing requirements. The output enable input ($\overline{OE}$) must be low during the time defined by t_{OEA} and t_{OEZ} for data to appear at the outputs. If t_{CWD} and t_{RWD} are not met the output may contain invalid data. Conforming to the $\overline{OE}$ timing requirements prevents bus contention on the KM41464's DQ pins.

Data Output

The KM41464A has tri-state output buffers which are controlled by $\overline{CAS}$ and OE. When either $\overline{CAS}$ or $\overline{OE}$ is high (V_{IH}), the output are in the high impedance (Hi-Z) state. In any cycle in which valid data appears at the outputs, the outputs first remains in the Hi-Z state until the data is valid and then the valid data appears at the outputs. The valid data remains at the outputs until $\overline{CAS}$ or $\overline{OE}$ returns high. This is true even if a new $\overline{RAS}$ cycle occurs (as in hidden refresh). Each of the KM41464A operating cycles are listed below after the corresponding output state produced by the cycle.

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Page Mode Read, Page Mode Read-Modify-Write.

Hi-Z Output State: Early Write, $\overline{RAS}$-only Refresh, Page Mode write, $\overline{CAS}$-only cycle.

Indeterminate Output State: Delayed Write (t_{CWD} or t_{RWD} are not met)

Refresh

The data in the KM41464A is stored on a tiny capacitor within each memory cell. Due to leakage, the data will leak off after a period of time. To maintain data integrity it is necessary to refresh each of the rows every 4 ms. There are several ways to accomplish this.

$\overline{RAS}$-Only Refresh: This is the most common method

KM41464A OPERATION (Continued)

for performing refresh. It is performed by strobing in a row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. This must be performed on each of the 256 row addresses (A_0-A_7) every 4ms.

$\overline{CAS}$-Before-$\overline{RAS}$ Refresh: The KM41464A has $\overline{CAS}$-before-$\overline{RAS}$ on-chip refreshing capability that eliminates the need for external refresh addresses. If $\overline{CAS}$ is held low for the specified set up time (t_{CSR}) before $\overline{RAS}$ goes low, the on-chip refresh circuitry is enabled. An internal refresh operation automatically occurs and the on-chip refresh address counter is internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the $\overline{CAS}$ active time and cycling $\overline{RAS}$. The KM41464A hidden refresh cycle is actually a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter. This eliminates the need for the external row address that is required in hidden refresh cycles by DRAMS that do not have $\overline{CAS}$-before-$\overline{RAS}$ refresh capability.

Other Refresh Methods: It is also possible to refresh the KM41464A by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in that row are automatically refreshed. There are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh are the preferred methods.

Page Mode

Page mode memory cycles provide faster access and lower power dissipaton than normal memory cycles. In page mode, it is possible to perform read, write or read-modify-write cycles. As long as the applicable timing requirements are observed, it is possible to mix these cycles in any order. A page mode cycle begins with a normal cycle. While $\overline{RAS}$ is kept low to maintain the row address, $\overline{CAS}$ is cycled to strobe in additional column addresses. This eliminates the time required to set up and strobe sequential row addresses for the same page.

Power-up

If $\overline{RAS}$=V_{SS} during power-up the KM41464A might begin an active cycle. This condition results in higher than necessary current demands from the power supply during power-up. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{CC} during power-up or be held at a valid V_{IH} in order to minimize the power-up current.

An initial pause of 100μsec is required after power-up followed by 8 initialization cycles before proper device operation is assured. Eight initialization cycles are also required after any 4 msec period in which there are no $\overline{RAS}$ cycles. An initialization cycle is any cycle in which $\overline{RAS}$ is cycled.

Termination

The lines from the TTL driver circuits to the KM41464A inputs act like unterminated transmission lines resulting in significant positive and negative overshoots at the inputs. To minimize overshoot it is advisable to terminate the input lines and to keep them as short as possible. Although either series or parallel termination may be used, series termination is generally recommended since it is simple and draws no additional power. It consists of a resistor in series with the input line placed close to the KM41464A input pin. The optimum value depends on the board layout. It must be determined experimentally and is usually in the range of 20 to 40 ohms.

Board Layout

It is important to lay out the power and ground lines on memory boards in such a way that switching transient effects are minimized. The recommended methods are gridded power and ground lines or separate power and ground planes. The power and ground lines act like transmission lines to the high frequency transients generated by DRAMS. The impedance is minimized if all the power supply traces to all the DRAMS run both horizontally and vertically and are connected at each intersection or better yet if power and ground planes are used.

Address and control lines should be as short as possible to avoid skew. In boards with many DRAMS these lines should fan out from a central point like a fork or comb rather than being connected in a serpentine pattern. Also the control logic should be centrally located on large memory boards to facilitate the shortest possible address and control lines to all the DRAMs.

Decoupling

The importance of proper decoupling cannot be over emphasized. Excessive transient noise or voltage droop on the V_{CC} line can cause loss of data integrity (soft errors). The total combined voltage changes over time in the V_{CC} to V_{SS} voltage (measured at the device pins) should not exceed 500mV.

A high frequency 0.3μF ceramic decoupling capacitor should be connected between the V_{CC} and ground pins of each KM41464A using the shortest possible traces.

KM41464A OPERATION (Continued)

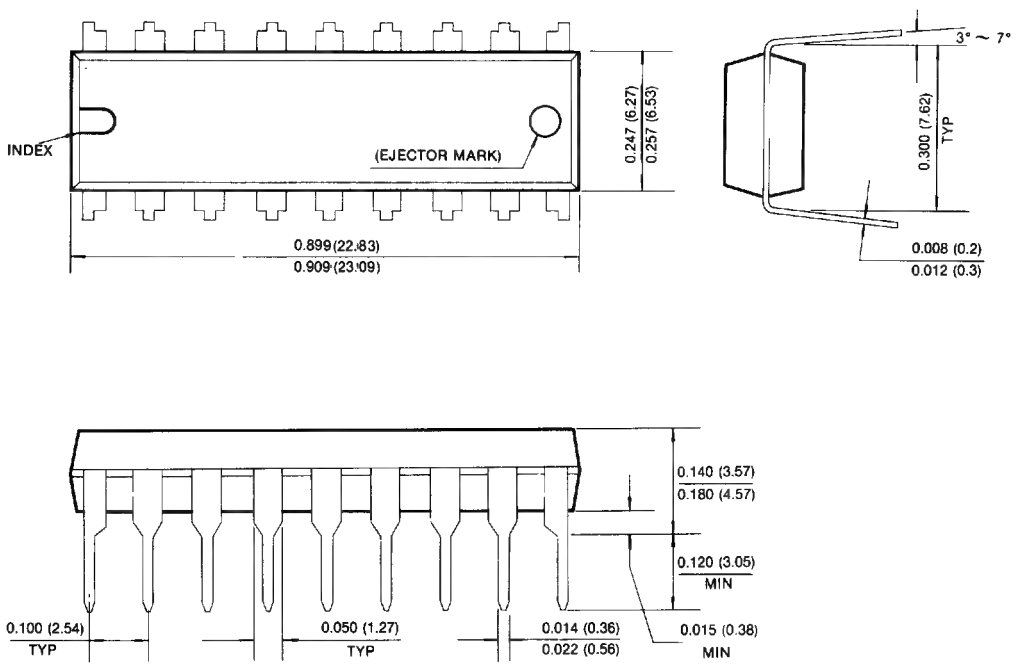
These capacitors act as a low impedance shunt for the high frequency switching transients generated by the KM41464A and they supply much of the current used by the KM41464A during cycling.

In addition, a large tantalum capacitor with a value of 47μF to 100μF should be used for bulk decoupling to recharge the 0.3μF capacitors between cycles, thereby reducing power line droop. The bulk decoupling capacitor should be placed near the point where the power traces meet the power grid or power plane. Even better results may be achieved by distributing more than one tantalum capacitor around the memory array.

PACKAGE DIMENSIONS

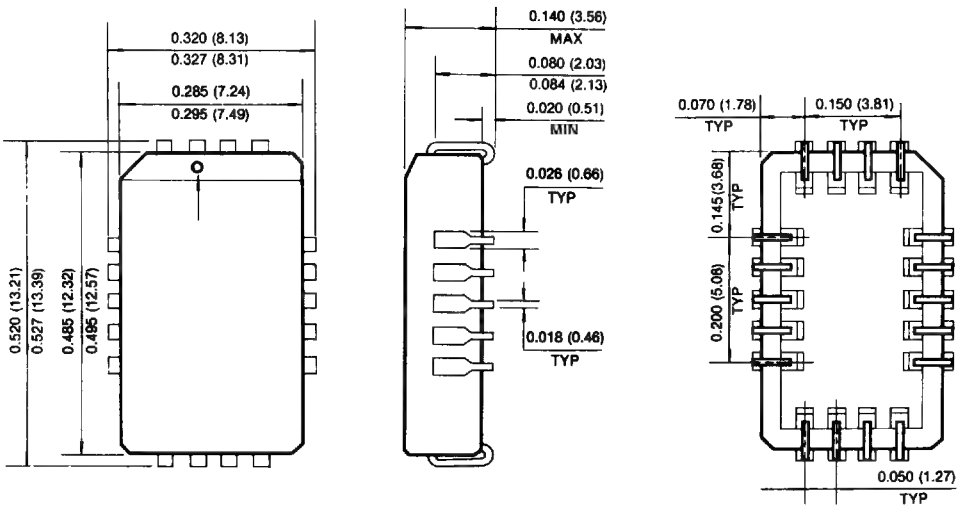
18-LEAD PLASTIC DUAL IN-LINE PACKAGE

Units: Inches (millimeters)

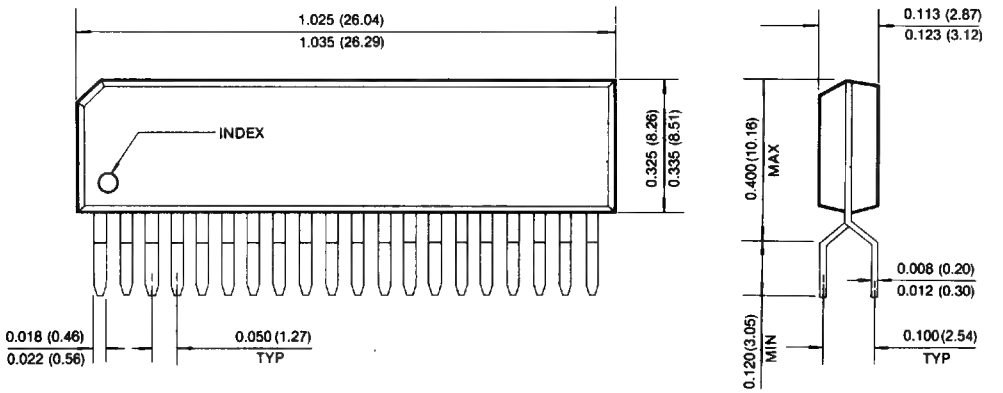


PACKAGE DIMENSIONS (Continued)

18-PIN PLASTIC LEADED CHIP CARRIER



20-PIN PLASTIC ZIGZAG-IN-LINE PACKAGE



1M x 1 Bit Dynamic RAM with Fast Page Mode

FEATURES

- **Performance range:**

	t_{RAC}	t_{CAC}	t_{RC}
KM41C1000A- 7	70ns	20ns	130ns
KM41C1000A- 8	80ns	20ns	150ns
KM41C1000A-10	100ns	25ns	180ns

- **Fast Page Mode operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **TTL compatible inputs and output**
- **Common I/O using early write**
- **Single +5V ± 10% power supply**
- **512 cycle/8ms refresh**
- **256K x 4 fast test mode**
- **JEDEC standard pinout available in Plastic DIP, SOJ, ZIP packages.**

GENERAL DESCRIPTION

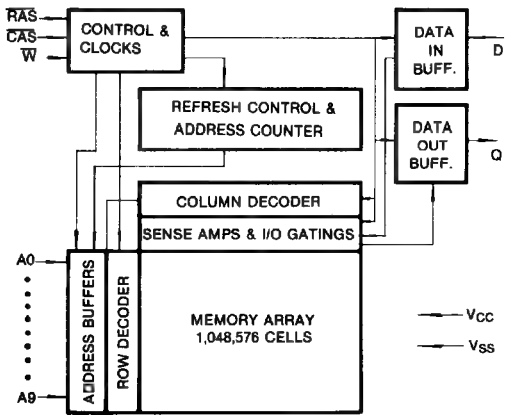
The Samsung KM41C1000A is a CMOS high speed 1,048,576 x 1 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes and mini computers, graphics and high performance microprocessor systems.

The KM41C1000A features Fast Page Mode operation which allows high speed random access of memory cells within the same row.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only Refresh. All inputs and output are fully TTL compatible.

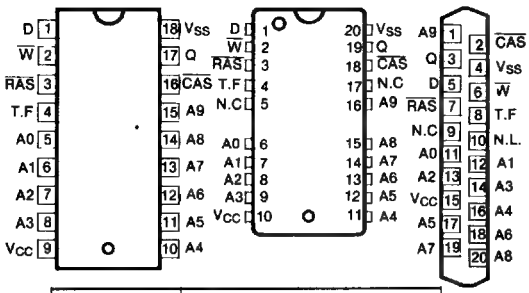
The KM41C1000A is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION

- **KM41C1000AP** • **KM41C1000AJ** • **KM41C1000AZ**



Pin Name	Pin Function
A_0-A_9	Address Inputs
$\overline{RAS}$	Row Address Strobe
D	Data In
Q	Data Out
$\overline{CAS}$	Column Address Strobe
$\overline{W}$	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground
T.F.	Test Function
N.C.	No Connection
N.L.	No Lead

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Units
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7.0	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	−1 to +7.0	V
Storage Temperature	T_{stg}	−55 to +150	°C
Power Dissipation	P_D	0.6	W
Short Circuit Output Current	I_{OS}	50	mA

*Note: Permanent device damage may occur of "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS}, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC} + 1	V
Input Low Voltage	V_{IL}	−1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Min	Max	Units
OPERATING CURRENT* ($\overline{RAS}$, $\overline{CAS}$, Address cycling @t_{RC} = min.)	KM41C1000A-7 KM41C1000A-8 KM41C1000A-10	I_{CC1}	—	80 70 60	mA
STANDBY CURRENT ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		I_{CC2}	—	2	mA
$\overline{RAS}$-ONLY REFRESH CURRENT* ($\overline{CAS}$ = V_{IH}, $\overline{RAS}$ cycling @t_{RC} = min.)	KM41C1000A-7 KM41C1000A-8 KM41C1000A-10	I_{CC3}	—	80 70 60	mA
FAST PAGE MODE CURRENT* ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling; @t_{PC} = min.)	KM41C1000A-7 KM41C1000A-8 KM41C1000A-10	I_{CC4}	—	60 50 40	mA
STANDBY CURRENT ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} − 0.2V)		I_{CC5}	—	1	mA
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CURRENT* ($\overline{RAS}$ and $\overline{CAS}$ cycling @t_{RC} = min.)	KM41C1000A-7 KM41C1000A-8 KM41C1000A-10	I_{CC6}	—	80 70 60	mA
INPUT LEAKAGE CURRENT (Any input 0 ≤ V_{IN} ≤ 6.5V, all other pins not under test = 0 volts.)		I_{IL}	−10	10	μA
OUTPUT LEAKAGE CURRENT (Data out is disabled, 0V ≤ V_{OUT} ≤ 5.5V		I_{OL}	−10	10	μA
OUTPUT HIGH VOLTAGE LEVEL (I_{OH} = −5mA)		V_{OH}	2.4	—	V
OUTPUT LOW VOLTAGE LEVEL (I_{OL} = 4.2mA)		V_{OL}	—	0.4	V

*Note: I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current.

CAPACITANCE ($T_A = 25°C$)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (D)	C_{IN1}	—	5	pF
Input Capacitance ($A_0 - A_9$)	C_{IN2}	—	6	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{W}$)	C_{IN3}	—	7	pF
Output Capacitance (Q)	C_{OUT}	—	7	pF

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC} = 5.0V \pm 10\%$. See notes 1,2)

STANDARD OPERATION

Parameter	Symbol	KM41C1000A-7		KM41C1000A-8		KM41C1000A-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	130		150		180		ns	
Read-modify-write cycle time	t_{RWC}	155		175		210		ns	
Access time from $\overline{RAS}$	t_{RAC}		70		80		100	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		20		20		25	ns	3,4,5
Access time from column address	t_{AA}		35		40		50	ns	3,10
Access time from $\overline{CAS}$ precharge	t_{CPA}		40		45		55	ns	3
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	5		5		5		ns	3
Output buffer turn-off delay	t_{OFF}	0	25	0	25	0	30	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	50		60		70		ns	
$\overline{RAS}$ pulse width	t_{RAS}	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		20		25		ns	
$\overline{CAS}$ hold time	t_{CSH}	70		80		100		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	20	10,000	25	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	50	25	60	25	75	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	35	20	40	20	50	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		15		15		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		20		20		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	55		65		75		ns	6
Column address to $\overline{RAS}$ lead time	t_{RAL}	35		40		50		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	9

STANDARD OPERATION (Continued)

Parameter	Symbol	KM41C1000A-7		KM41C1000A-8		KM41C1000A-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	9
Write command hold time	t_{WCH}	15		15		20		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	55		60		75		ns	6
Write command pulse width	t_{WP}	15		15		20		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		20		25		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	20		20		25		ns	
Data-in set-up time	t_{DS}	0		0		0		ns	10
Data-in hold time	t_{DH}	15		20		20		ns	10
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	55		65		75		ns	6
Refresh period (512 cycles)	t_{REF}		8		8		8	ms	
Write command set-up time	t_{WCS}	0		0		0		ns	8
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	20		20		25		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	70		80		100		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	35		40		50		ns	8

FAST PAGE MODE

Fast page mode cycle time	t_{PC}	45		50		60		ns	
$\overline{CAS}$ precharge time (Fast page mode)	t_{CP}	10		10		10		ns	
Fast page mode read-modify-write cycle time	t_{PRWC}	70		75		90		ns	
$\overline{RAS}$ pulse width (Fast page mode)	t_{RASP}	70	100,000	80	100,000	100	100,000	ns	

$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH

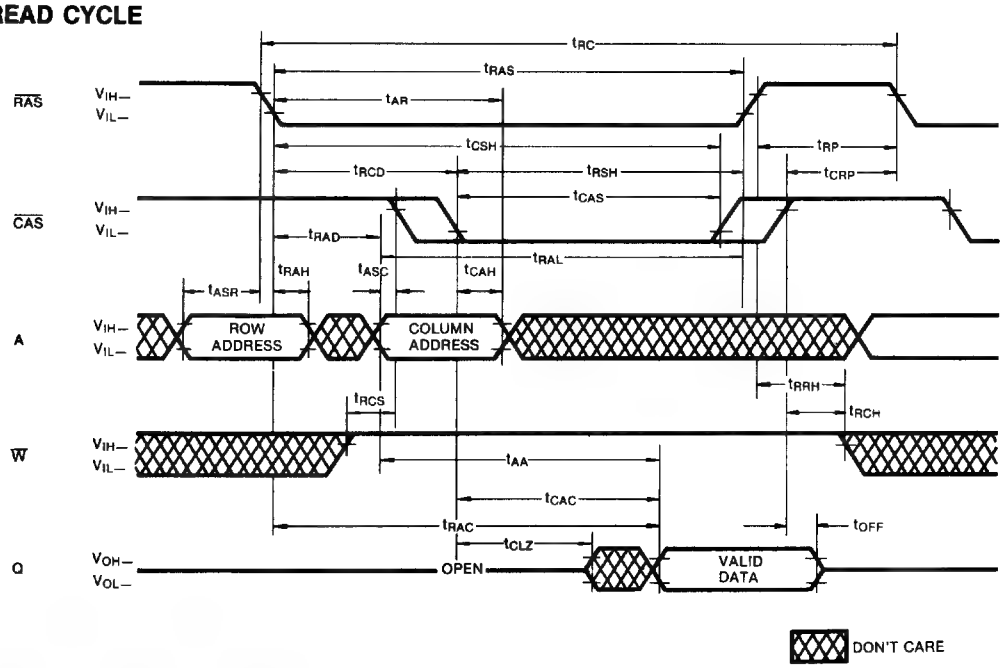
$\overline{CAS}$ setup time	t_{CSR}	10		10		10		ns	
$\overline{CAS}$ hold time	t_{CHR}	20		25		30		ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	10		10		10		ns	
Refresh couner test $\overline{CAS}$ precharge time	t_{CPT}	35		40		50		ns	

NOTES

1. An initial pause of 200μs is required after power up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max), and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$(max).
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to t_{RAD}(max).
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data output will remain open circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$(min) and $t_{RWD} \geq t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$ (min), then the cycle is a read-write cycle and the data output will contain data read from the selected cell. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the t_{RAD} (max) limit insures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled by t_{AA}.
12. Normal operation requires the "T.F" pin to be connected to V_{SS} or TTL logic low level or left unconnected on the printed wiring board.
13. When the "T.F" pin is connected to a defined positive voltage, the internal test function may be activated. Contact Samsung for specific operational details of the "test function."

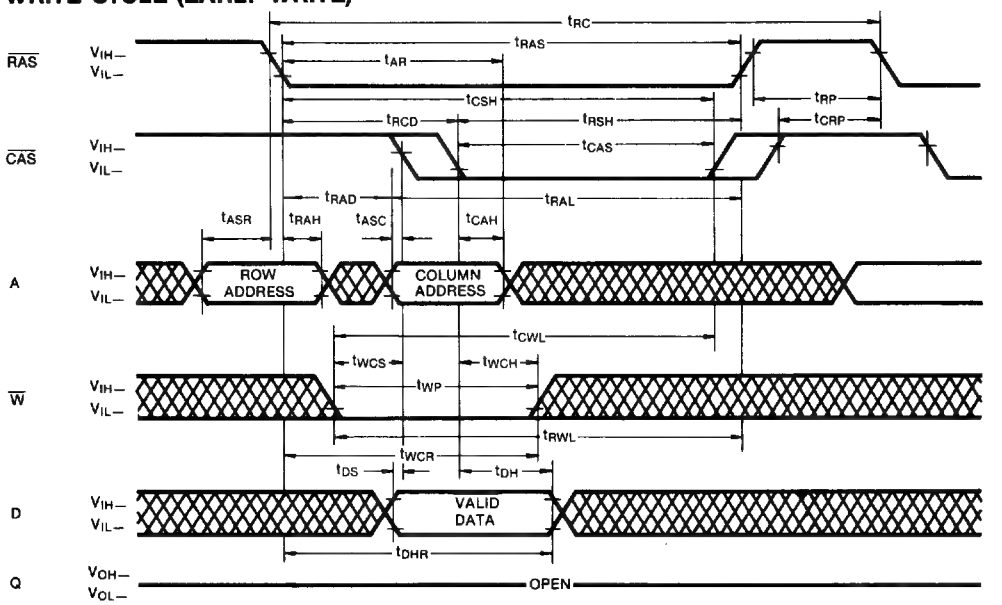
TIMING DIAGRAMS

READ CYCLE

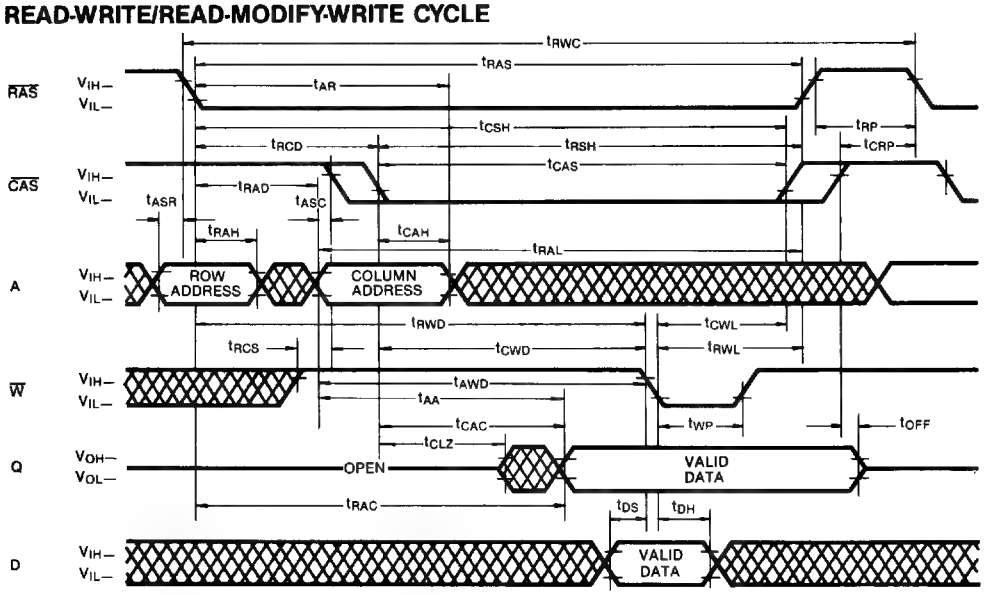


TIMING DIAGRAMS (Continued)

WRITE CYCLE (EARLY WRITE)



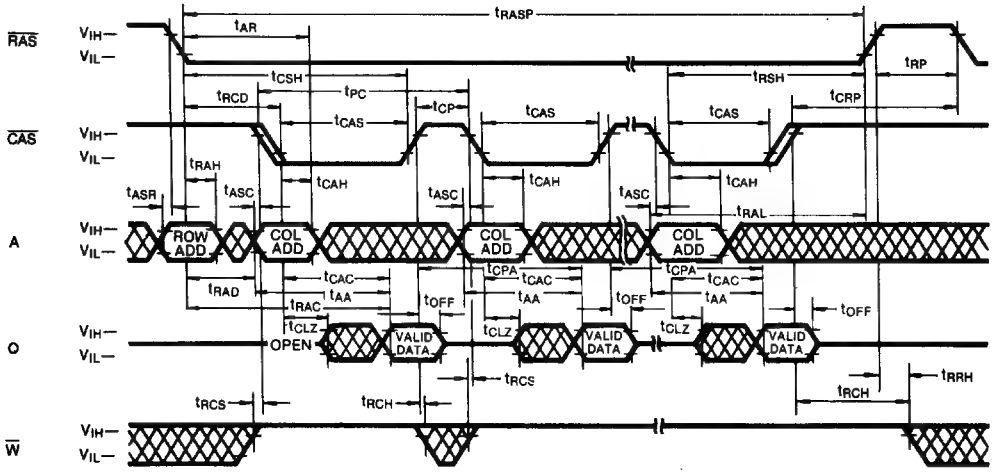
READ-WRITE/READ-MODIFY-WRITE CYCLE



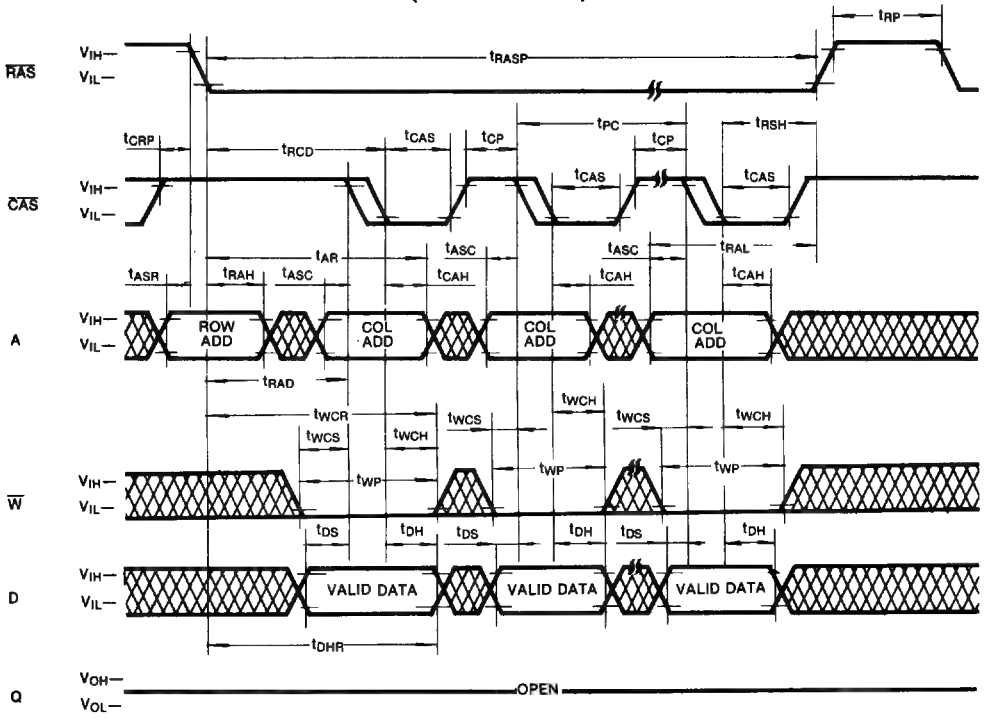
DON'T CARE

TIMING DIAGRAMS

FAST PAGE MODE READ CYCLE

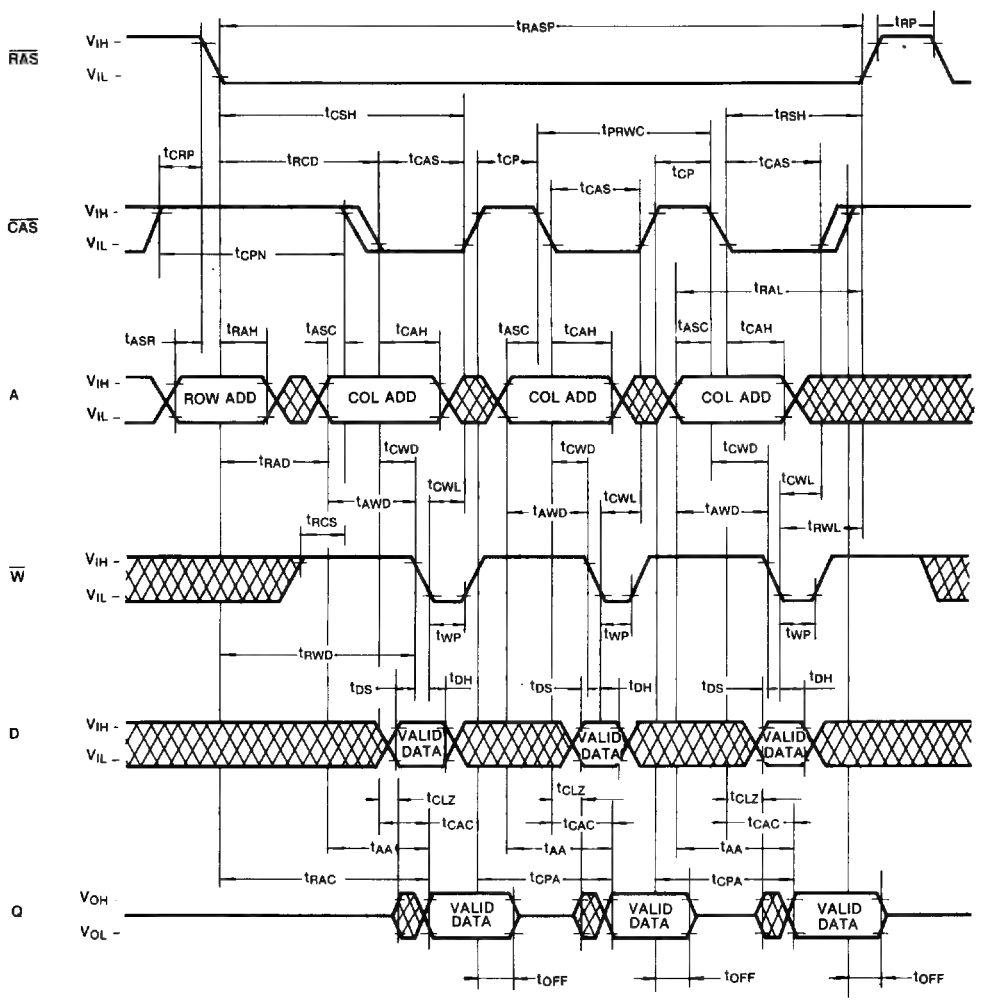


FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



TIMING DIAGRAMS (Continued)

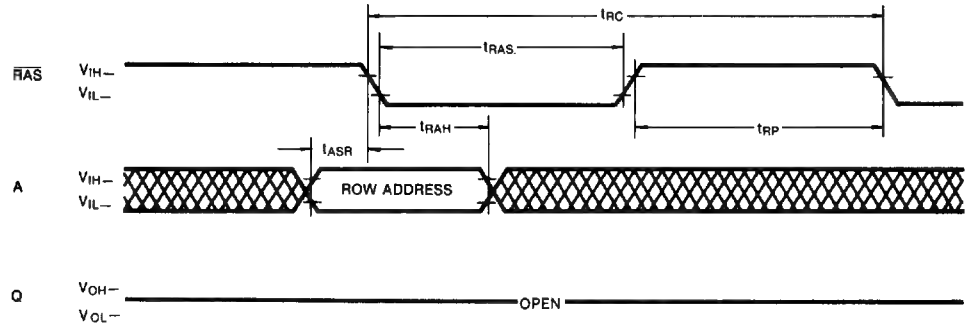
FAST PAGE MODE READ-WRITE CYCLE



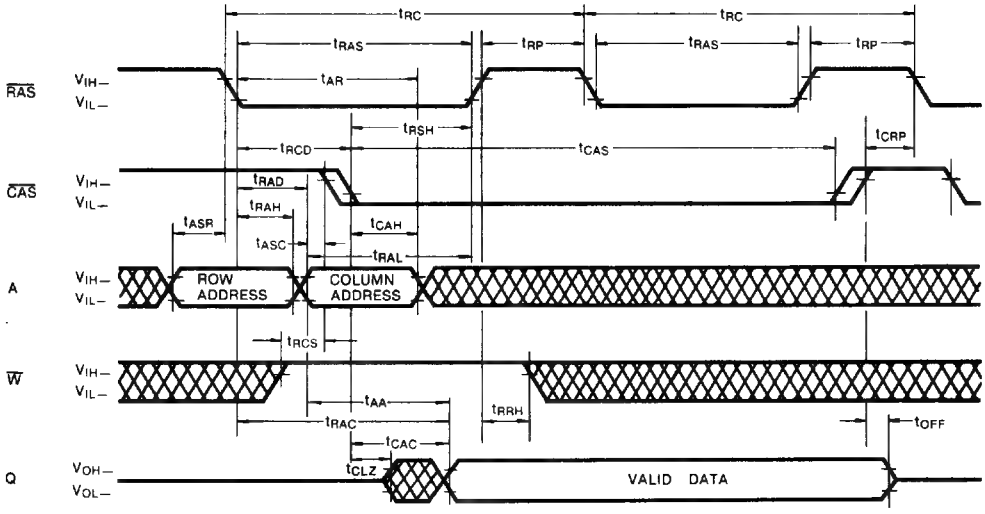
TIMING DIAGRAMS (Continued)

$\overline{RAS}$-ONLY REFRESH CYCLE

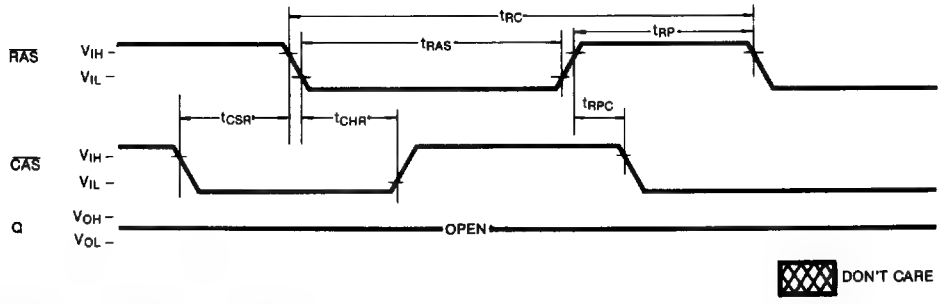
Note: $\overline{CAS}$ = V_{IH}, $\overline{W}$,D, A_9 = Don't Care



HIDDEN REFRESH CYCLE

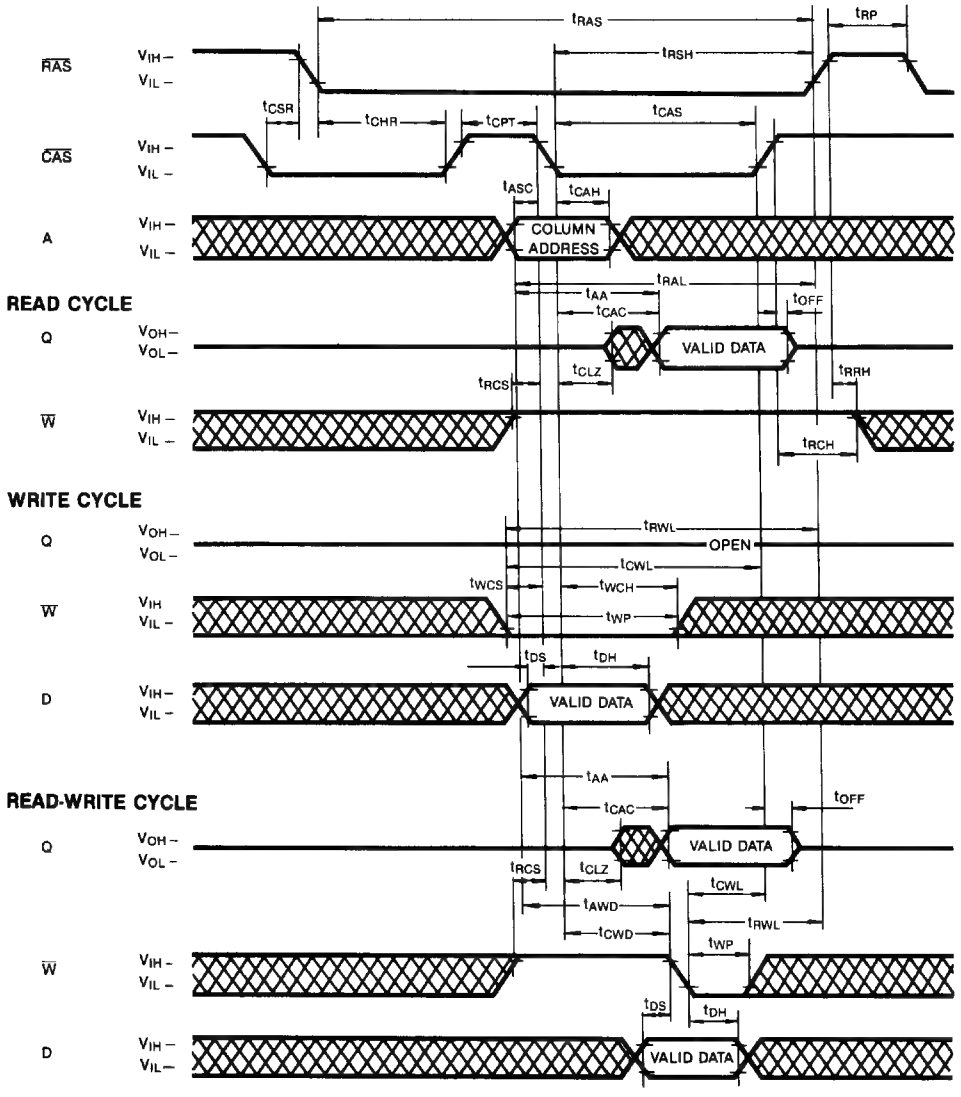


$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE



TIMING DIAGRAMS (Continued)

$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE



KM41C1000 OPERATION

Device Operation

The KM41C1000A contains 1,048,576 memory locations. Twenty address bits are required to address a particular memory location. Since the KM41C1000A has only 10 address input pins, time multiplexed addressing is used to input 10 row and 10 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{RAS}$), the column address strobe ($\overline{CAS}$) and the valid row and column address inputs.

Operation of the KM41C1000A begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. Then the address on the 10 address input pins is changed from a row address to a column address and is strobed in by $\overline{CAS}$. This is the beginning of any KM41C1000A cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both $\overline{RAS}$ and $\overline{CAS}$ have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time (tRP) requirement.

$\overline{RAS}$ and $\overline{CAS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths are specified by tRAS(min) and tCAS(min) respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, tRP, has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM41C1000A begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input($\overline{W}$) high during a $\overline{RAS}$/$\overline{CAS}$ cycle. The access time is normally specified with respect to the falling edge of $\overline{RAS}$. But the access time also depends on the falling edge of $\overline{CAS}$ and on the valid column address transition.

If $\overline{CAS}$ goes low before tRCD(max) and if the column address is valid before tRAD(max) then the access time to valid data is specified by tRAC(min). However, if $\overline{CAS}$ goes low after tRCD(max) or if the column address becomes valid after tRAD(max), access is specified by tCAC or tAA. In order to achieve the minimum access time, tRAC(min), it is necessary to meet both tRCD(max) and tRAD(max).

Write

The KM41C1000A can perform early write, late write and read-modify-write cycles. The differece between these cycles is in the state of data-out and is determined by the timing relationship between $\overline{W}$ and $\overline{CAS}$. In any type of write cycle, Data-in must be valid at or before the falling edge of $\overline{W}$ or $\overline{CAS}$, whichever is later.

Early Write: An early write cycle is performed by bringing $\overline{W}$ low before $\overline{CAS}$. The data at the data input pin (D) is written into the addressed memory cell. Throughout the early write cycle the output remains in the Hi-Z state. This cycle is good for common I/O applications because the data-in and data-out pins may be tied together without bus contention.

Read-Modify-Write: In this cycle, valid data from the addressed cell appears at the output before and during the time that data is being written into the same cell location. This cycle is achieved by bringing $\overline{W}$ low after $\overline{CAS}$ and meeting the data sheet read-modify-write cycle timing requirements. This cycle requires using a separate I/O to avoid bus contention.

Late Write: If $\overline{W}$ is brought low after $\overline{CAS}$, a late write cycle will occur. The late write cycle is very similar to the read-modify-write cycle except that the timing parameters tCWD and tAWD are not necessarily met. The state of data-out is indeterminate since the output can be either Hi-Z or contain data depending on the timing conditions. This cycle requires a separate I/O to avoid bus contention.

Data Output

The KM41C1000A has a tri-state output buffer which is controlled by $\overline{CAS}$. Whenever $\overline{CAS}$ is high (VIH) the output is in the high impedance (Hi-Z) state. In any cycle in which valid data appears at the output, the output goes into the low impedance state in a time specified by tCLZ after the falling edge of $\overline{CAS}$. Invalid data may be present at the output during the time after tCLZ and before the valid data appears at the output. The timing parameters tCAC, tRAC and tAA specify when the valid data will be present at the output. The valid data remains at the output until $\overline{CAS}$ returns high. This is true even if a new $\overline{RAS}$ cycle occurs (as in hidden refresh). Each of the KM41C1000A operating cycles is listed below after the corresponding output state produced by the cycle.

Device Operation (Continued)

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Fast Page Mode Read, Fast Page Mode Read-Modify-Write

Hi-Z Output State: Early Write, $\overline{RAS}$-only Refresh, Fast Page Mode Write, $\overline{CAS}$-before-$\overline{RAS}$ Refresh, $\overline{CAS}$-only cycle.

Indeterminate Output State: Delayed Write

Refresh

The data in the KM41C1000A is stored on a tiny capacitor within each memory cell. Due to leakage the data may leak off after a period of time. To maintain data integrity it is necessary to refresh each of the rows every 8 ms. There are several ways to accomplish this.

$\overline{RAS}$-Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. This cycle must be repeated for each of the 512 row addresses, (A0-A8). The state of address A9 is ignored during refresh.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh: The KM41C1000A has $\overline{CAS}$-before-$\overline{RAS}$ on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{CAS}$ is held low for the specified set up time (tCSR) before $\overline{RAS}$ goes low, the on-chip refresh circuitry is enabled. An internal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the $\overline{CAS}$ active time and cycling $\overline{RAS}$. The KM41C1000A hidden refresh cycle is actually a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter.

Other Refresh Methods: It is also possible to refresh the KM41C1000A by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in that row are automatically refreshed. There are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh is the preferred method.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle

A special timing sequence using the $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle provides a convenient method of verifying the functionality of the $\overline{CAS}$-before-$\overline{RAS}$ refresh activated circuitry. The cycle begins as a $\overline{CAS}$-before-$\overline{RAS}$ refresh operation. Then, if $\overline{CAS}$ is brought high and then low again while $\overline{RAS}$ is held low, the read and write operations are enabled. In this mode, the row address bits A0 through A8 are supplied by the on-chip refresh counter. The A9 bit is set low internally.

Fast Page Mode

The KM41C1000A has Fast Page mode capability which provides high speed read, write or read-modify-write access to all memory cells within a selected row. These cycles may be mixed in any order. A fast page mode cycle begins with a normal cycle. Then, while $\overline{RAS}$ is kept low to maintain the row address, $\overline{CAS}$ is cycled to strobe in additional column addresses. This eliminates the time required to set up and strobe sequential row addresses for the same page.

Power-up

If $\overline{RAS} = V_{SS}$ during power-up, the KM41C1000A could begin an active cycle. This condition results in higher than necessary current demands from the power supply during power-up. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{CC} during power-up or be held at a valid VIH in order to minimize the power-up current.

An initial pause of 200 μsec is required after power-up followed by 8 initialization cycles before proper device operation is assured. Eight initialization cycles are also required after any 8 msec period in which there are no $\overline{RAS}$ cycles. An initialization cycle is any cycle in which $\overline{RAS}$ is cycled.

Termination

The lines from the TTL driver circuits to the KM41C1000A inputs act like unterminated transmission lines resulting in significant overshoot and undershoot at the inputs. To minimize overshoot it is advisable to terminate the input lines and to keep them as short as possible. Although either series or parallel termination may be used, series termination is generally recommended since it is simple and draws no additional power. It consists of a resistor in series with the input line placed close to the KM41C1000A input pin. The optimum value depends on the board layout. It must be determined experimentally and is usually in the range of 20 to 40 ohms..

Device Operation (Continued)

Board Layout

It is important to lay out the power and ground lines on memory boards in such a way that switching transient effects are minimized. The recommended methods are gridded power and ground lines or separate power and ground planes. The power and ground lines act like transmission lines to the high frequency transients generated by DRAMS. The impedance is minimized if all the power supply traces to all the DRAMS run both horizontally and vertically and are connected at each intersection or better yet if power and ground planes are used.

Decoupling

The importance of proper decoupling can not be over emphasized. Excessive transient noise or voltage droop on the V_{CC} line can cause loss of data integrity (soft errors). It is recommended that the total combined voltage changes over time in the VCC to VSS voltage (measured at the device pins) should not exceed 500mV.

A high frequency 0.3μF ceramic decoupling capacitor should be connected between the V_{CC} and ground pins of each KM41C1000A using the shortest possible traces. These capacitors act as a low impedance shunt for the high frequency switching transients generated by the KM41C1000A and they supply much of the current used by the KM41C1000A during cycling.

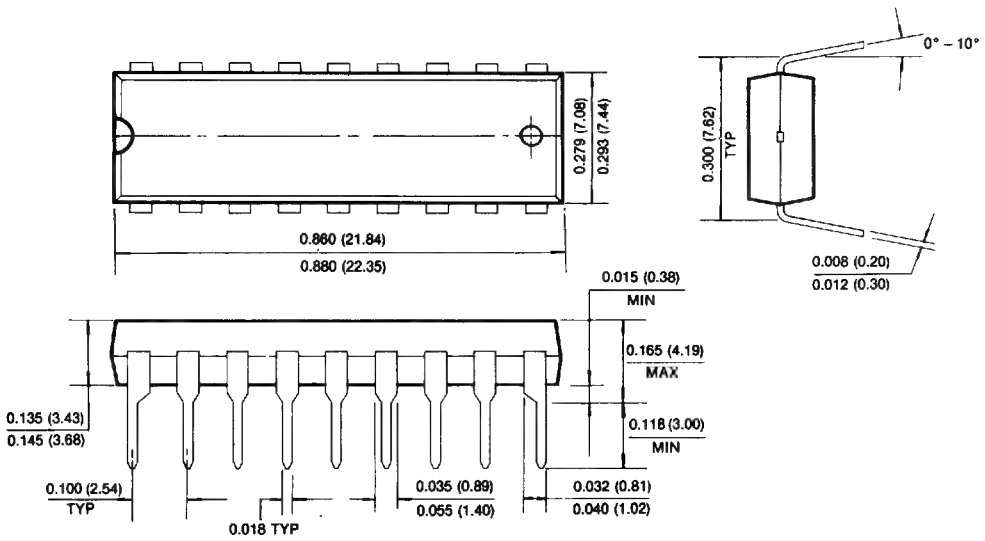
In addition, a large tantalum capacitor with a value of 47μF to 100μF should be used for bulk decoupling to recharge the 0.3μF capacitors between cycles, thereby reducing power line droop. The bulk decoupling capacitor should be placed near the point where the power traces meet the power grid or power plane. Even better results may be achieved by distributing more than one tantalum capacitor around the memory array.

2

PACKAGE DIMENSIONS

18-LEAD PLASTIC DUAL IN-LINE PACKAGE

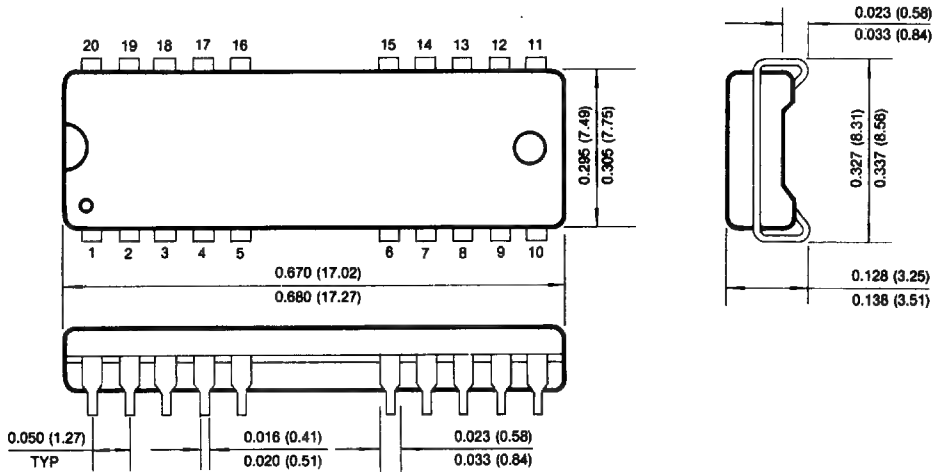
Units: Inches (Millimeters)



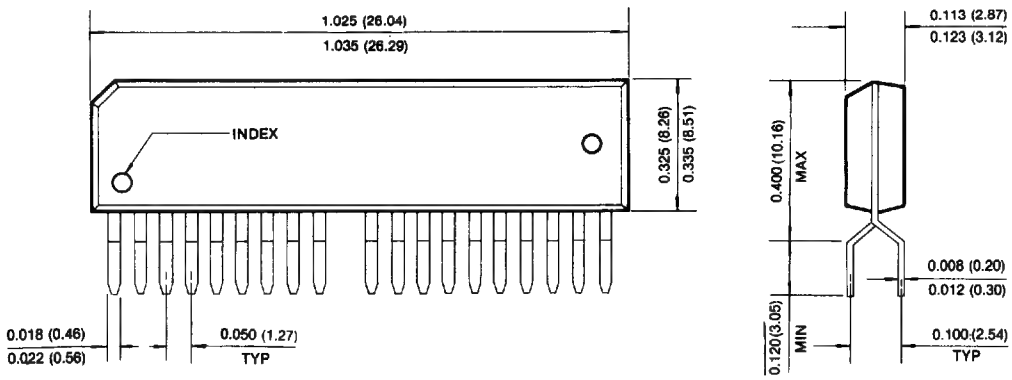
PACKAGE DIMENSIONS

20-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



20-LEAD PLASTIC ZIGZAG-IN-LINE PACKAGE



1M x 1 Bit Dynamic RAM with Nibble Mode

FEATURES

- **Performance range:**

	t_{RAC}	t_{CAC}	t_{RC}
KM41C1001A- 7	70ns	20ns	130ns
KM41C1001A- 8	80ns	20ns	150ns
KM41C1001A-10	100ns	25ns	180ns

- **Nibble Mode Operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ Refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **TTL compatible inputs and output**
- **Common I/O using early write**
- **Single +5V ± 10% power supply**
- **512 cycle/8ms refresh**
- **256K x 4 fast test mode**
- **JEDEC standard pinout available in Plastic DIP, SOJ, ZIP packages.**

GENERAL DESCRIPTION

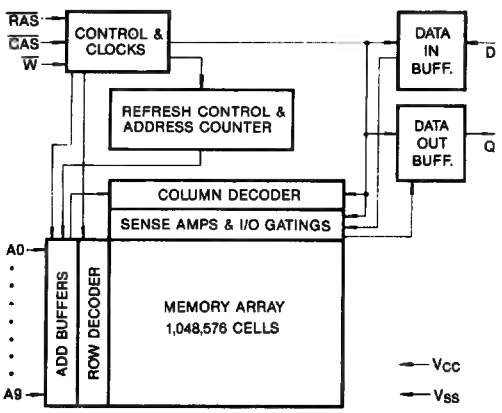
The Samsung KM41C1001A is a CMOS high speed 1,048,576 x 1 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes and mini computers, graphics and high performance microprocessor systems.

The KM41C1001A features Nibble Mode operation which allows high speed random access of up to 4-bits of data.

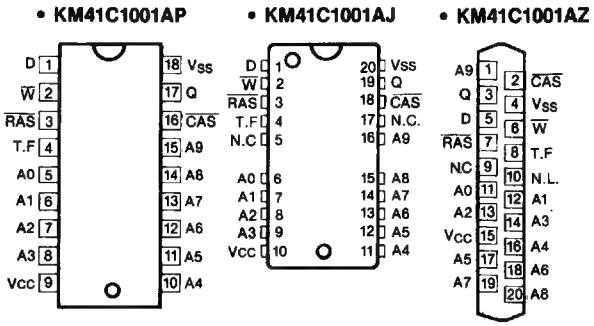
$\overline{CAS}$-before-$\overline{RAS}$ Refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only Refresh. All inputs and output are fully TTL compatible.

The KM41C1001A is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Pin Name	Pin Function
A_0-A_9	Address Inputs
$\overline{RAS}$	Row Address Strobe
D	Data In
Q	Data Out
$\overline{CAS}$	Column Address Strobe
$\overline{W}$	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground
T.F	Test Function
N.C	No Connection
N.L	No Lead

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−1 to +7.0	V
Storage Temperature	T_{stg}	−55 to +150	°C
Power Dissipation	P_D	0.6	W
Short Circuit Output Current	I_{OS}	50	mA

*Note: Permanent device damage may occur of "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC}+1	V
Input Low Voltage	V_{IL}	−1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
OPERATING CURRENT* ($\overline{RAS}$, $\overline{CAS}$, Address cycling @t_{RC} = min.)	KM41C1001A-7 KM41C1001A-8 KM41C1001A-10	I_{CC1}	—	85 75 65	mA
STANDBY CURRENT ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		I_{CC2}	—	2	mA
$\overline{RAS}$-ONLY REFRESH CURRENT* ($\overline{CAS}$ = V_{IH}, $\overline{RAS}$ cycling @t_{RC} = min.)	KM41C1001A-7 KM41C1001A-8 KM41C1001A-10	I_{CC3}	—	85 75 65	mA
NIBBLE MODE CURRENT* ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling; @t_{NC} = min.)	KM41C1001A-7 KM41C1001A-8 KM41C1001A-10	I_{CC4}	—	70 60 50	mA
STANDBY CURRENT ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} − 0.2V)		I_{CC5}	—	1	mA
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CURRENT* ($\overline{RAS}$ and $\overline{CAS}$ cycling @t_{RC} = min.)	KM41C1001A-7 KM41C1001A-8 KM41C1001A-10	I_{CC6}	—	85 75 65	mA
INPUT LEAKAGE CURRENT (Any input 0≤V_{IN}≤6.5V, all other pins not under test = 0 volts.)		I_{IL}	−10	10	μA
OUTPUT LEAKAGE CURRENT (Data out is disabled, 0V≤V_{OUT}≤5.5V		I_{OL}	−10	10	μA
OUTPUT HIGH VOLTAGE LEVEL (I_{OH} = −5mA)		V_{OH}	2.4	—	V
OUTPUT LOW VOLTAGE LEVEL (I_{OL} = 4.2mA)		V_{OL}	—	0.4	V

*Note: I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current.

CAPACITANCE ($T_A = 25°C$)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (D)	C_{IN1}	—	5	pF
Input Capacitance (A_0-A_9)	C_{IN2}	—	6	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{W}$)	C_{IN3}	—	7	pF
Output Capacitance (Q)	C_{OUT}	—	7	pF

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC} = 5.0V \pm 10\%$, See notes 1, 2)

Parameter	Symbol	KM41C1001A-7		KM41C1001A-8		KM41C1001A-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	130		150		180		ns	
Read-modify-write cycle time	t_{RWC}	155		175		210		ns	
Access time from $\overline{RAS}$	t_{RAC}		70		80		100	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		20		20		25	ns	3,4,5
Access time from column address	t_{AA}		35		40		50	ns	3,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	5		5		5		ns	3
Output buffer turn-off delay	t_{OFF}	0	25	0	25	0	30	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	50		60		70		ns	
$\overline{RAS}$ pulse width	t_{RAS}	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		20		25		ns	
$\overline{CAS}$ hold time	t_{CSH}	70		80		100		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	20	10,000	25	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	50	25	60	25	75	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	35	20	40	20	50	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		15		15		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		20		20		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	55		65		75		ns	6
Column address to $\overline{RAS}$ lead time	t_{RAL}	35		40		50		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	9

STANDARD OPERATION (Continued)

Parameter	Symbol	KM41C1001A-7		KM41C1001A-8		KM41C1001A-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	9
Write command hold time	t_{WCH}	15		15		20		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	55		60		75		ns	6
Write command pulse width	t_{WP}	15		15		20		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		20		25		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	20		20		25		ns	
Data-in set-up time	t_{DS}	0		0		0		ns	10
Data-in hold time	t_{DH}	15		20		20		ns	10
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	55		65		75		ns	6
Refresh period (512 cycles)	t_{REF}		8		8		8	ms	
Write command set-up time	t_{WCS}	0		0		0		ns	8
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	20		20		25		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	70		80		100		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	35		40		50		ns	8

NIBBLE MODE

Nibble Mode Cycle Time	t_{NC}	40		40		45		ns	
Nibble Mode Read-Write Cycle Time	t_{NRWC}	65		65		70		ns	
Nibble Mode Access Time	t_{NCAC}		20		20		25	ns	
Nibble Mode $\overline{CAS}$ Pulse Width	t_{NCAS}	20		20		25		ns	
Nibble Mode $\overline{CAS}$ Precharge Time	t_{NCP}	10		10		10		ns	
Nibble Mode $\overline{RAS}$ Hold Time	t_{NRSH}	20		20		25		ns	
Nibble Mode $\overline{CAS}$ to $\overline{W}$ Delay Time	t_{NCWD}	20		20		25		ns	
Nibble Mode $\overline{W}$ to $\overline{RAS}$ Lead Time	t_{NRWL}	20		20		25		ns	
Nibble Mode $\overline{W}$ to $\overline{CAS}$ Lead Time	t_{NCWL}	20		20		25		ns	

$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH

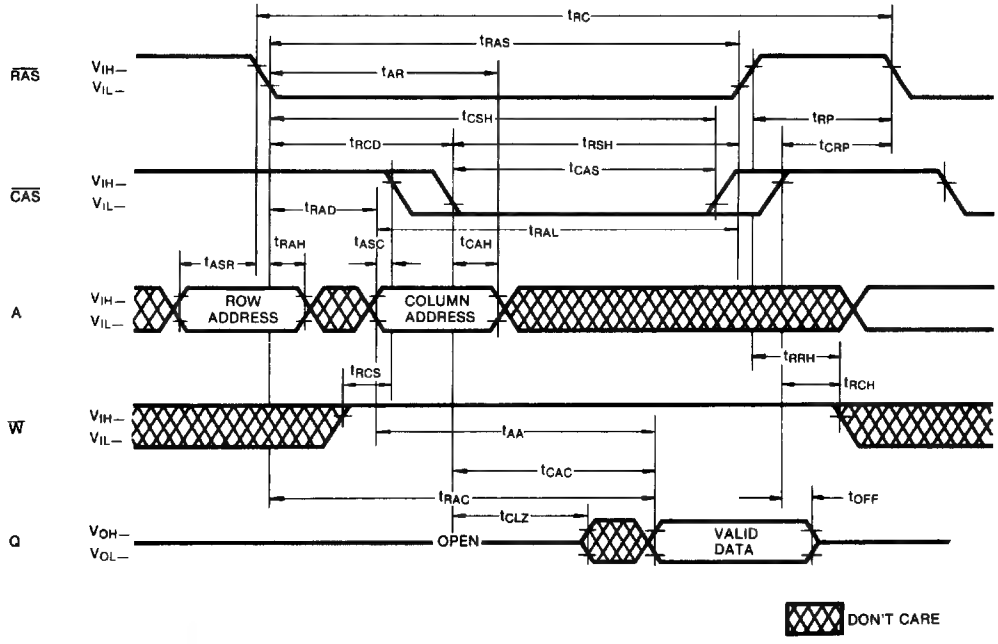
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	20		25		30		ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	10		10		10		ns	
Refresh counter test $\overline{CAS}$ precharge time	t_{CPT}	35		40		50		ns	

NOTES

1. An initial pause of 200μs is required after power up' followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max), and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met, t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$(max).
6. t_{AR}, t_{WCH}, t_{DHR} are referenced to t_{RAD}(max).
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data output will remain open circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$(min) and $t_{RWD} \geq t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$(min), then the cycle is a read-write cycle and the data output will contain data read from the selected cell. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycles.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met, t_{RAD}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
12. Normal operation requires the "T.F" pin to be connected to V_{SS} or TTL logic low level or left unconnected on the printed wiring board.
13. When the "T.F" pin is connected to a defined positive voltage, the internal test function may be activated. Contact Samsung for specific operational details of the "test function."

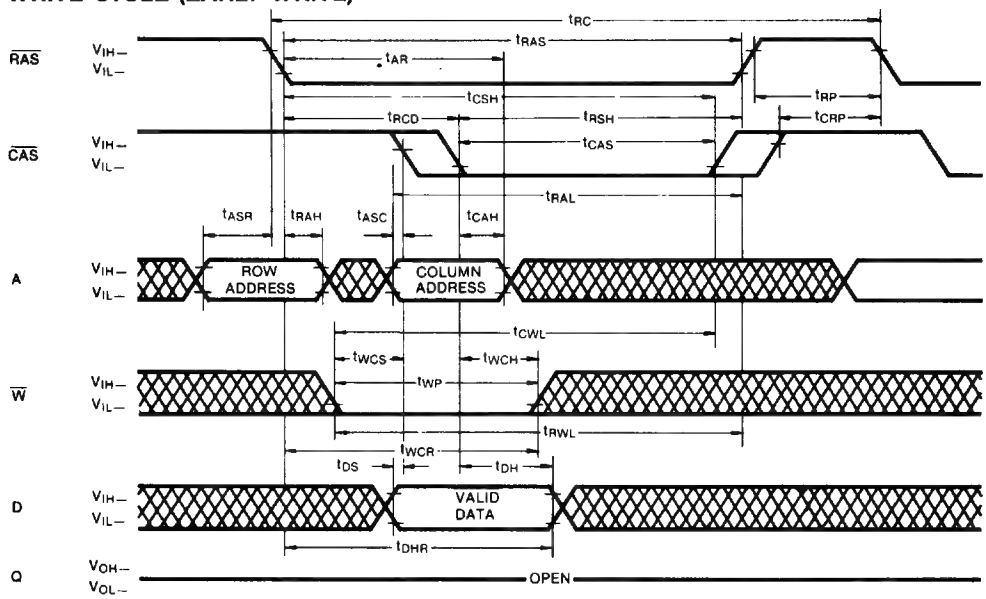
TIMING DIAGRAMS

READ CYCLE

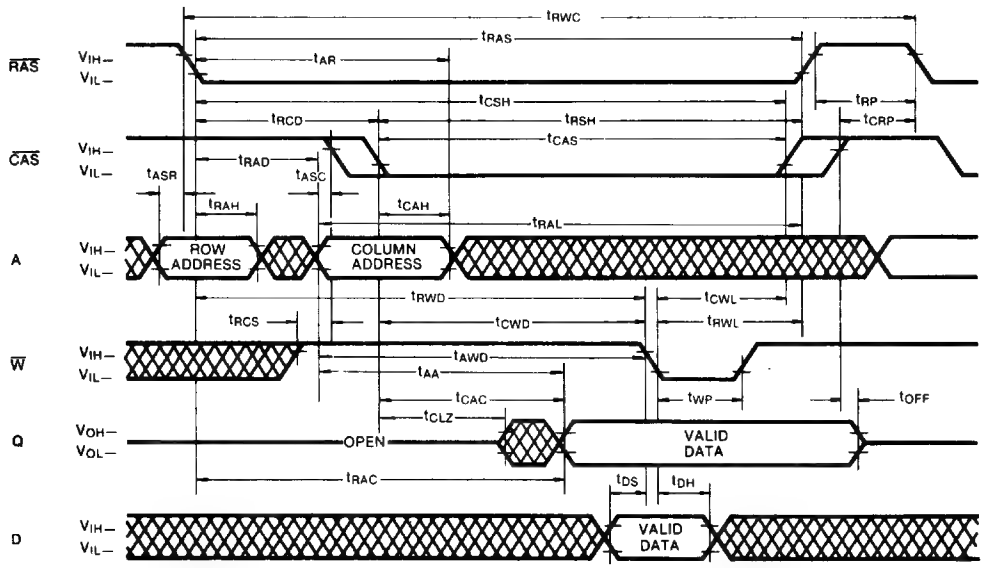


TIMING DIAGRAMS (Continued)

WRITE CYCLE (EARLY WRITE)



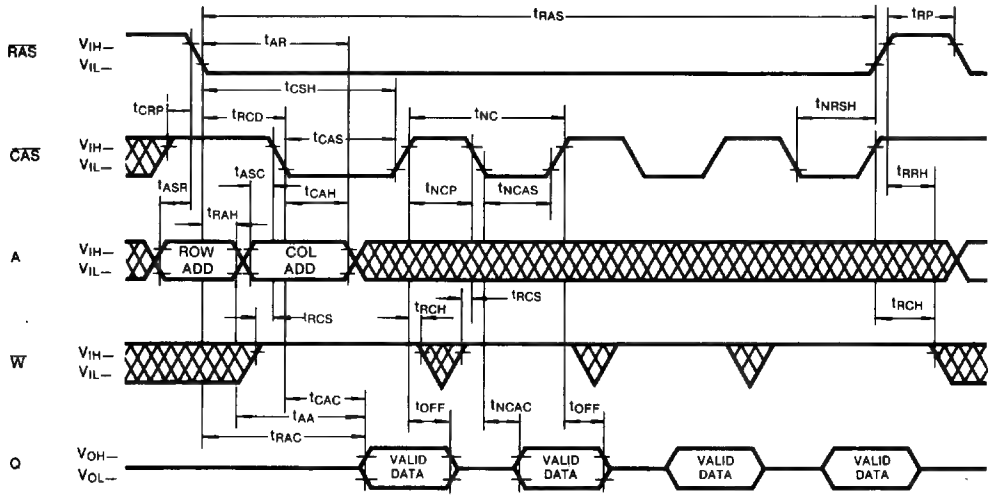
READ-WRITE/READ-MODIFY-WRITE CYCLE



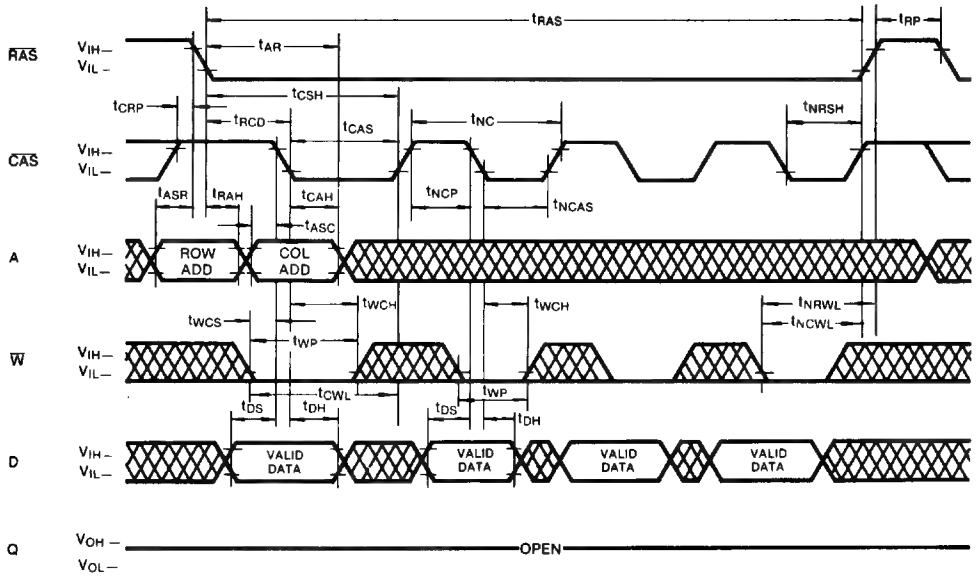
DON'T CARE

TIMING DIAGRAMS (Continued)

NIBBLE MODE READ CYCLE



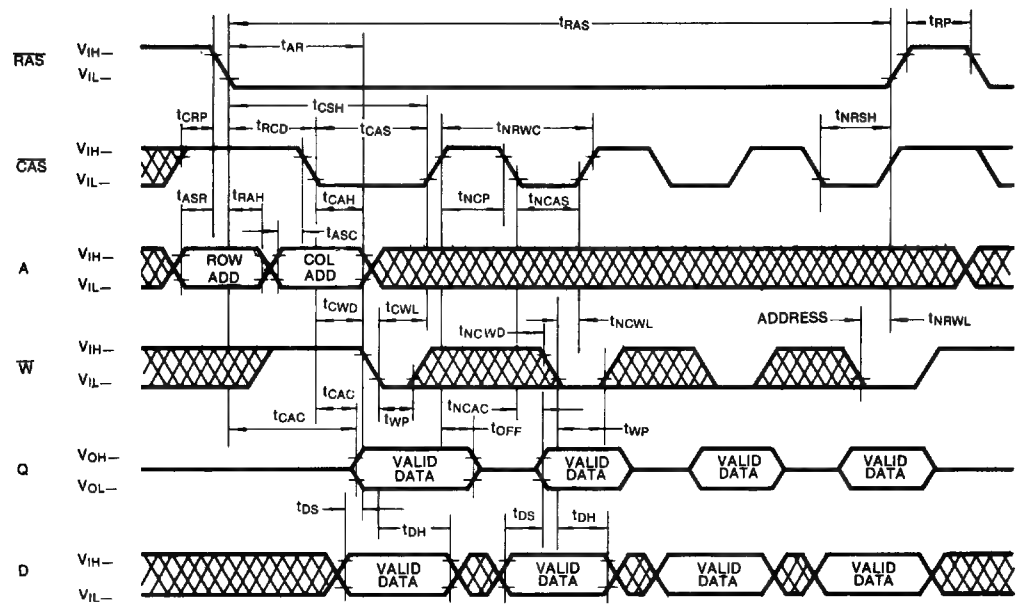
NIBBLE MODE WRITE CYCLE



DON'T CARE

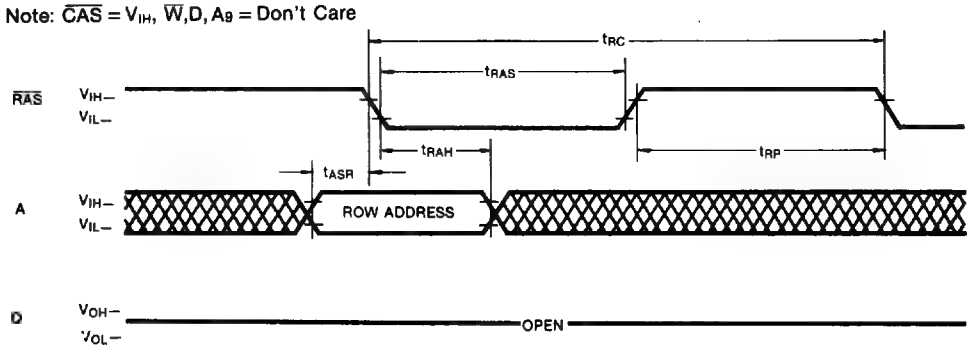
TIMING DIAGRAMS (Continued)

NIBBLE MODE READ-WRITE CYCLE



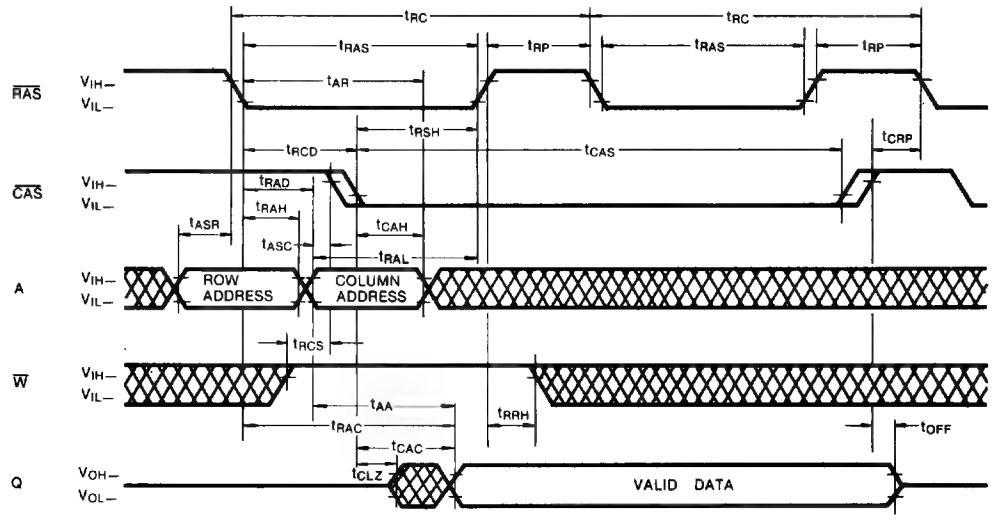
RAS-ONLY REFRESH CYCLE

Note: $\overline{CAS}$ = V_{IH}, $\overline{W}$,D, A_9 = Don't Care



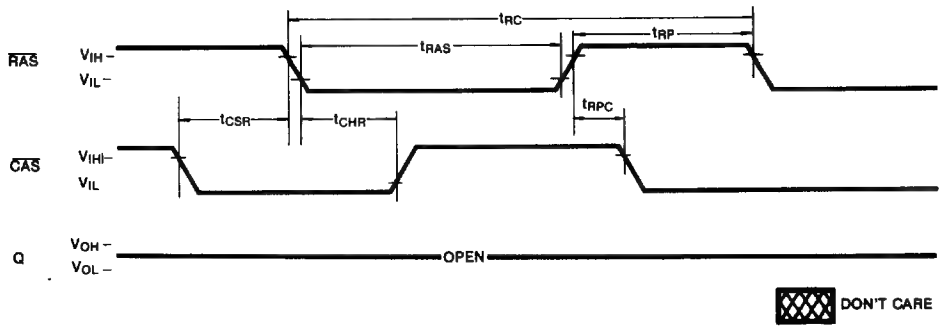
TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE



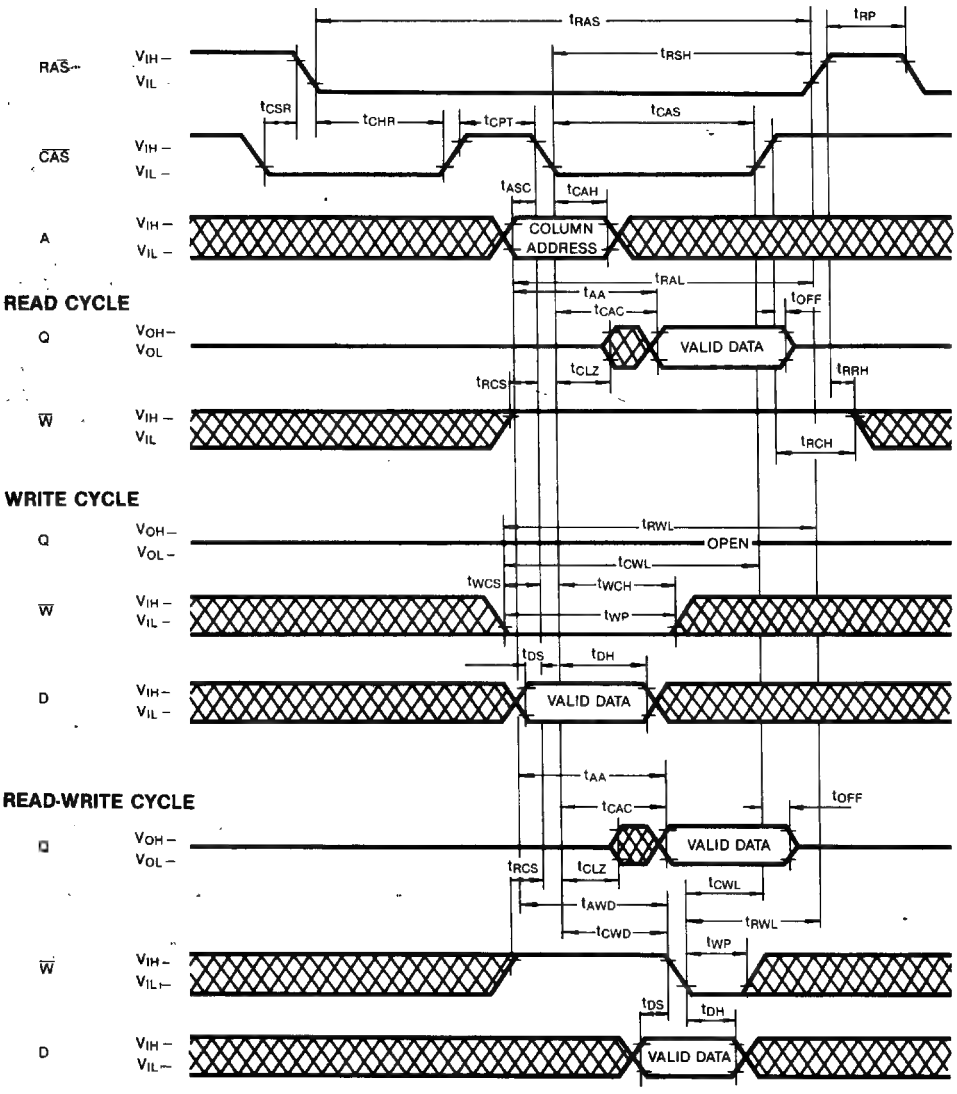
CAS-BEFORE-RAS REFRESH CYCLE

NOTE: $\overline{W}$ = Don't Care, A_0-A_9 = Don't Care



TIMING DIAGRAMS (Continued)

$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE



DON'T CARE

KM41C1001A OPERATION

Device Operation

The KM41C1001A contains 1,048,576 memory locations. Twenty address bits are required to address a particular memory location. Since the KM41C1001A has only 10 address input pins, time multiplexed addressing is used to input 10 row and 10 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{RAS}$), the column address strobe ($\overline{CAS}$) and the valid row and column address inputs.

Operation of the KM41C1001A begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. Then the address on the 10 address input pins is changed from a row address to a column address and is strobed in by $\overline{CAS}$. This is the beginning of any KM41C1001A cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both $\overline{RAS}$ and $\overline{CAS}$ have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time (tRP) requirement.

$\overline{RAS}$ and $\overline{CAS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths are specified by tRAS(min) and tCAS(min) respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, tRP, has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM41C1001A begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input($\overline{W}$) high during a $\overline{RAS}$/$\overline{CAS}$ cycle. The access time is normally specified with respect to the falling edge of $\overline{RAS}$. But the access time also depends on the falling edge of $\overline{CAS}$ and on the valid column address transition.

If $\overline{CAS}$ goes low before tRCD(max) and if the column address is valid before tRAD(max) then the access time to valid data is specified by tRAC(min). However, if $\overline{CAS}$ goes low after tRCD(max) or if the column address becomes valid after tRAD(max), access is specified by tCAC or tAA. In order to achieve the minimum access time, tRAC(min), it is necessary to meet both tRCD(max) and tRAD(max).

Write

The KM41C1001A can perform early write, late write and read-modify-write cycles. The differece between these cycles is in the state of data-out and is determined by the timing relationship between $\overline{W}$ and $\overline{CAS}$. In any type of write cycle, Data-in must be valid at or before the falling edge of $\overline{W}$ or $\overline{CAS}$, whichever is later.

Early Write: An early write cycle is performed by bringing $\overline{W}$ low before $\overline{CAS}$. The data at the data input pin (D) is written into the addressed memory cell. Throughout the early write cycle the output remains in the HI-Z state. This cycle is good for common I/O applications because the data-in and data-out pins may be tied together without bus contention.

Read-Modify-Write: In this cycle, valid data from the addressed cell appears at the output before and during the time that data is being written into the same cell location. This cycle is achieved by bringing $\overline{W}$ low after $\overline{CAS}$ and meeting the data sheet read-modify-write cycle timing requirements. This cycle requires using a separate I/O to avoid bus contention.

Late Write: If $\overline{W}$ is brought low after $\overline{CAS}$, a late write cycle will occur. The late write cycle is very similar to the read-modify-write cycle except that the timing parameters tCWD and tAWD are not necessarily met. The state of data-out is indeterminate since the output can be either HI-Z or contain data depending on the timing conditions. This cycle requires a separate I/O to avoid bus contention.

Data Output

The KM41C1001A has a tri-state output buffer which is controlled by $\overline{CAS}$. Whenever $\overline{CAS}$ is high (VIH) the output is in the high impedance (Hi-Z) state. In any cycle in which valid data appears at the output, the output goes into the low impedance state in a time specified by tCLZ after the falling edge of $\overline{CAS}$. Invalid data may be present at the output during the time after tCLZ and before the valid data appears at the output. The timing parameters tCAC, tRAC and tAA specify when the valid data will be present at the output. The valid data remains at the output until $\overline{CAS}$ returns high. This is true even if a new $\overline{RAS}$ cycle occurs (as in hidden refresh). Each of the KM41C1001A operating cycles is listed below after the corresponding output state produced by the cycle.

Device Operation (Continued)

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Nibble Mode Read, Nibble Mode Read-Modify-Write.

Hi-Z Output State: Early Write, $\overline{RAS}$-only Refresh, Nibble Mode Write, $\overline{CAS}$-before-$\overline{RAS}$ Refresh, $\overline{CAS}$-only cycle.

Indeterminate Output State: Delayed Write

Refresh

The data in the KM41C1001A is stored on a tiny capacitor within each memory cell. Due to leakage the data may leak off after a period of time. To maintain data integrity it is necessary to refresh each of the rows every 8 ms. There are several ways to accomplish this.

$\overline{RAS}$-Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. This cycle must be repeated for each of the 512 row addresses, (A0-A8). The state of address A9 is ignored during refresh.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh: The KM41C1001A has $\overline{CAS}$-before-$\overline{RAS}$ on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{CAS}$ is held low for the specified set up time (tCSR) before $\overline{RAS}$ goes low, the on-chip refresh circuitry is enabled. An internal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the $\overline{CAS}$ active time and cycling $\overline{RAS}$. The KM41C1001A hidden refresh cycle is actually a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter.

Other Refresh Methods: It is also possible to refresh the KM41C1001A by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in that row are automatically refreshed. There are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh is the preferred method.

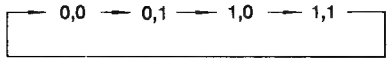
$\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle

A special timing sequence using the $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle provides a convenient method of verifying the functionality of the $\overline{CAS}$-before-$\overline{RAS}$ refresh activated circuitry. The cycle begins as a $\overline{CAS}$-before-$\overline{RAS}$ refresh operation. Then, if $\overline{CAS}$ is brought high and then low again while $\overline{RAS}$ is held low, the read and write operations are enabled. In this mode, the row address bits A0 through A8 are supplied by the on-chip refresh counter. The A9 bit is set low internally.

Nibble Mode

The KM41C1001A has Nibble mode capability. Nibble mode operation allows high speed serial read, write or read-modify-write access of 4 consecutive bits. The first of 4 bits is accessed in the usual manner. The remaining nibble bits are accessed by toggling $\overline{CAS}$ high then low while $\overline{RAS}$ remains low.

The 4 bits of data that may be accessed during Nibble mode are determined by the lower 9 row address bits (R_{A0}-R_{A8}) and 9 column address bits (C_{A0}-C_{A8}). The two address bits, C_{A9} and R_{A9}, are used to select 1 of the 4 nibble bits for initial access. The remaining nibble bits are accessed by toggling $\overline{CAS}$ with $\overline{RAS}$ held low. Each high-low $\overline{CAS}$ transition will internally increment the nibble address (C_{A9}, R_{A9}) as shown in the following diagram with R_{A9} being the least significant bit.



If more than 4 bits are accessed during Nibble mode, the address sequence will wrap around and repeat. If any bit is written during Nibble mode, the new data will be read on any subsequent access. If the write operation is executed again on a subsequent access, the new data will be written into the selected cell location.

A Nibble mode cycle can be a read, write, or read-modify-write cycle. Any combinations of reads and writes or read-modify-write are allowed.

Power-up

If $\overline{RAS} = V_{SS}$ during power-up, the KM41C1001A could begin an active cycle. This condition results in higher than necessary current demands from the power supply during power-up. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{CC} during power-up or be held at a valid VIH in order to minimize the power-up current.

An initial pause of 200 μsec is required after power-up followed by 8 initialization cycles before proper device operation is assured. Eight initialization cycles are also required after any 8 msec period in which there are no $\overline{RAS}$ cycles. An initialization cycle is any cycle in which $\overline{RAS}$ is cycled.

Termination

The lines from the TTL driver circuits to the KM41C1001A inputs act like unterminated transmission lines resulting in significant overshoot and undershoot at the inputs. To minimize overshoot it is advisable to terminate the input lines and to keep them as short as possible. Although either series or parallel termination may be used, series termination is generally recommended since it is simple and draws no additional power. It consists of a resistor in series with the input line placed close to the KM41C1001A input pin. The optimum value depends on the board layout. It must be determined experimentally and is usually in the range of 20 to 40 ohms.

Board Layout

It is important to lay out the power and ground lines on memory boards in such a way that switching transient effects are minimized. The recommended methods are gridded power and ground lines or separate power and ground planes. The power and ground lines act like transmission lines to the high frequency transients generated by DRAMS. The impedance is minimized if all the power supply traces to all the DRAMS run both horizontally and vertically and are connected at each intersection or better yet if power and ground planes are used.

Decoupling

The importance of proper decoupling can not be over emphasized. Excessive transient noise or voltage droop on the V_{CC} line can cause loss of data integrity (soft errors). It is recommended that the total combined voltage changes over time in the VCC to VSS voltage (measured at the device pins) should not exceed 500mV.

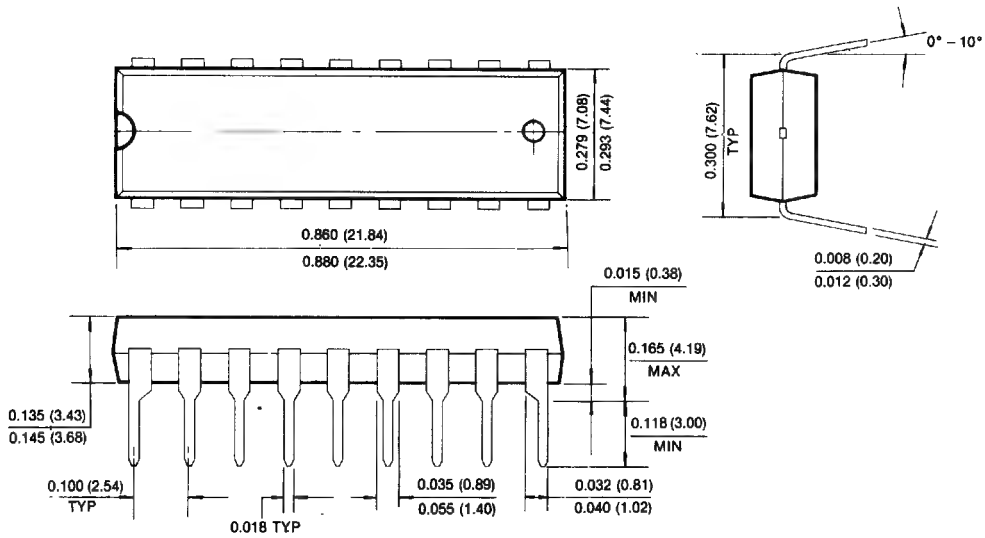
A high frequency 0.3μF ceramic decoupling capacitor should be connected between the V_{CC} and ground pins of each KM41C1001A using the shortest possible traces. These capacitors act as a low impedance shunt for the high frequency switching transients generated by the KM41C1001A and they supply much of the current used by the KM41C1001A during cycling.

In addition, a large tantalum capacitor with a value of 47μF to 100μF should be used for bulk decoupling to recharge the 0.3μF capacitors between cycles, thereby reducing power line droop. The bulk decoupling capacitor should be placed near the point where the power traces meet the power grid or power plane. Even better results may be achieved by distributing more than one tantalum capacitor around the memory array.

PACKAGE DIMENSIONS

18-LEAD PLASTIC DUAL IN-LINE PACKAGE

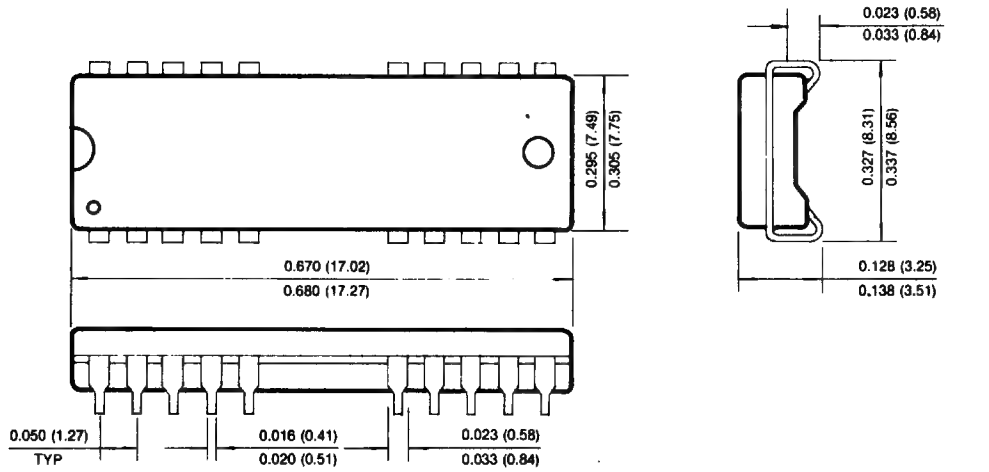
Units: Inches (Millimeters)



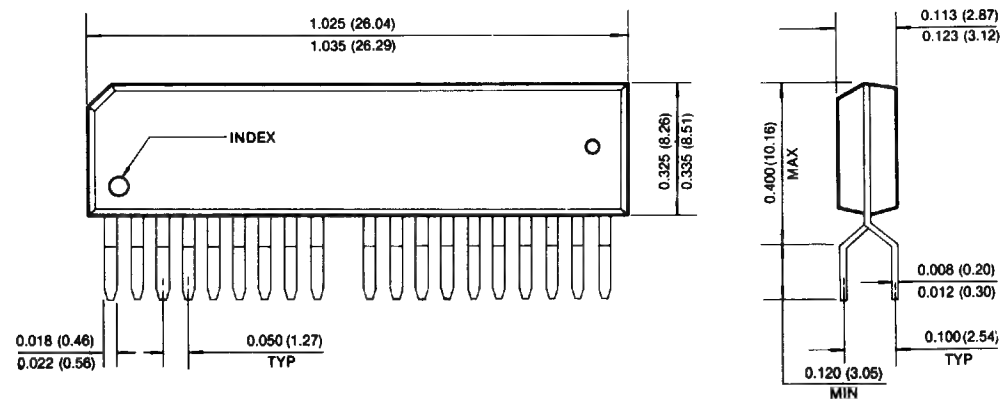
PACKAGE DIAGRAMS (Continued)

20-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



20-PIN PLASTIC ZIGZAG-IN-LINE PACKAGE



1M x 1 Bit Dynamic RAM with Static Column Mode

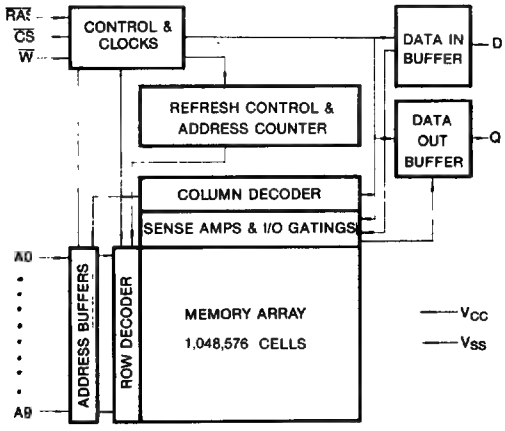
FEATURES

- **Performance range:**

	t_{RAC}	t_{CAC}	t_{RC}
KM41C1002A- 7	70ns	20ns	130ns
KM41C1002A- 8	80ns	20ns	150ns
KM41C1002A-10	100ns	25ns	180ns

- **Static Column Mode operation**
- **$\overline{CS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **TTL compatible inputs and output**
- **Common I/O using 'Early Write'**
- **Single +5V ± 10% power supply**
- **512 cycles/8ms refresh**
- **256K x 4 fast test mode**
- **JEDEC standard pinout**
- **Available in Plastic DIP, SOJ and ZIP**

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The Samsung KM41C1002A is a CMOS high speed 1,048,576 x 1 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes and mini computers, graphics and high performance microprocessor systems.

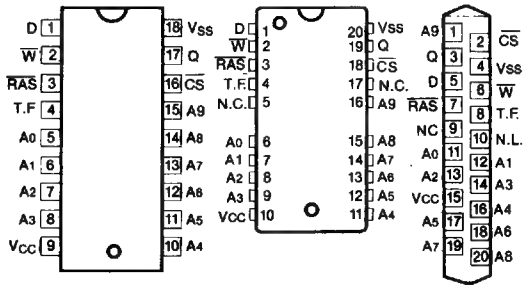
The KM41C1002A features Static Column Mode operation which allows high speed random or Sequential access within a row. Static Column Mode operation offers high performance while relaxing many critical system timing requirements for fast usable speed.

$\overline{CS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only Refresh. All inputs and output are fully TTL compatible.

The KM41C1002A is fabricated using Samsung's advanced CMOS process.

PIN CONFIGURATION

- **KM41C1002AP** • **KM41C1002AJ** • **KM41C1002AZ**



Pin Name	Pin Function
A_0-A_9	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CS}$	Chip Select Input
$\overline{W}$	Read/Write Input
D	Data In
Q	Data Out
T.F.	Test Function
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection
N.L.	No Lead

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−1 to +7.0	V
Storage Temperature	T_{stg}	−55 to +150	°C
Power Dissipation	P_D	0.6	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC}+1	V
Input Low Voltage	V_{IL}	−1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
OPERATING CURRENT* ($\overline{RAS}$, $\overline{CS}$, Address cycling @t_{RC} = min.)	KM41C1002A-7 KM41C1002A-8 KM41C1002A-10	I_{CC1}	—	80 70 60	mA
STANDBY CURRENT ($\overline{RAS}$ = $\overline{CS}$ = V_{IH})		I_{CC2}	—	2	mA
$\overline{RAS}$-ONLY REFRESH CURRENT* ($\overline{CS}$ = V_{IH}, $\overline{RAS}$ cycling @t_{RC} = min.)	KM41C1002A-7 KM41C1002A-8 KM41C1002A-10	I_{CC3}	—	80 70 60	mA
STATIC COLUMN MODE CURRENT* ($\overline{CS}$ = V_{IH}, $\overline{RAS}$ cycling; @t_{SC} = min.)	KM41C1002A-7 KM41C1002A-8 KM41C1002A-10	I_{CC4}	—	60 50 40	mA
STANDBY CURRENT ($\overline{RAS}$ = $\overline{CS}$ = V_{CC} − 0.2V)		I_{CC5}	—	1	mA
$\overline{CS}$-BEFORE-$\overline{RAS}$ REFRESH CURRENT* ($\overline{RAS}$ and $\overline{CS}$ cycling @t_{RC} = min.)	KM41C1002A-7 KM41C1002A-8 KM41C1002A-10	I_{CC6}	—	80 70 60	mA
INPUT LEAKAGE CURRENT (Any input 0≤V_{IN}≤6.5V, all other pins not under test = 0 volts.)		I_{IL}	−10	10	μA
OUTPUT LEAKAGE CURRENT (Data out is disabled, 0V≤V_{OUT}≤5.5V		I_{OL}	−10	10	μA
OUTPUT HIGH VOLTAGE LEVEL (I_{OH} = −5mA)		V_{OH}	2.4	—	V
OUTPUT LOW VOLTAGE LEVEL (I_{OL} = 4.2mA)		V_{OL}	—	0.4	V

*Note: I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current.

CAPACITANCE ($T_A = 25°C$)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (D)	C_{IN1}	—	5	pF
Input Capacitance (A_0-A_9)	C_{IN2}	—	6	pF
Input Capacitance ($\overline{RAS}$, $\overline{CS}$, $\overline{W}$)	C_{IN3}	—	7	pF
Output Capacitance (Q)	C_{OUT}	—	7	pF

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC} = 5.0V \pm 10\%$, See notes 1, 2)

Parameter	Symbol	KM41C1002A-7		KM41C1002A-8		KM41C1002A-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	130		150		180		ns	
Read-modify-write cycle time	t_{RWC}	155		175		210		ns	
Access time from $\overline{RAS}$	t_{RAC}		70		80		100	ns	3,4,11
Access time from $\overline{CS}$	t_{CAC}		20		20		25	ns	3,4,5
Access time from column address	t_{AA}		35		40		50	ns	3,11
$\overline{CS}$ to output in Low-Z	t_{CLZ}	5		5		5		ns	3,12
Output buffer turn-off delay	t_{OFF}	0	25	0	25	0	30	ns	7
Output data hold time from column address	t_{AOH}	5		5		5		ns	
Output data enable time from $\overline{W}$	t_{OW}		45		50		70	ns	
Output data hold time from $\overline{W}$	t_{WOH}	0		0		0		ns	
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	50		60		70		ns	
$\overline{RAS}$ pulse width	t_{RAS}	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		20		25		ns	
$\overline{CS}$ hold time	t_{CSH}	70		80		100		ns	
$\overline{CS}$ pulse width	t_{CS}	20	10,000	20	10,000	25	10,000	ns	
$\overline{RAS}$ to $\overline{CS}$ delay time	t_{RCD}	20	50	25	60	25	75	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	35	20	40	20	50	ns	11
$\overline{CS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		15		15		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		20		20		ns	
Write address hold time referenced to $\overline{RAS}$	t_{AWR}	55		65		75		ns	6

STANDARD OPERATION (Continued)

Parameter	Symbol	KM41C1002A-7		KM41C1002A-8		KM41C1002A-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Column address hold time referenced to $\overline{RAS}$	t_{AR}	85		95		115		ns	6
Column address to $\overline{RAS}$ lead time	t_{RAL}	35		40		50		ns	
Column address hold time referenced to $\overline{RAS}$ rise	t_{AH}	10		10		10		ns	
Last write to column address delay time	t_{LWAD}	20	30	25	35	25	45	ns	
Last write to column address hold time	t_{AHLW}	65		75		95		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold time referenced to $\overline{CS}$	t_{RCH}	0		0		0		ns	9
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	9
Write command hold time	t_{WCH}	15		20		20		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	55		65		75		ns	6
Write command pulse width	t_{WP}	15		20		20		ns	
Write command inactive time	t_{WI}	10		10		10		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		20		25		ns	
Write command to $\overline{CS}$ lead time	t_{CWL}	20		20		25		ns	
Data-in set-up time	t_{DS}	0		0		0		ns	10
Data-in hold time	t_{DH}	15		20		20		ns	10
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	55		65		75		ns	6
Refresh period (512 cycles)	t_{REF}		8		8		8	ms	
Write command set-up time	t_{WCS}	0		0		0		ns	8
$\overline{CS}$ to $\overline{W}$ delay time	t_{CWD}	20		20		25		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	70		80		100		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	35		40		50		ns	8
STATIC COLUMN MODE									
Static column mode cycle time	t_{SC}	40		45		55		ns	
Static column mode read-write cycle time	t_{SRWC}	70		80		100		ns	
$\overline{RAS}$ pulse width (static column mode)	t_{RASC}	70	100,000	80	100,000	100	100,000	ns	
$\overline{CS}$ pulse width (static column mode)	t_{CSC}	20	100,000	20	100,000	25	100,000	ns	
$\overline{CS}$ precharge time (static column mode)	t_{CP}	10		10		10		ns	
$\overline{CS}$-BEFORE-$\overline{RAS}$ REFRESH									
$\overline{CS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10		10		10		ns	
$\overline{CS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	20		25		30		ns	
$\overline{RAS}$ precharge to $\overline{CS}$ hold time	t_{RPC}	10		10		10		ns	
Refresh couner test $\overline{CS}$ precharge time	t_{CPT}	35		40		50		ns	

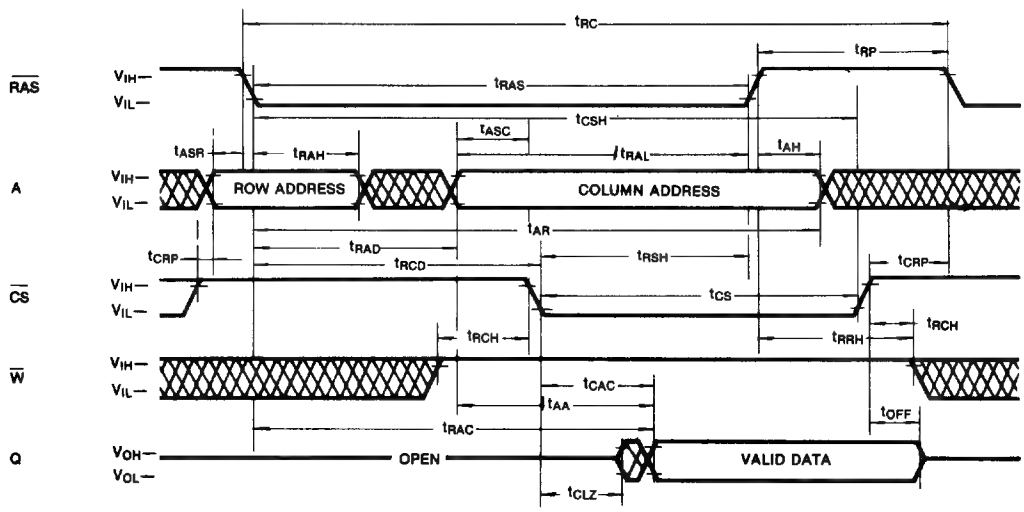
1. An initial pause of 200 μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved. Before using the internal refresh counter, 8 $\overline{CAS}$-before-$\overline{RAS}$ refresh initialization cycles are required (instead of 8 $\overline{RAS}$ cycles).
2. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} (min) and V_{IL} (max), and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.

NOTES (Continued)

5. Assumes that $t_{RCD} \geq t_{RCD}(max)$.
6. t_{AWR}, t_{WCR}, t_{DHR} are referenced to $t_{RAD}(max)$.
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}(min)$ the cycle is an early write cycle and the data output will remain open circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}(min)$ and $t_{RWD} \geq t_{RWD}(min)$ and $t_{AWD} \geq t_{AWD}(min)$, then the cycle is a read-write cycle and the data output will contain data read from the selected cell. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycles.
10. These parameters are referenced to the $\overline{CS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the $t_{RAD}(max)$ limit insures that $t_{RAC}(max)$ can be met, $t_{RAD}(max)$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD}(max)$ limit, then access time is controlled by t_{AA}.
12. Operation within the $t_{LWAD}(max)$ limit insures that $t_{ALW}(max)$ can be met. $t_{LWAD}(max)$ is specified as a reference point only. If t_{LWAD} is greater than the specified $t_{LWAD}(max)$ limit, then access time is controlled by t_{AA}.
13. Normal operation requires the "T.F" pin to be connected to V_{SS} or TTL logic low level or left unconnected on the printed wiring board.
14. When the "T.F" pin is connected to a defined positive voltage, the internal test function may be activated. Contact Samsung for specific operational details of the "test function."

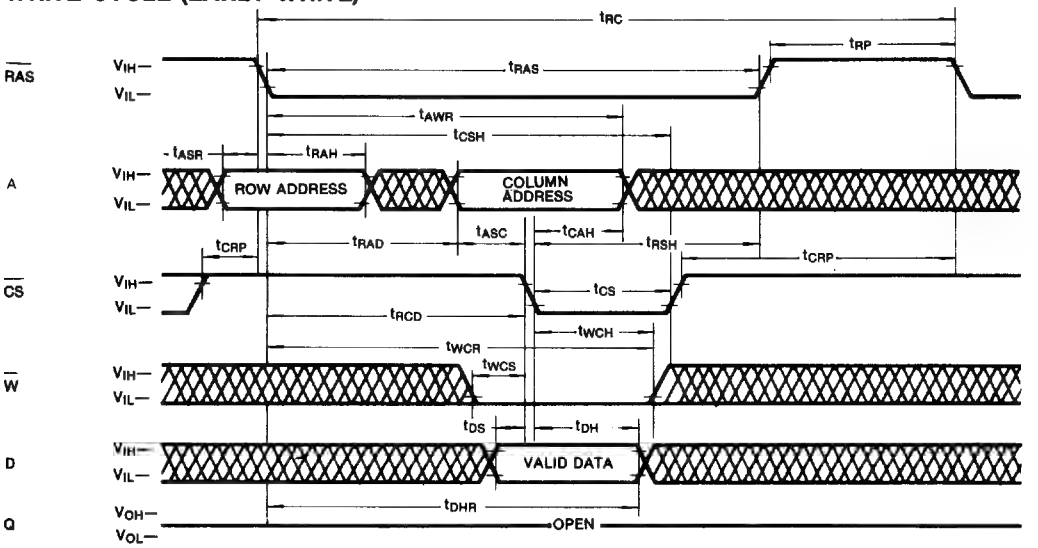
TIMING DIAGRAMS

READ CYCLE

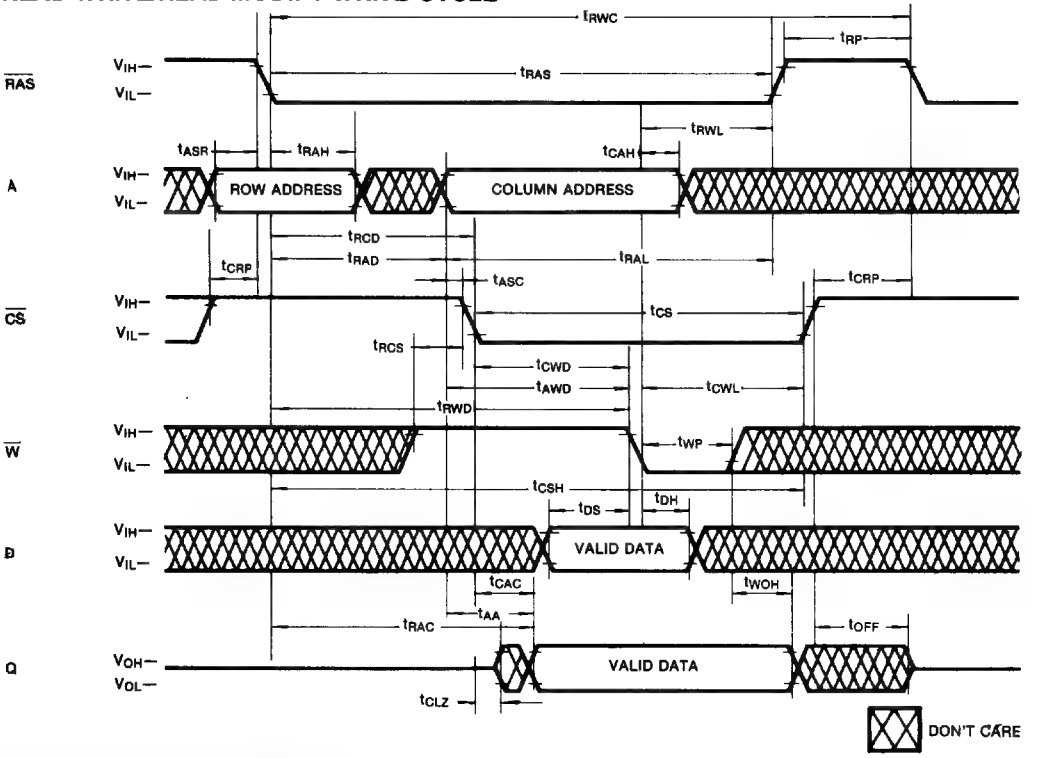


TIMING DIAGRAMS (Continued)

WRITE CYCLE (EARLY WRITE)

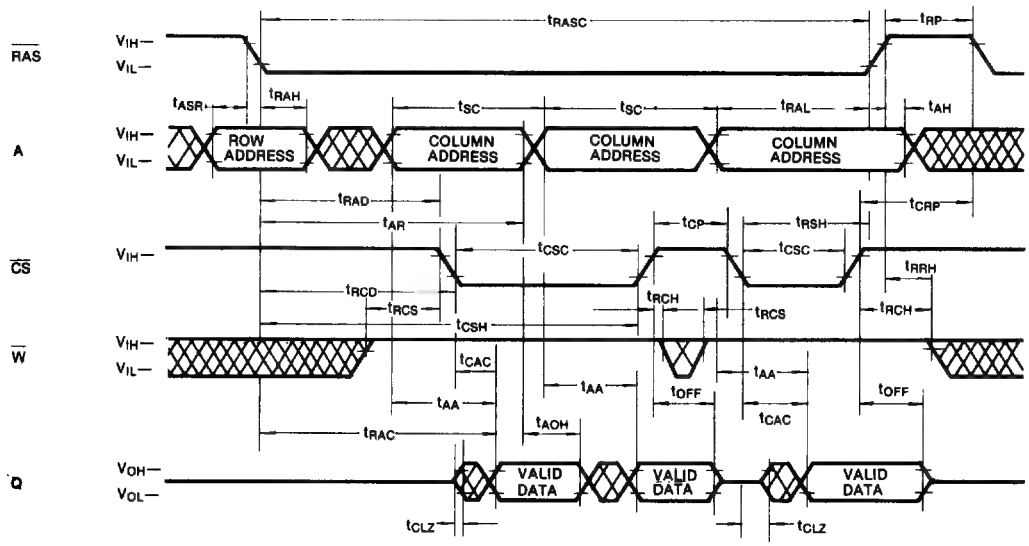


READ-WRITE/READ-MODIFY-WRITE CYCLE

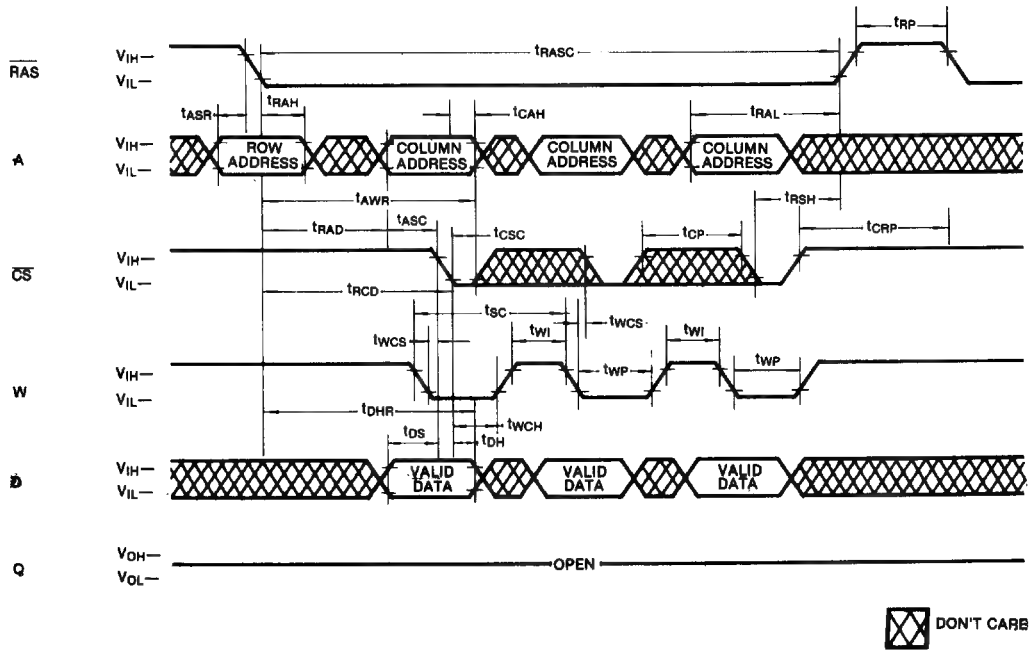


TIMING DIAGRAMS (Continued)

STATIC COLUMN MODE READ CYCLE

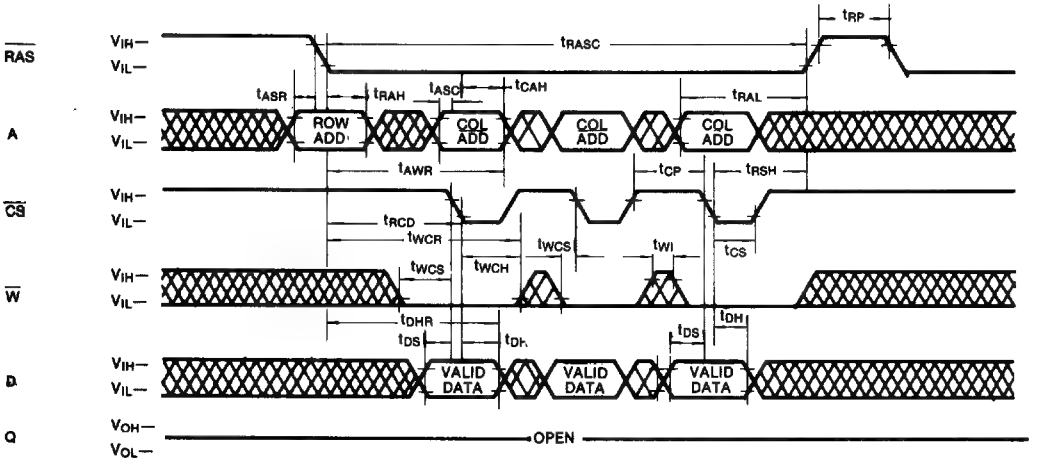


STATIC COLUMN MODE WRITE CYCLE (W controlled early write)

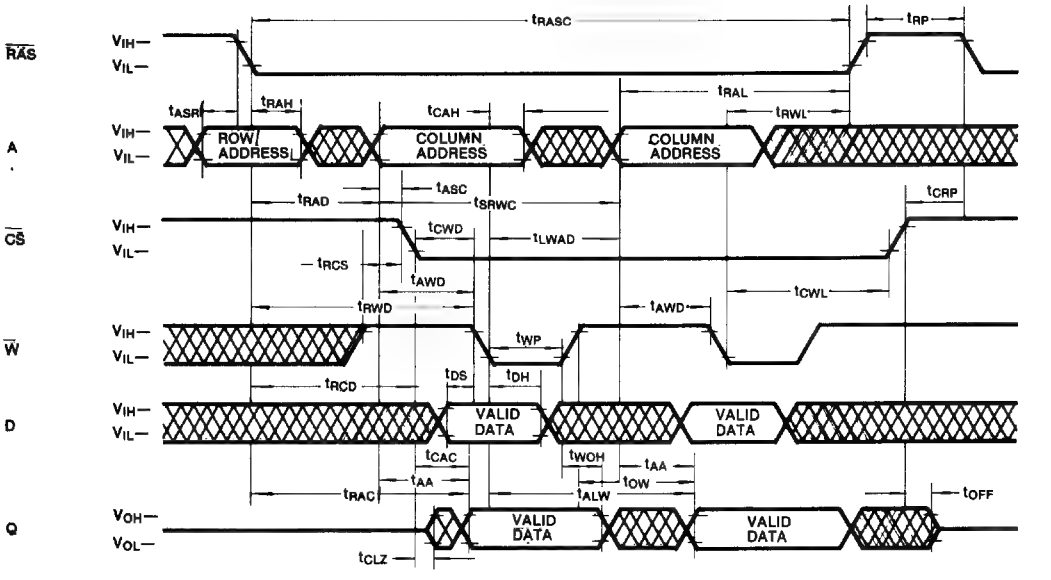


TIMING DIAGRAMS (Continued)

STATIC COLUMN MODE WRITE CYCLE ($\overline{CS}$ controlled early write)

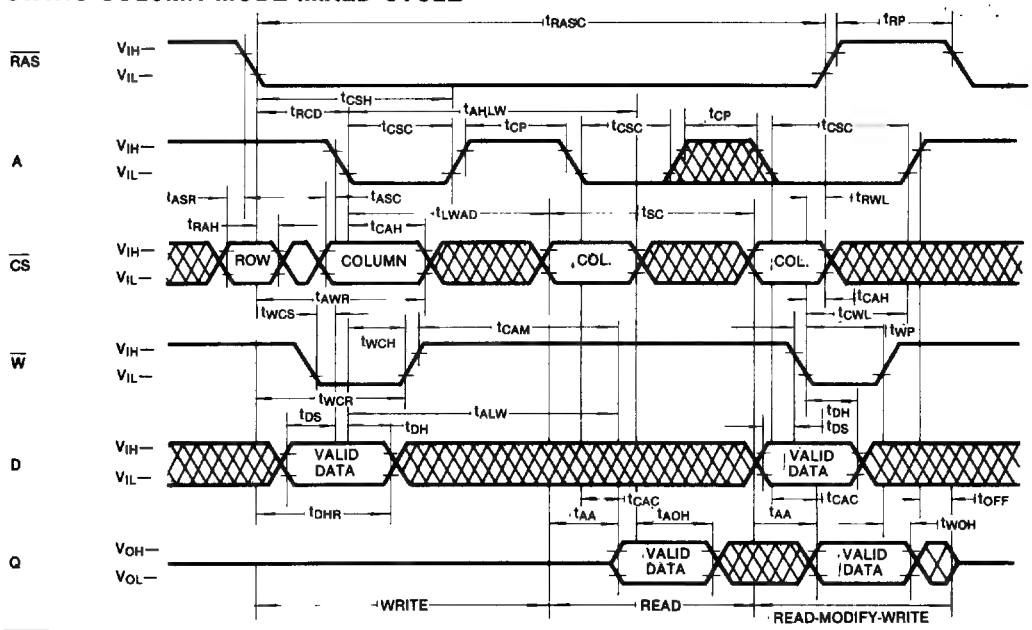


STATIC COLUMN MODE READ-WRITE CYCLE



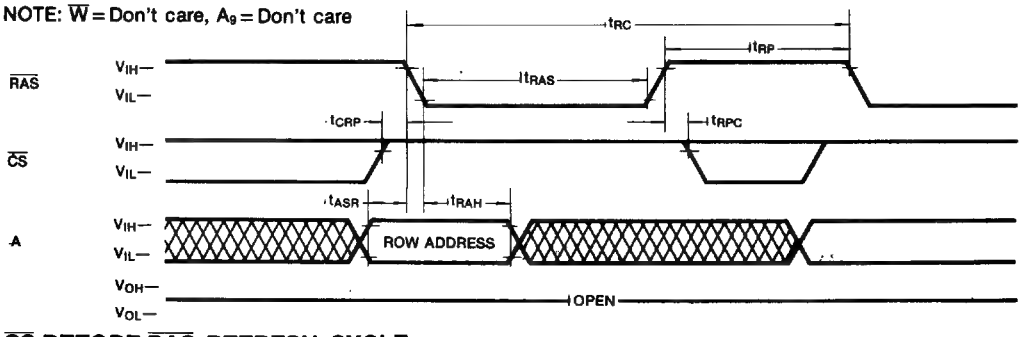
TIMING DIAGRAMS (Continued)

STATIC COLUMN MODE MIXED CYCLE



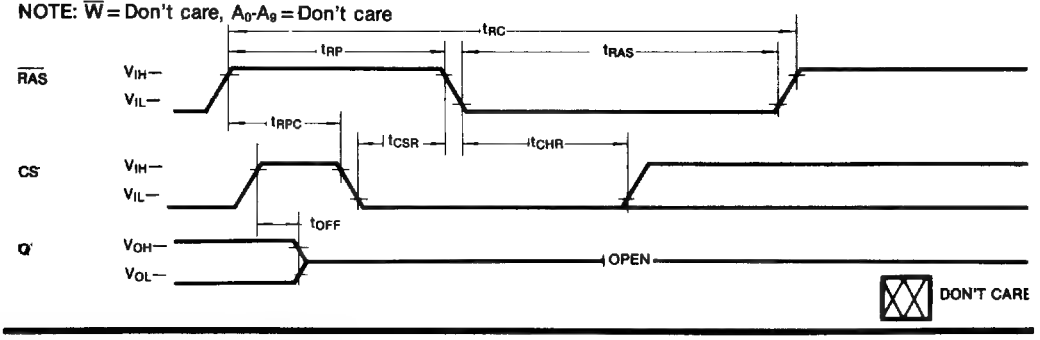
RAS-ONLY REFRESH CYCLE

NOTE: W = Don't care, A_9 = Don't care



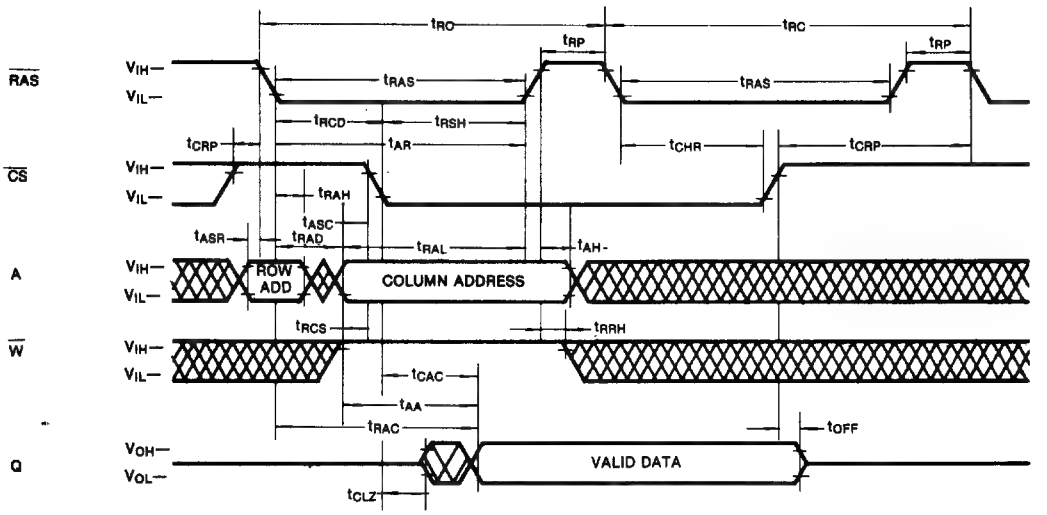
CS-BEFORE-RAS REFRESH CYCLE

NOTE: W = Don't care, A_0-A_9 = Don't care

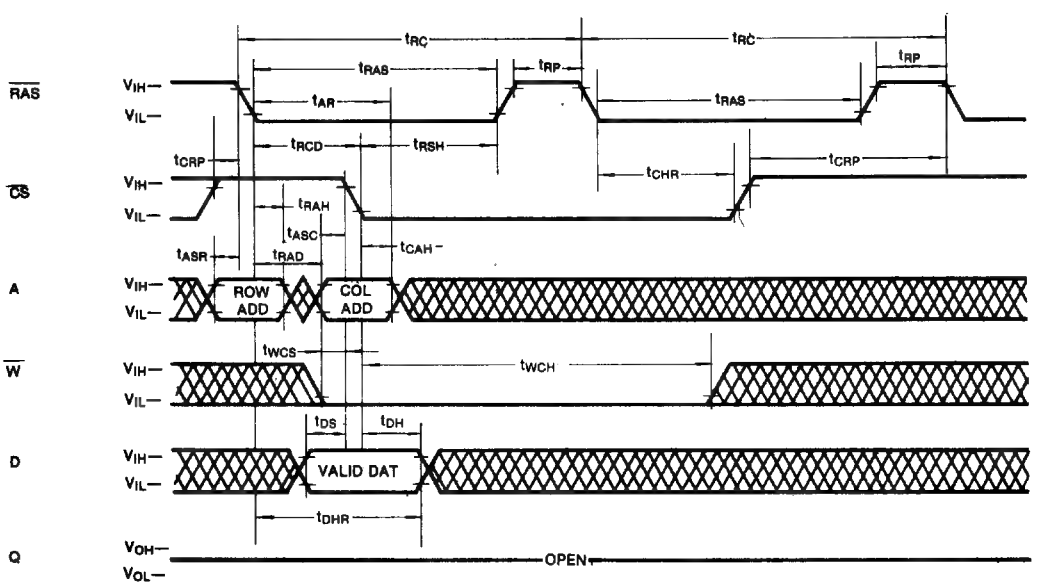


TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)



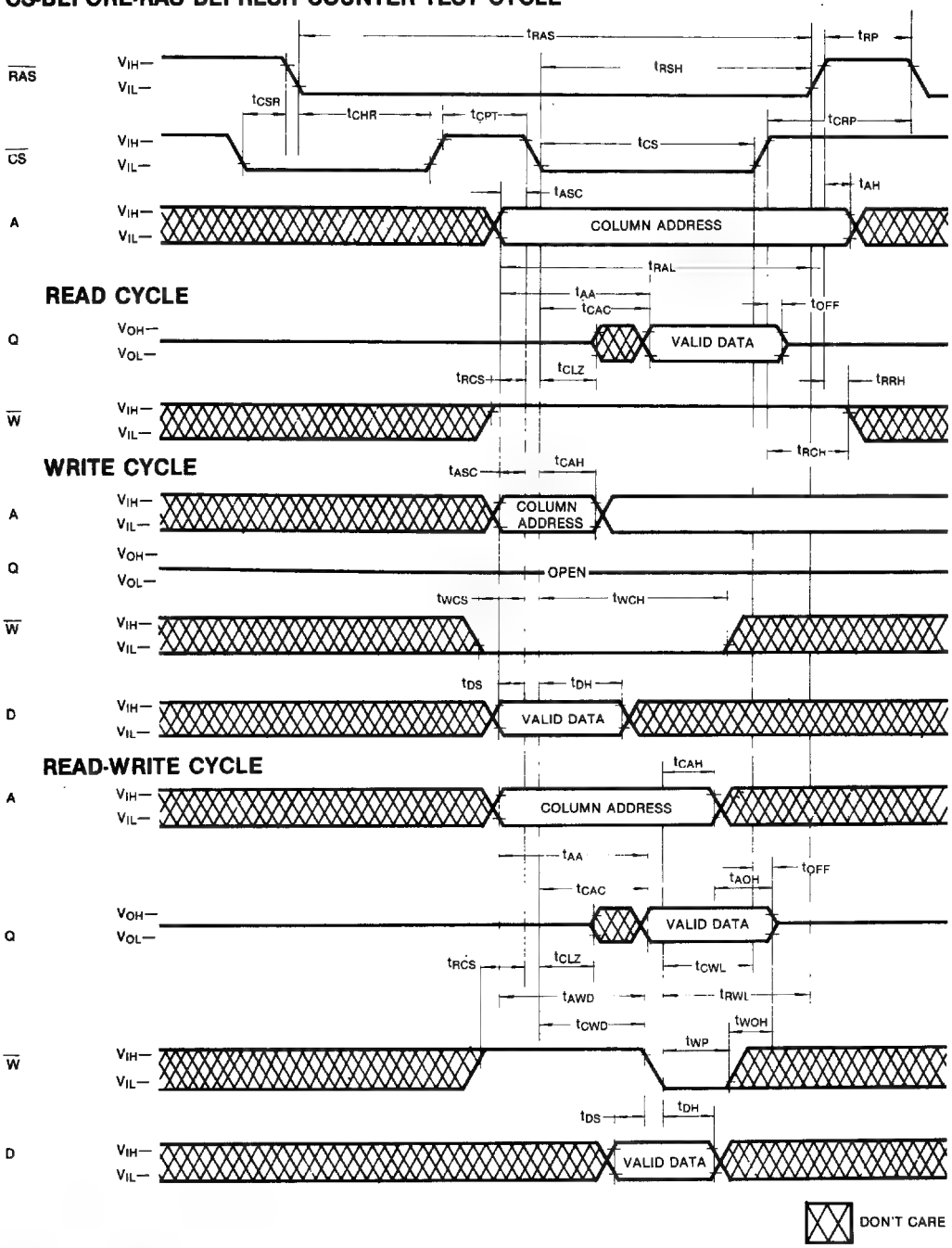
HIDDEN REFRESH CYCLE (WRITE)



DON'T CARE

TIMING DIAGRAMS (Continued)

$\overline{CS}$-BEFORE-$\overline{RAS}$ BEFRESH COUNTER TEST CYCLE



KM41C1002A OPERATION

Device Operation

The KM41C1002A contains 1,048,576 memory locations. Twenty address bits are required to address a particular memory location. Since the KM41C1002A has only 10 address input pins, time multiplexed addressing is used to input 10 row and 10 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{RAS}$), the column address strobe ($\overline{CS}$) and the valid row and column address inputs.

Operation of the KM41C1002A begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{CS}$ remains high. Then the address on the 10 address input pins is changed from a row address to a column address and is strobed in by $\overline{CS}$. This is the beginning of any KM41C1002A cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both $\overline{RAS}$ and $\overline{CS}$ have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time (tRP) requirement.

$\overline{RAS}$ and $\overline{CS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CS}$ pulse widths are specified by tRAS(min) and tCAS(min) respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CS}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, tRP, has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM41C1002A begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input($\overline{W}$) high during a $\overline{RAS}$/$\overline{CS}$ cycle. The access time is normally specified with respect to the falling edge of $\overline{RAS}$. But the access time also depends on the falling edge of $\overline{CS}$ and on the valid column address transition.

If $\overline{CS}$ goes low before tRCD(max) and if the column address is valid before tRAD(max) then the access time to valid data is specified by tRAC(min). However, if $\overline{CS}$ goes low after tRCD(max) or if the column address becomes valid after tRAD(max), access is specified by tCAC or tAA. In order to achieve the minimum access time, tRAC(min), it is necessary to meet both tRCD(max) and tRAD(max).

Write

The KM41C1002A can perform early write, late write and read-modify-write cycles. The differece between these cycles is in the state of data-out and is determined by the timing relationship between $\overline{W}$ and $\overline{CS}$. In any type of write cycle, Data-in must be valid at or before the falling edge of $\overline{W}$ or $\overline{CS}$, whichever is later.

Early Write: An early write cycle is performed by bringing $\overline{W}$ low before $\overline{CS}$. The data at the data input pin (D) is written into the addressed memory cell. Throughout the early write cycle the output remains in the Hi-Z state. This cycle is good for common I/O applications because the data-in and data-out pins may be tied together without bus contention.

Read-Modify-Write: In this cycle, valid data from the addressed cell appears at the output before and during the time that data is being written into the same cell location. This cycle is achieved by bringing $\overline{W}$ low after $\overline{CS}$ and meeting the data sheet read-modify-write cycle timing requirements. This cycle requires using a separate I/O to avoid bus contention.

Late Write: If $\overline{W}$ is brought low after $\overline{CS}$, a late write cycle will occur. The late write cycle is very similar to the read-modify-write cycle except that the timing parameters tCWD and tAWD are not necessarily met. The state of data-out is indeterminate since the output can be either Hi-Z or contain data depending on the timing conditions. This cycle requires a separate I/O to avoid bus contention.

Data Output

The KM41C1002A has a tri-state output buffer which is controlled by $\overline{CS}$. Whenever $\overline{CS}$ is high (VIH) the output is in the high impedance (Hi-Z) state. In any cycle in which valid data appears at the output, the output goes into the low impedance state in a time specified by tCLZ after the falling edge of $\overline{CS}$. Invalid data may be present at the output during the time after tCLZ and before the valid data appears at the output. The timing parameters tCAC, tRAC and tAA specify when the valid data will be present at the output. The valid data remains at the output until $\overline{CS}$ returns high. This is true even if a new $\overline{RAS}$ cycle occurs (as in hidden refresh). Each of the KM41C1002A operating cycles is listed below after the corresponding output state produced by the cycle.

DEVICE OPERATION (Continued)

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Static Column Mode Read, Static Column Read-Modify-Write.

Hi-Z Output State: Early Write, $\overline{RAS}$-only Refresh, Static Column Mode Write, $\overline{CS}$-before-$\overline{RAS}$ Refresh, $\overline{CS}$-only cycle.

Indeterminate Output State: Delayed Write

Refresh

The data in the KM41C1002A is stored on a tiny capacitor within each memory cell. Due to leakage the data may leak off after a period of time. To maintain data integrity it is necessary to refresh each of the rows every 8 ms. There are several ways to accomplish this.

$\overline{RAS}$-Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{RAS}$ while $\overline{CS}$ remains high. This cycle must be repeated for each of the 512 row addresses, (A0-A8). The state of address A9 is ignored during refresh.

$\overline{CS}$-before-$\overline{RAS}$ Refresh: The KM41C1002A has $\overline{CS}$-before-$\overline{RAS}$ on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{CS}$ is held low for the specified set up time (tCSR) before $\overline{RAS}$ goes low, the on-chip refresh circuitry is enabled. An internal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next $\overline{CS}$-before-$\overline{RAS}$ refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the $\overline{CS}$ active time and cycling $\overline{RAS}$. The KM41C1002A hidden refresh cycle is actually a $\overline{CS}$-before-$\overline{RAS}$ refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter.

Other Refresh Methods: It is also possible to refresh the KM41C1002A by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in that row are automatically refreshed. There are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{RAS}$-only or $\overline{CS}$-before-$\overline{RAS}$ refresh is the preferred method.

$\overline{CS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle

A special timing sequence using the $\overline{CS}$-before-$\overline{RAS}$ refresh counter test cycle provides a convenient method of verifying the functionality of the $\overline{CS}$-before-$\overline{RAS}$ refresh activated circuitry. The cycle begins as a $\overline{CS}$-before-$\overline{RAS}$ refresh operation. Then, if $\overline{CS}$ is brought high and then low again while $\overline{RAS}$ is held low, the read and write operations are enabled. In this mode, the row address bits A0 through A8 are supplied by the on-chip refresh counter. The A9 bit is set low internally.

Static Column Mode

Static Column Mode allows high speed read write or read-modify-write random access to all the memory cells within a selected row. Operation within a selected row is similar to a static RAM. The read, write or readmodify-write cycles may be mixed in any order.

A Static Column mode read cycle starts as a normal cycle. Additional cells within the selected row are written by applying a new column address while $\overline{W}$ = VIH and $\overline{RAS}$ = VIL.

A Static Column mode write cycle starts as a normal cycle. Additional cells within the selected row are written by applying a new column address while $\overline{RAS}$ = VIL and toggiling either $\overline{W}$ or $\overline{CS}$. The data is written into the cell triggered by the latter falling edge of $\overline{W}$ or $\overline{CS}$.

Power-up

If $\overline{RAS} = V_{SS}$ during power-up, the KM41C1002A could begin an active cycle. This condition results in higher than necessary current demands from the power supply during power-up. It is recommended that $\overline{RAS}$ and $\overline{CS}$ track with V_{CC} during power-up or be held at a valid VIH in order to minimize the power-up current.

An initial pause of 200 μsec is required after power-up followed by 8 initialization cycles before proper device operation is assured. Eight initialization cycles are also required after any 8 msec period in which there are no $\overline{RAS}$ cycles. An initialization cycle is any cycle in which $\overline{RAS}$ is cycled.

DEVICE OPERATION (Continued)

Termination

The lines from the TTL driver circuits to the KM41C1002A inputs act like unterminated transmission lines resulting in significant overshoot and undershoot at the inputs. To minimize overshoot it is advisable to terminate the input lines and to keep them as short as possible. Although either series or parallel termination may be used, series termination is generally recommended since it is simple and draws no additional power. It consists of a resistor in series with the input line placed close to the KM41C1002A input pin. The optimum value depends on the board layout. It must be determined experimentally and is usually in the range of 20 to 40 ohms.

Board Layout

It is important to lay out the power and ground lines on memory boards in such a way that switching transient effects are minimized. The recommended methods are gridded power and ground lines or separate power and ground planes. The power and ground lines act like transmission lines to the high frequency transients generated by DRAMS. The impedance is minimized if all the power supply traces to all the DRAMS run both horizontally and vertically and are connected at each intersection or better yet if power and ground planes are used.

Decoupling

The importance of proper decoupling can not be over emphasized. Excessive transient noise or voltage droop on the V_{CC} line can cause loss of data integrity (soft errors). It is recommended that the total combined voltage changes over time in the VCC to VSS voltage (measured at the device pins) should not exceed 500mV.

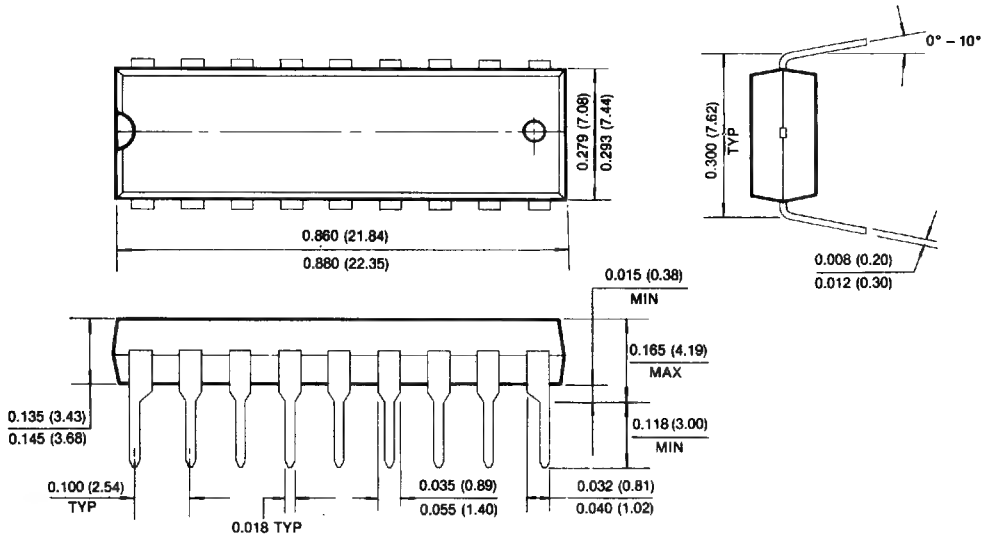
A high frequency 0.3μF ceramic decoupling capacitor should be connected between the V_{CC} and ground pins of each KM41C1002A using the shortest possible traces. These capacitors act as a low impedance shunt for the high frequency switching transients generated by the KM41C1002A and they supply much of the current used by the KM41C1002A during cycling.

In addition, a large tantalum capacitor with a value of 47μF to 100μF should be used for bulk decoupling to recharge the 0.3μF capacitors between cycles, thereby reducing power line droop. The bulk decoupling capacitor should be placed near the point where the power traces meet the power grid or power plane. Even better results may be achieved by distributing more than one tantalum capacitor around the memory array.

PACKAGE DIMENSIONS

18-LEAD PLASTIC DUAL IN-LINE PACKAGE

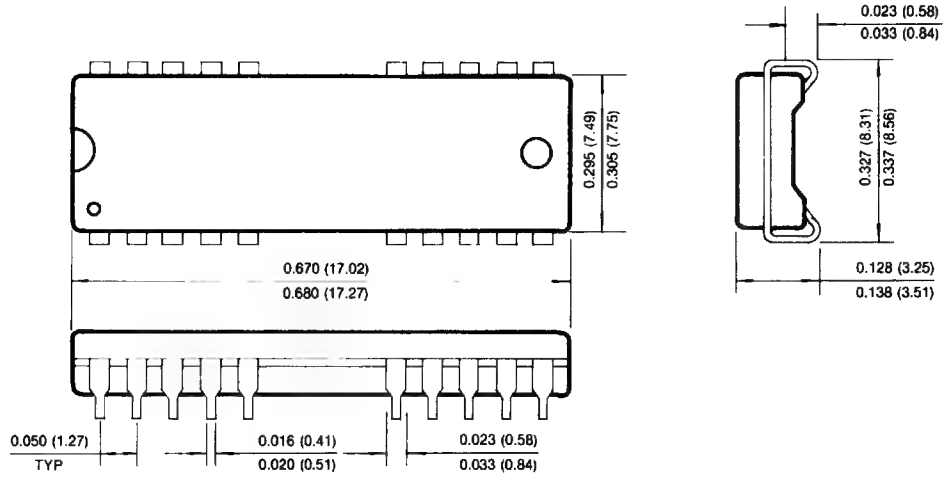
Units: Inches (Millimeters)



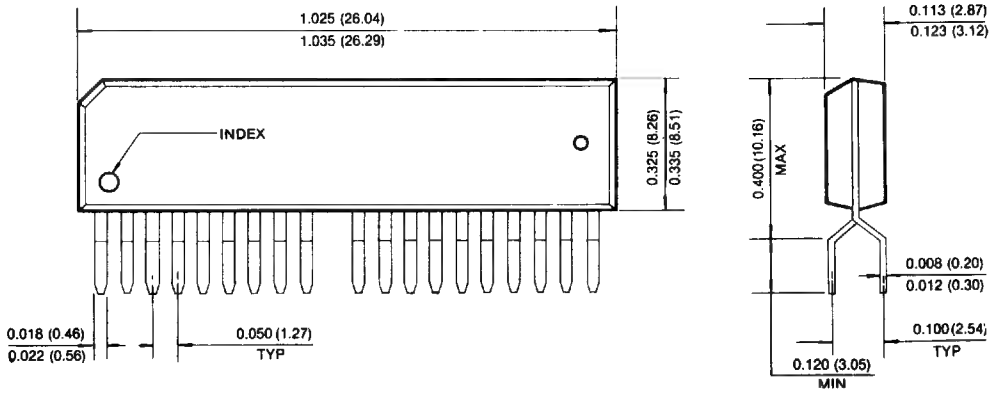
PACKAGE DIAGRAMS (Continued)

20-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



20-PIN PLASTIC ZIGZAG-IN-LINE PACKAGE



256K x 4 Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

- **Performance range:**

	t_{RAC}	t_{CAC}	t_{RC}
KM44C256A- 8	80ns	20ns	150ns
KM44C256A-10	100ns	25ns	180ns
KM44C256A-12	120ns	30ns	220ns

- **Fast Page Mode operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **TTL compatible inputs and output**
- **Early Write or output Enable Controlled Write**
- **Single +5V ± 10% power supply**
- **512 cycles/8ms refresh**
- **JEDEC standard pinout**
- **Available in Plastic DIP, SOJ and ZIP**

GENERAL DESCRIPTION

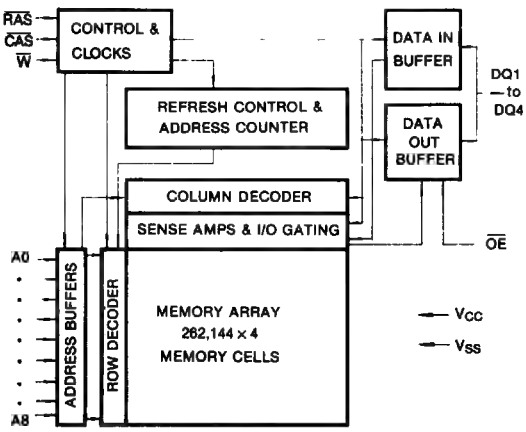
The Samsung KM44C256A is a CMOS high speed 262,144 x 4 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes and mini computers, graphics and high performance microprocessor systems.

The KM44C256A features Fast Page Mode operation which allows high speed random access of memory cells within the same row.

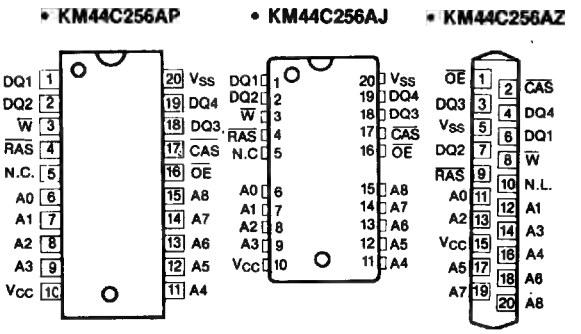
$\overline{CAS}$-before-$\overline{RAS}$ Refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only Refresh. All inputs and output are fully TTL compatible.

The KM44C256A is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Pin Name	Pin Function
A_0-A_8	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Output Enable
DQ_1-DQ_4	Data In/Data Out
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection
N.L.	No Lead

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−1 to +7.0	V
Storage Temperature	T_{stg}	−55 to +150	°C
Power Dissipation	P_D	600	mW
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC}+1	V
Input Low Voltage	V_{IL}	−1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
OPERATING CURRENT* ($\overline{RAS}$, $\overline{CAS}$, Address cycling @t_{RC} = min.)	KM44C256A-8 KM44C256A-10 KM44C256A-12	I_{CC1}	—	75 65 55	mA
STANDBY CURRENT ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		I_{CC2}	—	2	mA
$\overline{RAS}$-ONLY REFRESH CURRENT* ($\overline{CAS}$ = V_{IH}, $\overline{RAS}$ cycling @t_{RC} = min.)	KM44C256A-8 KM44C256A-10 KM44C256A-12	I_{CC3}	—	75 65 55	mA
FAST PAGE MODE CURRENT* ($\overline{CAS}$ = V_{IH}, $\overline{RAS}$ cycling; @t_{PC} = min.)	KM44C256A-8 KM44C256A-10 KM44C256A-12	I_{CC4}	—	55 45 35	mA
STANDBY CURRENT ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} − 0.2V)		I_{CC5}	—	1	mA
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CURRENT* ($\overline{RAS}$ and $\overline{CAS}$ cycling @t_{RC} = min.)	KM44C256A-8 KM44C256A-10 KM44C256A-12	I_{CC6}	—	75 65 55	mA
INPUT LEAKAGE CURRENT (Any input 0 ≤ V_{IN} ≤ 6.5V, all other pins not under test = 0 volts.)		I_{IL}	−10	10	μA
OUTPUT LEAKAGE CURRENT (Data out is disabled, 0V ≤ V_{OUT} ≤ 5.5V		I_{OL}	−10	10	μA
OUTPUT HIGH VOLTAGE LEVEL (I_{OH} = −5mA)		V_{OH}	2.4	—	V
OUTPUT LOW VOLTAGE LEVEL (I_{OL} = 4.2mA)		V_{OL}	—	0.4	V

*Note: I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current.

CAPACITANCE (T_A = 25°C)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A_0-A_8)	C_{IN1}	—	6	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{OE}$)	C_{IN2}	—	7	pF
Output Capacitance (DQ_1-DQ_4)	C_{DQ}	—	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, V_{CC} = 5.0V ± 10%, See notes 1, 2)

Parameter	Symbol	KM44C256A-8		KM44C256A-10		KM44C256A-12		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	150		180		220		ns	
Read-modify-write cycle time	t_{RWC}	205		245		295		ns	
Fast page mode cycle time	t_{PC}	50		60		75		ns	
Fast page mode read-write cycle time	t_{PRWC}	105		125		145		ns	
Access time from $\overline{RAS}$	t_{RAC}		80		100		120	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		20		25		30	ns	3,4,5
Access time from column address	t_{AA}		40		50		60	ns	3,11
Access time from $\overline{CAS}$ precharge	t_{CPA}		45		55		65	ns	3
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	5		5		5		ns	3
Output buffer turn-off delay	t_{OFF}	0	25	0	30	0	35	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	60		70		90		ns	
$\overline{RAS}$ pulse width	t_{RAS}	80	10,000	100	10,000	120	10,000	ns	
$\overline{RAS}$ pulse width (fast page mode)	t_{RASP}	80	100,000	100	100,000	120	100,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		25		30		ns	
$\overline{CAS}$ hold time	t_{CSH}	80		100		120		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	25	10,000	30	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	25	60	25	75	25	90	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	20	40	20	50	20	60	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		ns	11
$\overline{CAS}$ precharge time (fast page mode)	t_{CP}	10		10		15		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	15		15		15		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	KM44C256A-8		KM44C256A-10		KM44C256A-12		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Column address hold time	t_{CAH}	20		20		25		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	65		75		90		ns	6
Column address to $\overline{RAS}$ lead time	t_{RAL}	40		50		60		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	9
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	9
Write command hold time	t_{WCH}	20		20		25		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	65		75		90		ns	6
Write command pulse width	t_{WP}	20		20		25		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		25		30		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	20		25		30		ns	
Data set-up time	t_{DS}	0		0		0		ns	10
Data hold time	t_{DH}	20		20		25		ns	10
Data hold time referenced to $\overline{RAS}$	t_{DHR}	65		75		90		ns	6
Refresh period	t_{REF}		8		8		8	ms	
Write command set-up time	t_{WCS}	0		0		0		ns	8
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	50		60		70		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	110		135		160		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	70		85		100		ns	8
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	t_{CSR}	10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	t_{CHR}	30		30		30		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	10		10		10		ns	
$\overline{CAS}$ precharge time ($\overline{CAS}$ before $\overline{RAS}$ counter test cycle)	t_{CPT}	40		50		60		ns	
$\overline{RAS}$ hold time referenced to $\overline{OE}$	t_{ROH}	20		20		20		ns	
$\overline{OE}$ access time	t_{OEA}		20		25		30	ns	
$\overline{OE}$ to data delay	t_{OED}	20		25		30		ns	
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	0	20	0	25	0	30	ns	
$\overline{OE}$ command hold time	t_{OEH}	20		25		30		ns	

NOTES

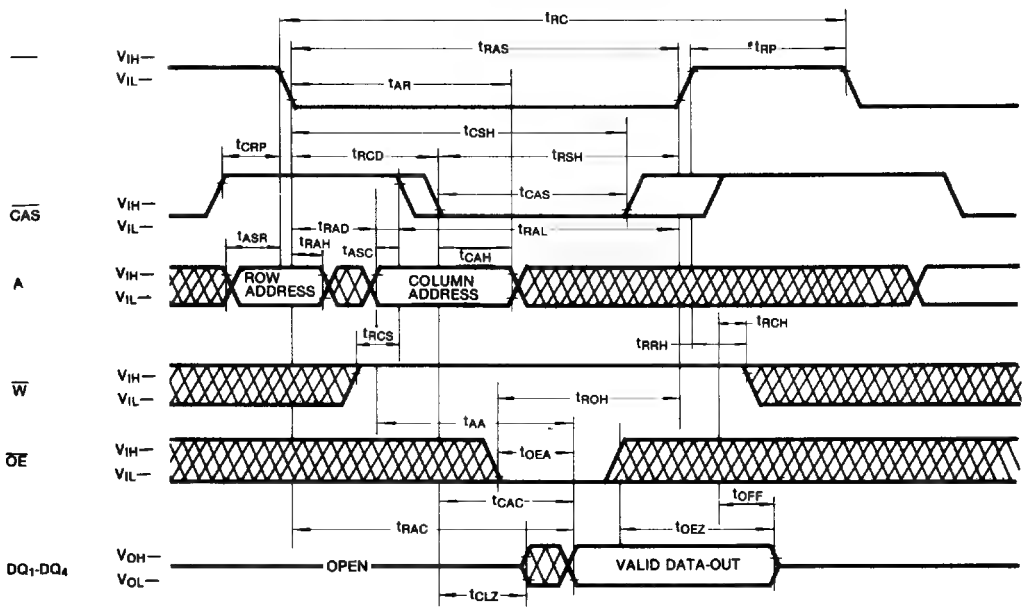
1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.

NOTES (Continued)

5. Assumes that $t_{RCD} \geq t_{RCD}(max)$.
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to $t_{RAD}(max)$.
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} > t_{WCS}(min)$ the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}(min)$, $t_{RWD} \geq t_{RWD}(min)$ and $t_{AWD} \geq t_{AWD}(min)$, then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the $t_{RAD}(max)$ limit insures that $t_{RCD}(max)$ can be met. $t_{RAD}(max)$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD}(max)$ limit, then access time is controlled by t_{AA}.

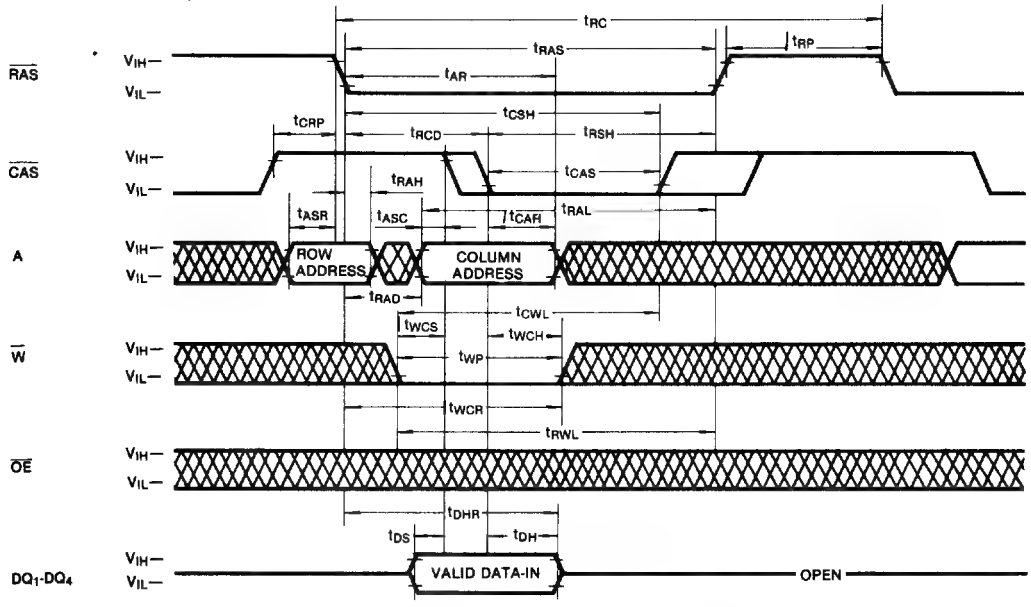
TIMING DIAGRAMS

READ CYCLE

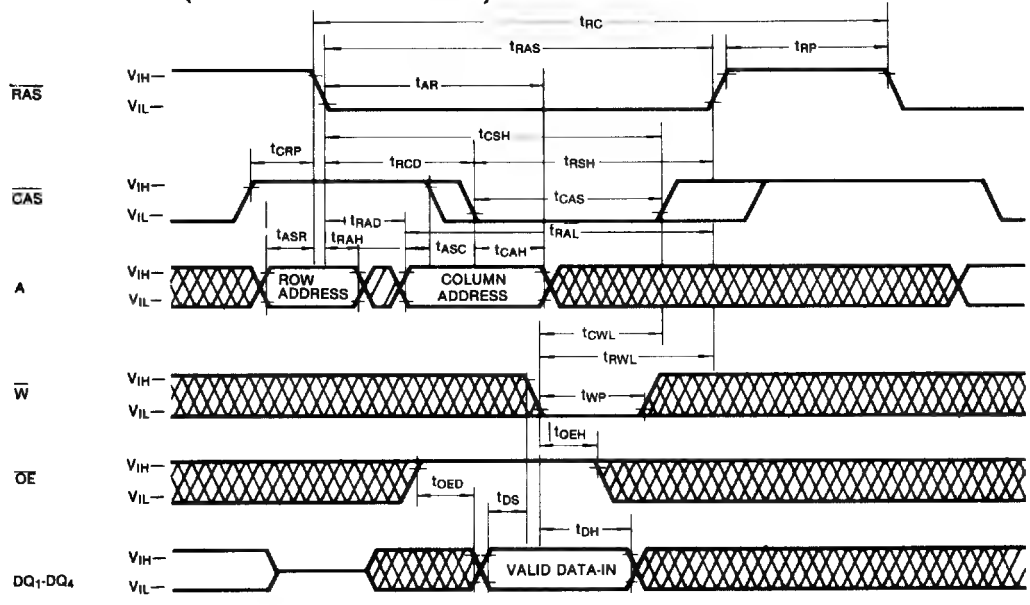


TIMING DIAGRAMS (Continued)

WRITE CYCLE (EARLY WRITE)



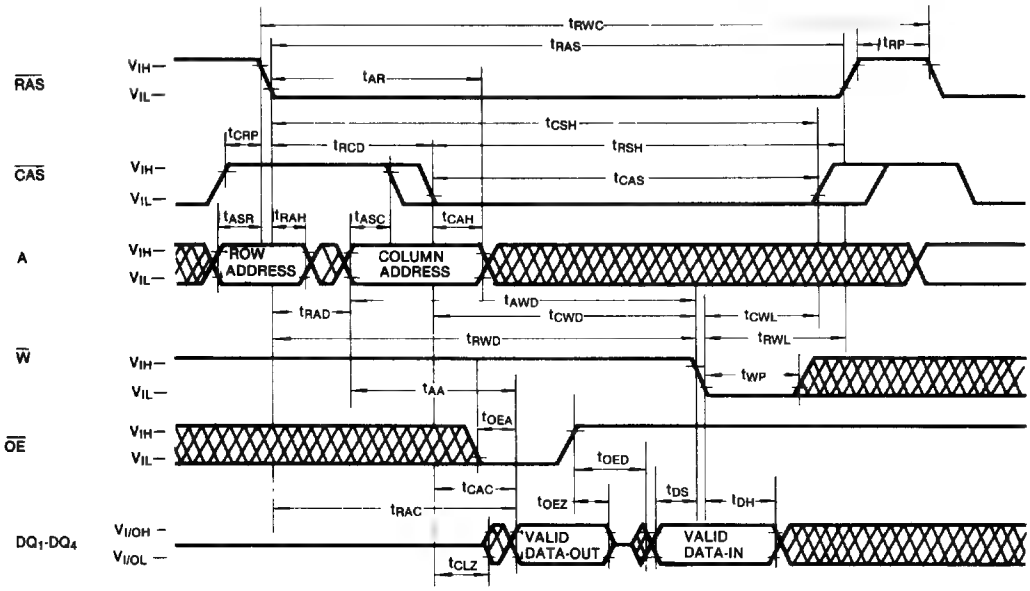
WRITE CYCLE (OE CONTROLLED WRITE)



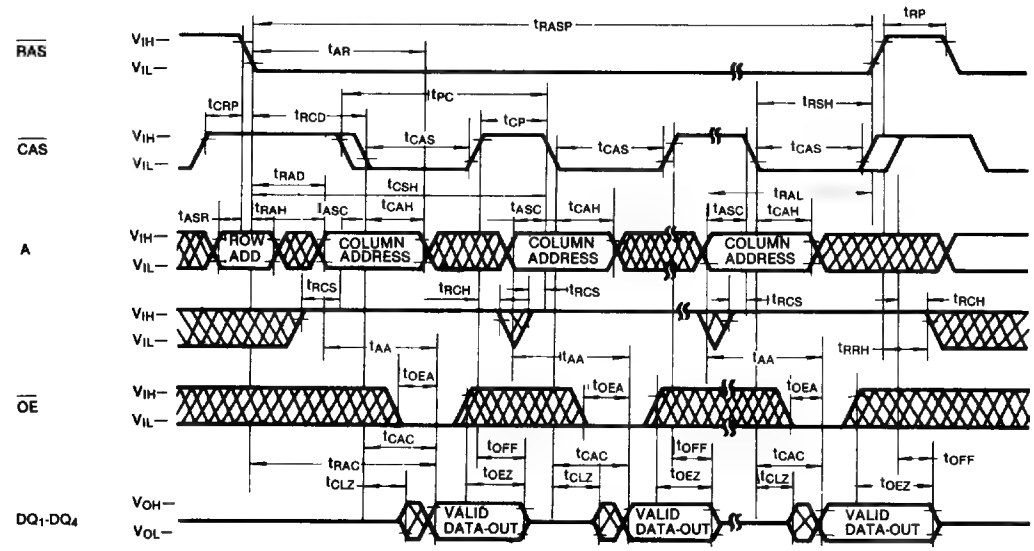
DON'T CARE

TIMING DIAGRAMS (Continued)

READ-MODIFY-WRITE

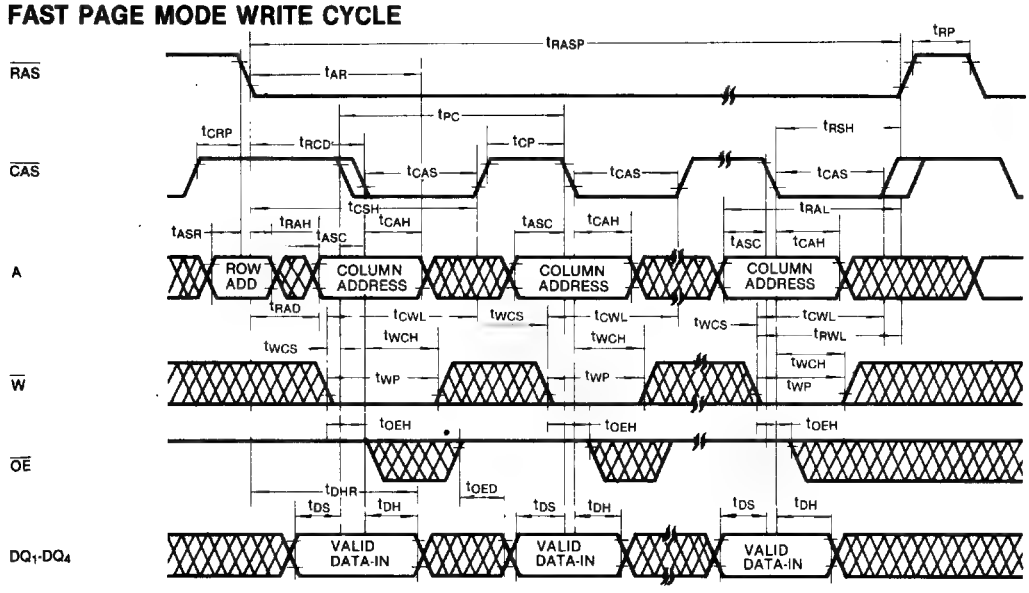


FAST PAGE MODE READ CYCLE

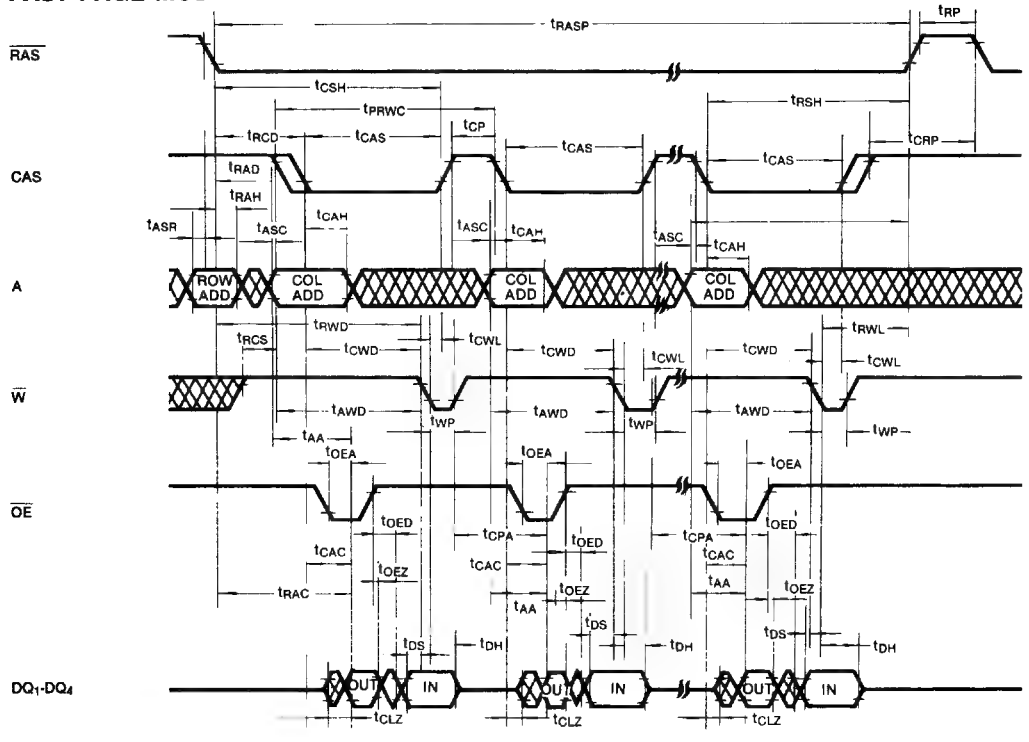


DON'T CARE

FAST PAGE MODE WRITE CYCLE



FAST PAGE MODE READ-MODIFY-WRITE

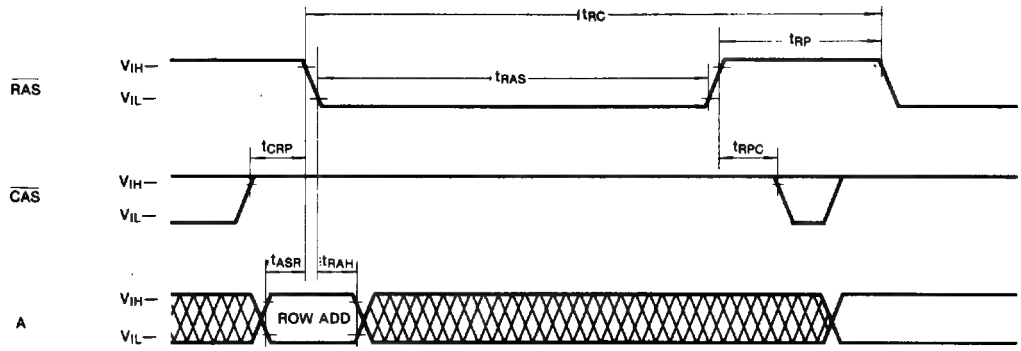


DON'T CARE

TIMING DIAGRAMS (Continued)

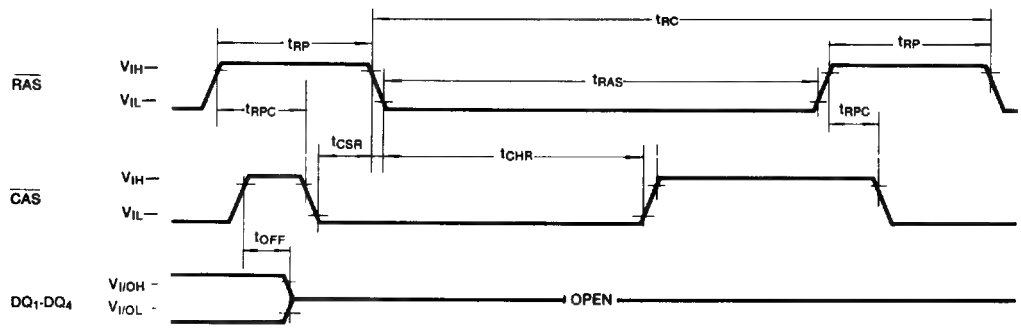
$\overline{RAS}$-ONLY REFRESH CYCLE

Note: $\overline{W}$, $\overline{OE}$ = Don't care



$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

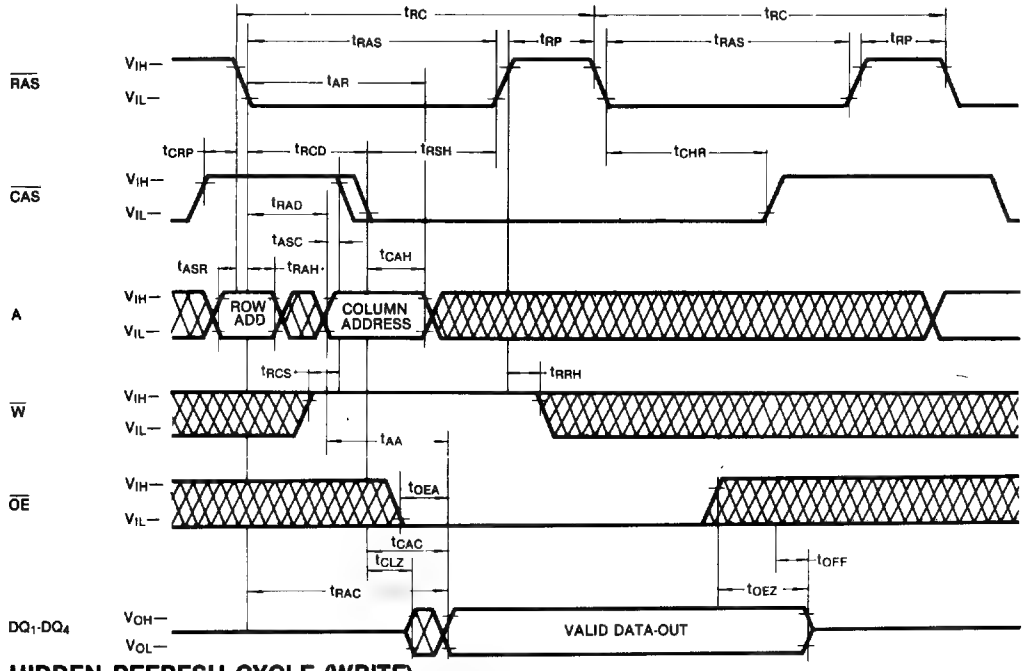
Note: $\overline{W}$, $\overline{OE}$, A = Don't care



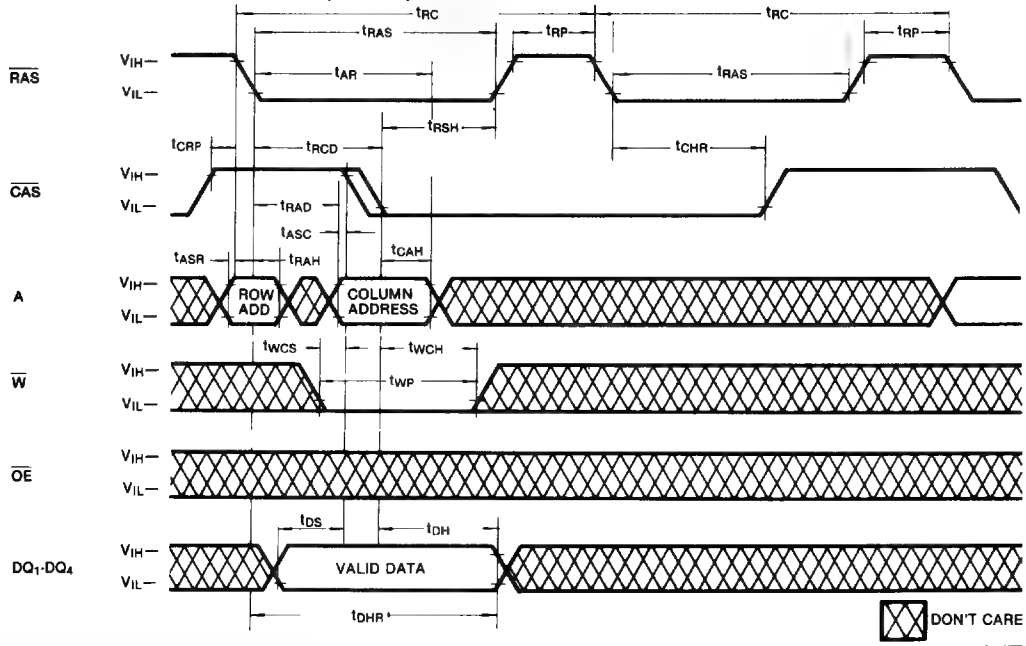
DON'T CARE

TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)

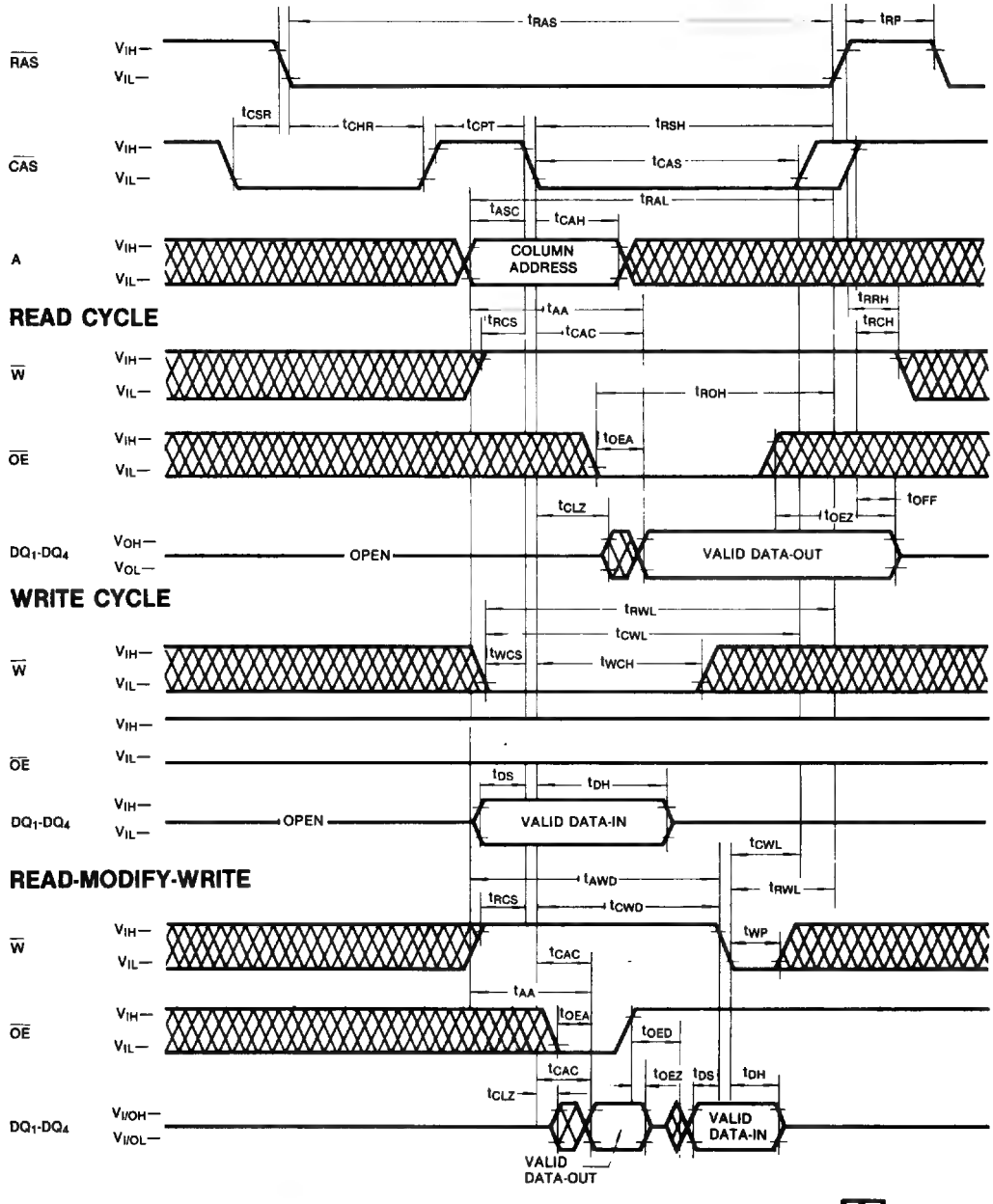


HIDDEN REFRESH CYCLE (WRITE)



TIMING DIAGRAMS (Continued)

CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



KM44C256A OPERATION

Device Operation

The KM44C256A contains 1,048,576 memory locations organized as 262,144 four-bit words. Eighteen address bits are required to address a particular 4-bit word in the memory array. Since the KM44C256A has only 9 address input pins, time multiplexed addressing is used to input 9 row and 9 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{RAS}$), the column address strobe ($\overline{CAS}$) and the valid address inputs.

Operation of the KM44C256A begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. Then the address on the 9 address input pins is changed from a row address to a column address and is strobed in by $\overline{CAS}$. This is the beginning of any KM44C256A cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both $\overline{RAS}$ and $\overline{CAS}$ have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time (tRP) requirement.

$\overline{RAS}$ and $\overline{CAS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths are specified by tRAS(min) and tCAS(min) respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, tRP, has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM44C256A begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input($\overline{W}$) high during a $\overline{RAS}$/$\overline{CAS}$ cycle. The access time is normally specified with respect to the falling edge of $\overline{RAS}$. But the access time also depends on the falling edge of $\overline{CAS}$ and on the valid column address transition.

If $\overline{CAS}$ goes low before tRCD(max) and if the column address is valid before tRAD(max) then the access time to valid data is specified by tRAC(min). However, if $\overline{CAS}$ goes low after tRCD(max) or if the column address becomes valid after tRAD(max), access is specified by tCAC or tAA. In order to achieve the minimum access time, tRAC(min), it is necessary to meet both tRCD(max) and tRAD(max).

The KM44C256A has common data I/O pins. For this reason an output enable control input ($\overline{OE}$) has been provided so the output buffer can be precisely controlled. For data to appear at the outputs, $\overline{OE}$ must be low for the period of time defined by tOEA and tOEZ.

Write

The KM44C256A can perform early write, and read-modify-write cycles. The differece between these cycles is in the state of data-out and is determined by the timing relationship between $\overline{W}$, $\overline{OE}$ and $\overline{CAS}$. In any type of write cycle, Data-in must be valid at or before the falling edge of $\overline{W}$ or $\overline{CAS}$, whichever is later.

Early Write: An early write cycle is performed by bringing $\overline{W}$ low before $\overline{CAS}$. The 4-bit wide data at the data input pins is written into the addressed memory cells. Throughout the early write cycle the output remains in the Hi-Z state. In the early write cycle the output buffers remain in he Hi-Z state regardless of the state of the $\overline{OE}$ input.

Read-Modify-Write: In this cycle, valid data from the addressed cell appears at the output before and during the time that data is being written into the same cell location. This cycle is achieved by bringing $\overline{W}$ low after $\overline{CAS}$ and meeting the data sheet read-modify-write timing requirements. This output enable input ($\overline{OE}$) must be low during the time defined by tOEA and tOEZ for data to appear at the outputs. If tCWD and tRWD are not met the output may contain invalid data. Conforming to the $\overline{OE}$ timing requirements prevents bus contention on the KM44C256A DQ pins.

Data Output

The KM44C256A has a tri-state output buffer which are controlled by $\overline{CAS}$ and $\overline{OE}$. When either $\overline{CAS}$ or $\overline{OE}$ is high (VIH) the output are in the high impedance (Hi-Z) state. In any cycle in which valid data appears at the output, the output goes into the low impedance state in a time specified by tCLZ after the falling edge of $\overline{CAS}$. Invalid data may be present at the output during the time after tCLZ and before the valid data appears at the output. The timing parameters tCAC, tRAC and tAA specify when the valid data will be present at the output. This is true even if a new $\overline{RAS}$ cycle occurs (as in hidden refresh). Each of the KM44C256A operating cycles is listed below after the corresponding output state produced by the cycle.

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Fast Page Mode Read, Fast Page Mode Read-Modify-Write.

Hi-Z Output State: Early Write, $\overline{RAS}$-only Refresh, Fast Page Mode Write, $\overline{CAS}$-only cycle.

Indeterminate Output State: Delayed Write (tCWD or tRWD are not met)

DEVICE OPERATION (Continued)

Refresh

The data in the KM44C256A is stored on a tiny capacitor within each memory cell. Due to leakage the data may leak off after a period of time. To maintain data integrity it is necessary to refresh each of the rows every 8 ms. There are several ways to accomplish this.

$\overline{RAS}$-Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. This cycle must be repeated for each of the 512 row addresses, (A0-A8).

$\overline{CAS}$-before-$\overline{RAS}$ Refresh: The KM44C256A has $\overline{CAS}$-before-$\overline{RAS}$ on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{CAS}$ is held low for the specified set up time (tCSR) before $\overline{RAS}$ goes low, the on-chip refresh circuitry is enabled. An internal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the $\overline{CAS}$ active time and cycling $\overline{RAS}$. The KM44C256A hidden refresh cycle is actually a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter.

Other Refresh Methods: It is also possible to refresh the KM44C256A by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in that row are automatically refreshed. There are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh is the preferred method.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle

A special timing sequence using the $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle provides a convenient method of verifying the functionality of the $\overline{CAS}$-before-$\overline{RAS}$ refresh activated circuitry. The cycle begins as a $\overline{CAS}$-before-$\overline{RAS}$ refresh operation. Then, if $\overline{CAS}$ is brought high and then low again while $\overline{RAS}$ is held low, the read and write operations are enabled. In this mode, the row address bits A0 through A8 are supplied by the on-chip refresh counter. The A9 bit is set low internally.

Fast Page Mode

Fast page mode provides high speed read, write or read-modify-write access to all memory cells within a selected row. These cycles may be mixed in any order. A fast page mode cycle begins with a normal cycle. Then, while $\overline{RAS}$ is kept low to maintain the row address, $\overline{CAS}$ is cycled to strobe in additional column addresses. This eliminates the time required to set up and strobe sequential row addresses for the same page.

Power-up

If $\overline{RAS} = V_{SS}$ during power-up, the KM44C256A could begin an active cycle. This condition results in higher than necessary current demands from the power supply during power-up. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{CC} during power-up or be held at a valid VIH in order to minimize the power-up current.

An initial pause of 200 μsec is required after power-up followed by 8 initialization cycles before proper device operation is assured. Eight initialization cycles are also required after any 8 msec period in which there are no $\overline{RAS}$ cycles. An initialization cycle is any cycle in which $\overline{RAS}$ is cycled.

Termination

The lines from the TTL driver circuits to the KM44C256A inputs act like unterminated transmission lines resulting in significant positive and negative overshoot at the inputs. To minimize overshoot it is advisable to terminate the input lines and to keep them as short as possible. Although either series or parallel termination may be used, series termination is generally recommended since it is simple and draws no additional power. It consists of a resistor in series with the input line placed close to the KM44C256A input pin. The optimum value depends on the board layout. It must be determined experimentally and is usually in the range of 20 to 40 ohms.

Board Layout

It is important to lay out the power and ground lines on memory boards in such a way that switching transient effects are minimized. The recommended methods are gridded power and ground lines or separate power and ground planes. The power and ground lines act like transmission lines to the high frequency transients generated by DRAMS. The impedance is minimized if all the power supply traces to all the DRAMS run both horizontally and vertically and are connected at each intersection or better yet if power and ground planes are used.

Address and control lines should be as short as possible to avoid skew. In boards with many DRAMS these lines should fan out from a central point like a fork or comb rather than being connected in a serpentine pattern. Also the control logic should be centrally located on large memory boards to facilitate the shortest possible address and control lines to all the DRAMS.

DEVICE OPERATION (Continued)

Decoupling

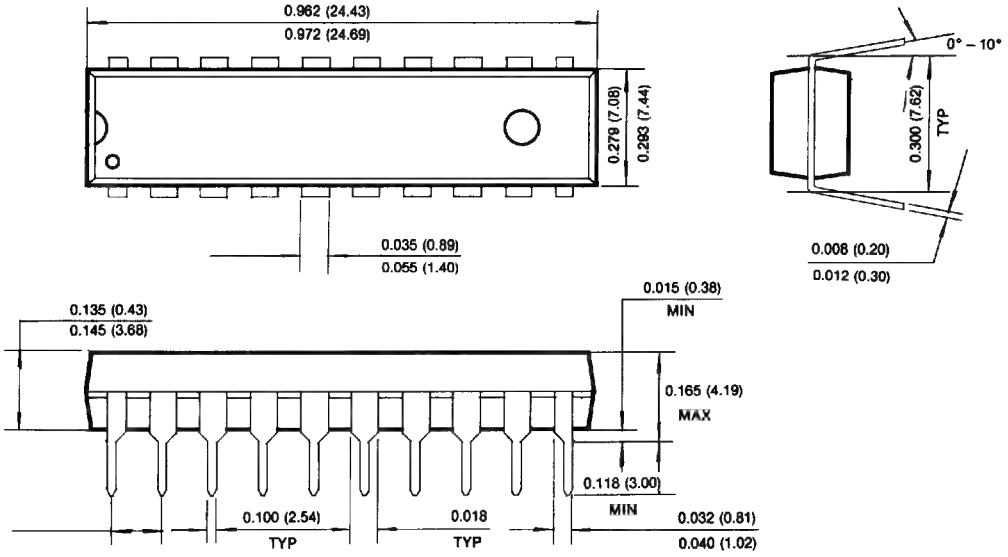
The importance of proper decoupling can not be over emphasized. Excessive transient noise or voltage droop on the V_{CC} line can cause loss of data integrity (soft errors). It is recommended that the total combined voltage changes over time in the VCC to VSS voltage (measured at the device pins) should not exceed 500mV.

A high frequency 0.3μF ceramic decoupling capacitor should be connected between the V_{CC} and ground pins of each KM44C256A using the shortest possible traces. These capacitors act as a low impedance shunt for the high frequency switching transients generated by the KM44C256A and they supply much of the current used by the KM44C256A during cycling.

In addition, a large tantalum capacitor with a value of 47μF to 100μF should be used for bulk decoupling to recharge the 0.3μF capacitors between cycles, thereby reducing power line droop. The bulk decoupling capacitor should be placed near the point where the power traces meet the power grid or power plane. Even better results may be achieved by distributing more than one tantalum capacitor around the memory array.

PACKAGE DIMENSIONS

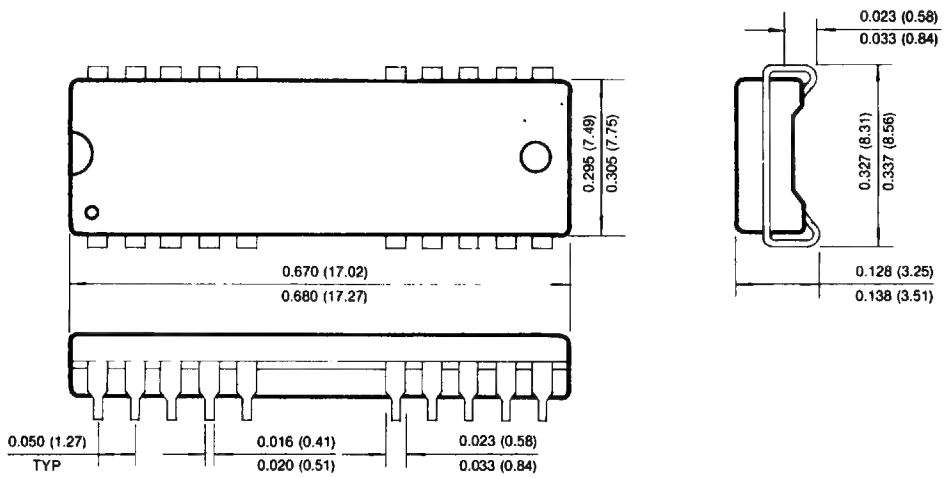
20-LEAD PLASTIC DUAL IN-LINE PACKAGE



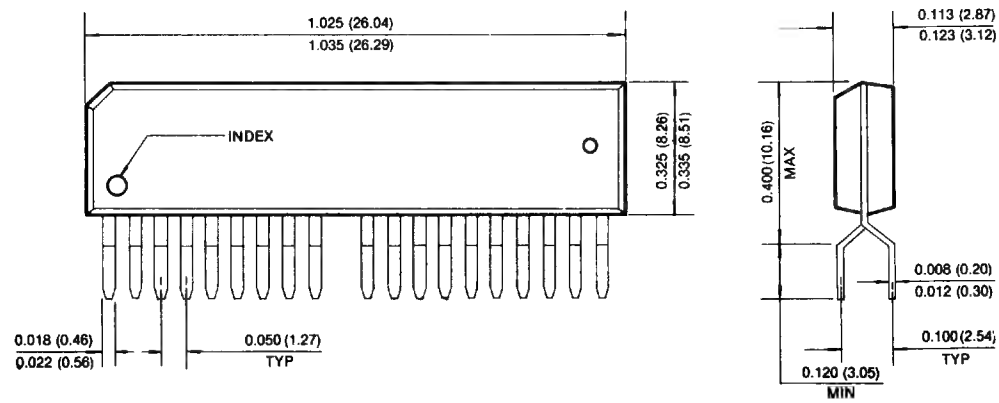
PACKAGE DIAGRAMS (Continued)

20-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



20-PIN PLASTIC ZIGZAG-IN-LINE PACKAGE



256K x 4 Bit CMOS Dynamic RAM with Static Column Mode

FEATURES

- **Performance range:**

	t_{RAC}	t_{CAC}	t_{RC}
KM44C258A-8	80ns	20ns	150ns
KM44C258A-10	100ns	25ns	180ns
KM44C258A-12	120ns	30ns	220ns

- **Static Column Mode operation**
- **$\overline{CS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden refresh capability**
- **TTL compatible inputs and output**
- **Early Write or Output Enable Controlled Write**
- **Single +5V ± 10% power supply**
- **512 cycles/8ms refresh**
- **JEDEC standard pinout**
- **Available in Plastic 20-pin DIP, SOJ and ZIP**

GENERAL DESCRIPTION

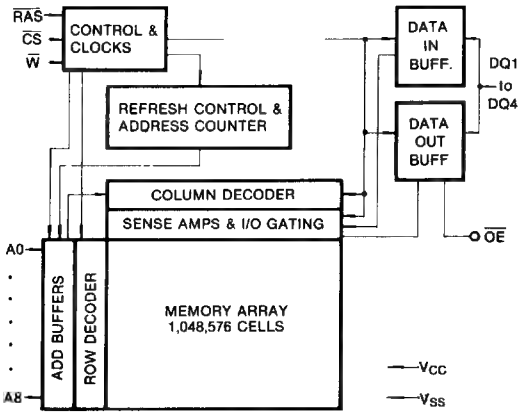
The Samsung KM44C258A is a CMOS high speed 262,144 x 4 dynamic random access memory. Its design is optimized for high performance applications such as cache based mainframes and mini computers, graphics, digital signal processing and high performance microprocessor systems.

Static Column Mode Operation allows high speed random or sequential access within a row. The KM44C258A offers high performance while relaxing many critical system timing requirements for fast usable speed.

$\overline{CS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only Refresh. All inputs and output are fully TTL compatible.

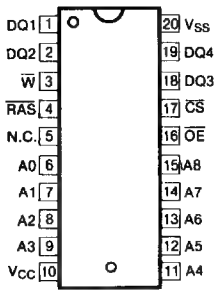
The KM44C258A is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM

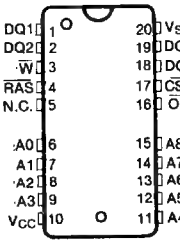


PIN CONFIGURATIONS

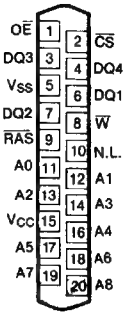
- **KM44C258AP**



- **KM44C258AJ**



- **KM44C258AZ**



Pin Name	Pin Function
A_0-A_8	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CS}$	Chip Select Input
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Output Enable
DQ_1-DQ_4	Data In/Data Output
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection
N.L.	No Lead

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−1 to +7.0	V
Storage Temperature	T_{stg}	−55 to +150	°C
Power Dissipation	P_D	600	mW
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC}+1	V
Input Low Voltage	V_{IL}	−1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
OPERATING CURRENT* ($\overline{RAS}$, $\overline{CS}$, Address cycling @t_{RC} = min.)	KM44C258A-8 KM44C258A-10 KM44C258A-12	I_{CC1}	—	75 65 55	mA
STANDBY CURRENT ($\overline{RAS}$ = $\overline{CS}$ = V_{IH})		I_{CC2}	—	2	mA
$\overline{RAS}$-ONLY REFRESH CURRENT* ($\overline{CS}$ = V_{IH}, $\overline{RAS}$ cycling @t_{RC} = min.)	KM44C258A-8 KM44C258A-10 KM44C258A-12	I_{CC3}	—	75 65 55	mA
STATIC COLUMN MODE CURRENT* ($\overline{RAS}$ = $\overline{CS}$ = V_{IL}, Address cycling; @t_{SC} = min.)	KM44C258A-8 KM44C258A-10 KM44C258A-12	I_{CC4}	—	55 45 35	mA
STANDBY CURRENT ($\overline{RAS}$ = $\overline{CS}$ = V_{CC} − 0.2V)		I_{CC5}	—	1	mA
$\overline{CS}$-BEFORE-RAS REFRESH CURRENT* ($\overline{RAS}$ and $\overline{CS}$ cycling @t_{RC} = min.)	KM44C258A-8 KM44C258A-10 KM44C258A-12	I_{CC6}	—	75 65 55	mA
INPUT LEAKAGE CURRENT (Any input 0≤V_{IN}≤6.5V, all other pins not under test = 0 volts.)		I_{IL}	−10	10	μA
OUTPUT LEAKAGE CURRENT (Data out is disabled, 0V≤V_{OUT}≤5.5V		I_{OL}	−10	10	μA
OUTPUT HIGH VOLTAGE LEVEL (I_{OH} = −5mA)		V_{OH}	2.4	—	V
OUTPUT LOW VOLTAGE LEVEL (I_{OL} = 4.2mA)		V_{OL}	—	0.4	V

*Note: I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current.

CAPACITANCE ($T_A = 25°C$)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A_0-A_8)	C_{IN1}	—	6	pF
Input Capacitance ($\overline{RAS}$, $\overline{CS}$, $\overline{W}$, $\overline{OE}$)	C_{IN2}	—	7	pF
Output Capacitance (DQ_1-DQ_4)	C_{DQ}	—	7	pF

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC} = 5.0V \pm 10\%$, See notes 1, 2)

Parameter	Symbol	KM44C258A-8		KM44C258A-10		KM44C258A-12		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	150		180		220		ns	
Read-modify-write cycle time	t_{RWC}	205		245		295		ns	
Static column mode cycle time	t_{SC}	45		55		65		ns	
Static column mode read-write cycle time	t_{SRWC}	110		135		160		ns	
Access time from $\overline{RAS}$	t_{RAC}		80		100		120	ns	3,4,11
Access time from $\overline{CS}$	t_{CAC}		20		25		30	ns	3,4,5
Access time from column address	t_{AA}		40		50		60	ns	3,11
Access time from last write	t_{ALW}		75		95		115	ns	3,12
$\overline{CS}$ to output in Low-Z	t_{CLZ}	5		5		5		ns	3
Output buffer turn-off delay time	t_{OFF}	0	25	0	30	0	35	ns	7
Output data hold time from column address	t_{AOH}	5		5		5		ns	
Output data enable time from $\overline{W}$	t_{OW}		50		70		85	ns	
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	60		70		90		ns	
$\overline{RAS}$ pulse width	t_{RAS}	80	10,000	100	10,000	120	10,000	ns	
$\overline{RAS}$ pulse width (static column mode)	t_{RASC}	80	100,000	100	100,000	120	100,000	ns	
$\overline{CS}$ to $\overline{RAS}$ hold time	t_{RSH}	20		25		30		ns	
$\overline{RAS}$ to $\overline{CS}$ hold time	t_{CSH}	80		100		120		ns	
$\overline{CS}$ pulse width	t_{CS}	20	10,000	25	10,000	30	10,000	ns	
$\overline{CS}$ pulse width (static column mode)	t_{CSC}	20	100,000	25	100,000	30	100,000	ns	
$\overline{RAS}$ to $\overline{CS}$ delay time	t_{RCD}	25	60	25	75	25	90	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	20	40	20	50	20	60	ns	11
$\overline{CS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		ns	11
$\overline{CS}$ precharge time (static column mode)	t_{CP}	10		10		15		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	15		15		15		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	20		20		25		ns	
Write address hold time referenced to $\overline{RAS}$	t_{AWR}	65		75		90		ns	6

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC} = 5.0V \pm 10\%$. See notes 1, 2)

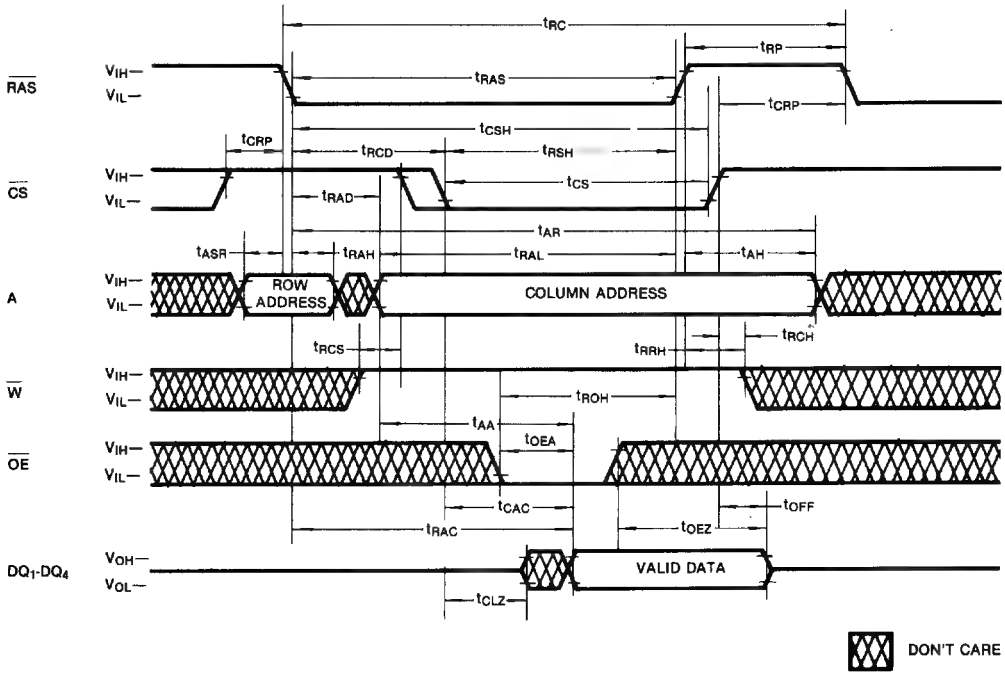
Parameter	Symbol	KM44C258A-8		KM44C258A-10		KM44C258A-12		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Column address hold time referenced to $\overline{RAS}$	t_{AR}	95		115		140		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	40		50		60		ns	
Column address hold time referenced to $\overline{RAS}$ rise	t_{AH}	10		10		15		ns	
Last write to column address delay time	t_{LWAD}	25	35	25	45	30	55	ns	
Last write to column address hold time	t_{AHLW}	75		95		115		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold time referenced to $\overline{CS}$	t_{RCH}	0		0		0		ns	9
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	9
Write command hold time	t_{WCH}	20		20		25		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	65		75		90		ns	6
Write command pulse width	t_{WP}	20		20		25		ns	
Write command inactive time	t_{WI}	10		10		15		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		25		30		ns	
Write command to $\overline{CS}$ lead time	t_{CWL}	20		25		30		ns	
Data set-up time	t_{DS}	0		0		0		ns	10
Data hold time	t_{DH}	20		20		25		ns	10
Data hold time referenced to $\overline{RAS}$	t_{DHR}	65		75		90		ns	6
Refresh period (512 cycles)	t_{REF}		8		8		8	ms	
Write command set-up time	t_{WCS}	0		0		0		ns	8
$\overline{CS}$ to $\overline{W}$ delay time	t_{CWD}	50		60		70		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	110		135		160		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	70		85		100		ns	8
$\overline{CS}$ setup time ($\overline{CS}$-before-$\overline{RAS}$ cycle)	t_{CSR}	10		10		10		ns	
$\overline{CS}$ hold time ($\overline{CS}$-before-$\overline{RAS}$ cycle)	t_{CHR}	30		30		30		ns	
$\overline{RAS}$ to $\overline{CS}$ precharge time	t_{RPC}	10		10		10		ns	
$\overline{CS}$ precharge ($\overline{CS}$-before-$\overline{RAS}$ counter test cycle)	t_{CPT}	40		50		60		ns	
$\overline{RAS}$ hold time reference to OE	t_{ROH}	20		20		20		ns	
$\overline{OE}$ access time	t_{OEA}		20		25		30	ns	
$\overline{OE}$ to data delay	t_{OED}	20		25		30		ns	
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	0	20	0	25	0	30	ns	
$\overline{OE}$ command hold time	t_{OEH}	20		25		30		ns	

NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max), and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$(max).
6. t_{AWR}, t_{WCR}, t_{DHR} are referenced to t_{RAD}(max).
7. This parameter defineds the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data out pin will remain open circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$(min) and $t_{RWD} \geq t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$(min), then the cycle is a read-write cycle and the data out will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is in indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
12. Operation within the t_{LWAD}(max) limit insures that t_{ALW}(max) can be met. t_{LWAD}(max) is specified as a reference point only. If t_{LWAD} is greater than the specified t_{LWAD}(max) limit, then access time is controlled by t_{AA}.

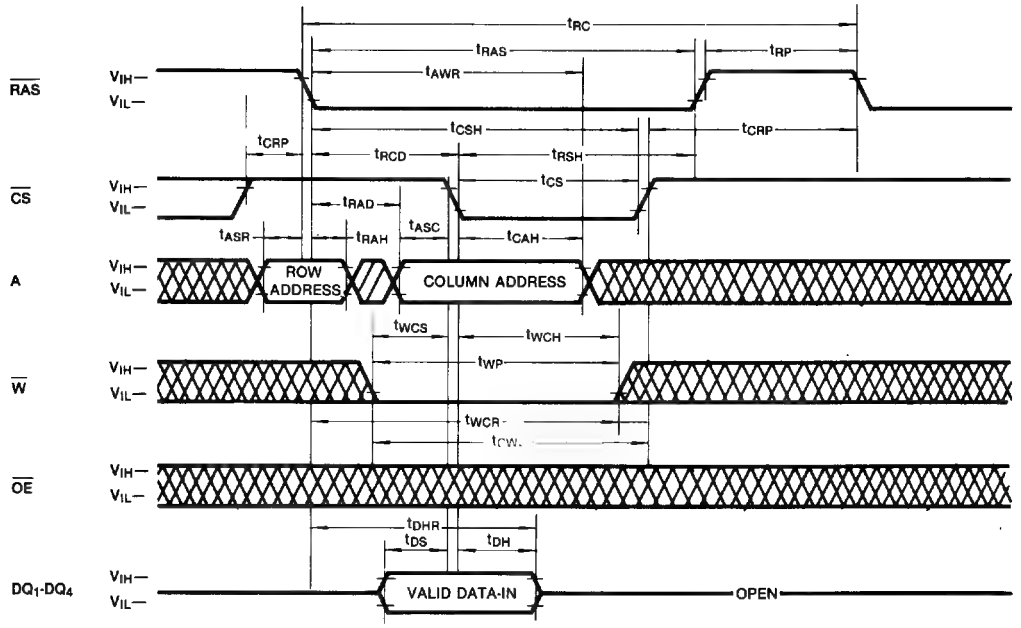
TIMING DIAGRAMS (Continued)

READ CYCLE

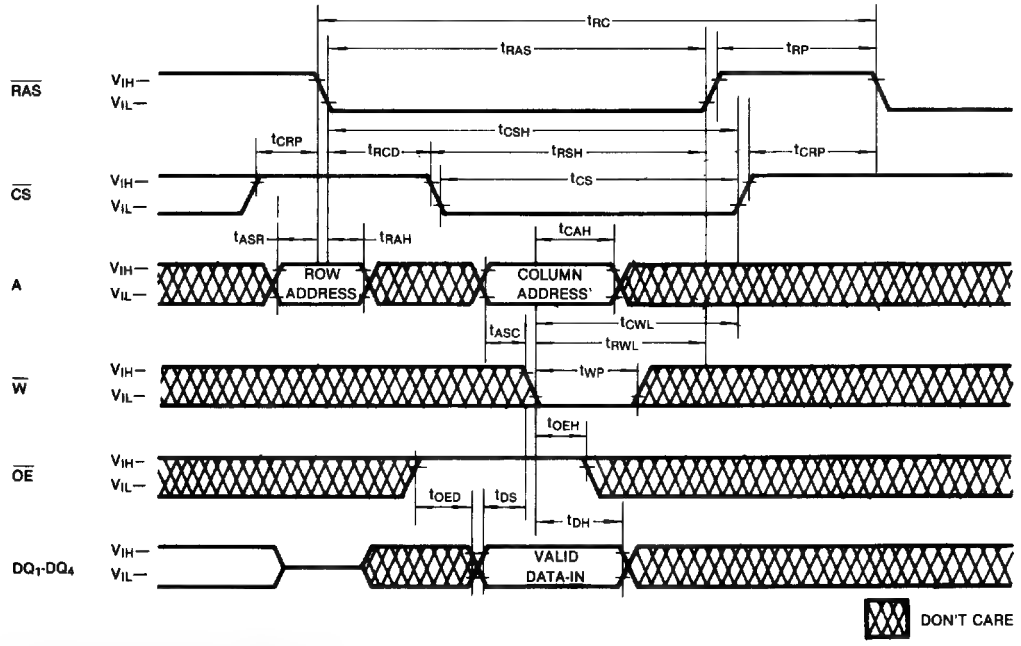


TIMING DIAGRAMS (Continued)

WRITE CYCLE (EARLY WRITE)

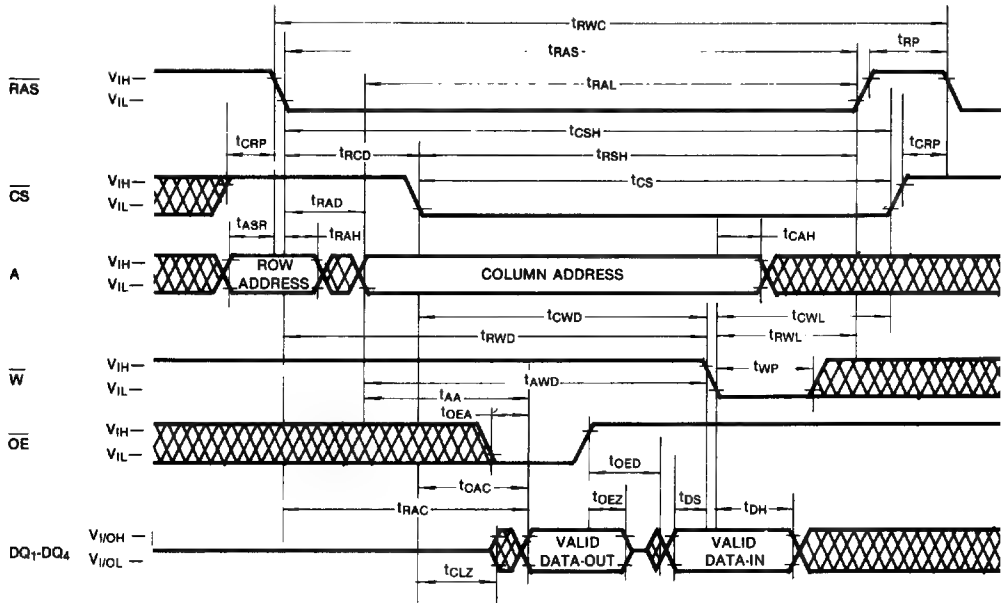


WRITE CYCLE (OE CONTROLLED WRITE)

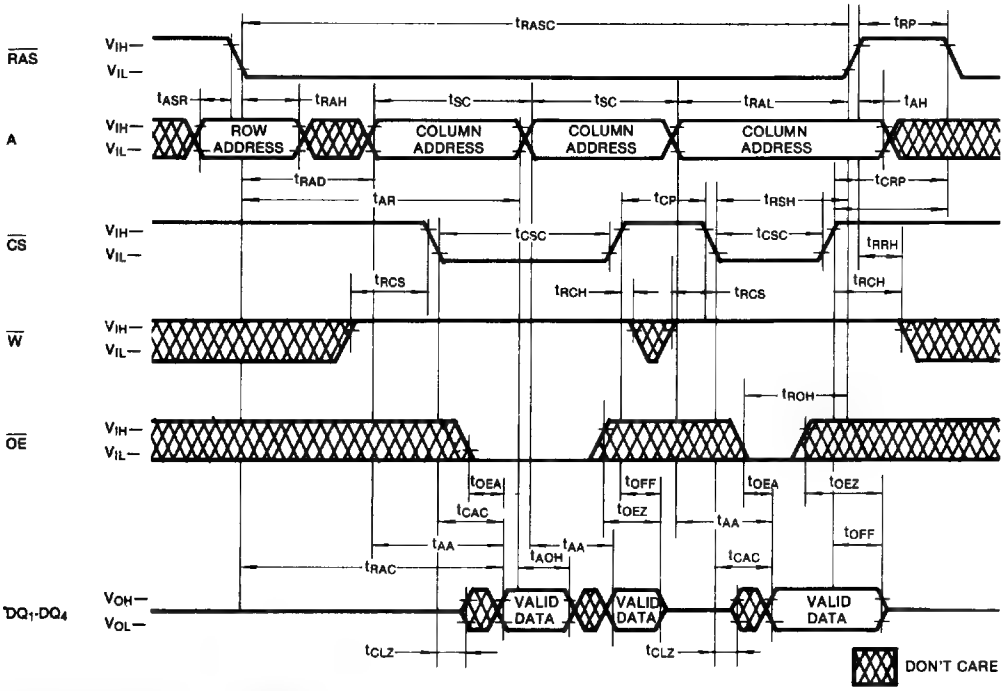


TIMING DIAGRAMS (Continued)

READ-WRITE/READ-MODIFY-WRITE

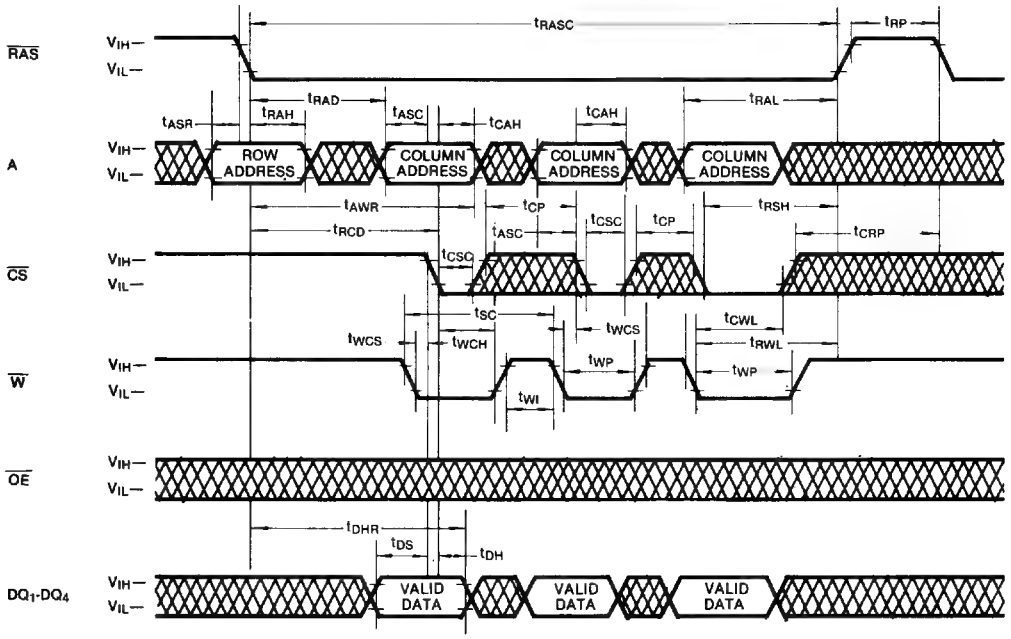


STATIC COLUMN MODE READ CYCLE

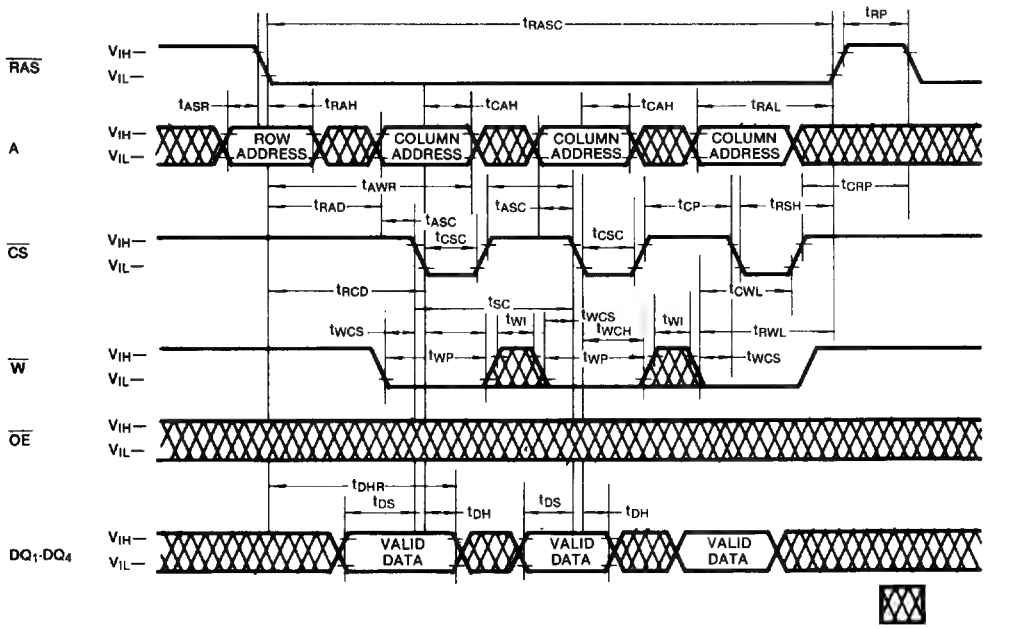


TIMING DIAGRAMS (Continued)

STATIC COLUMN MODE WRITE CYCLE ($\overline{W}$ controlled early write)

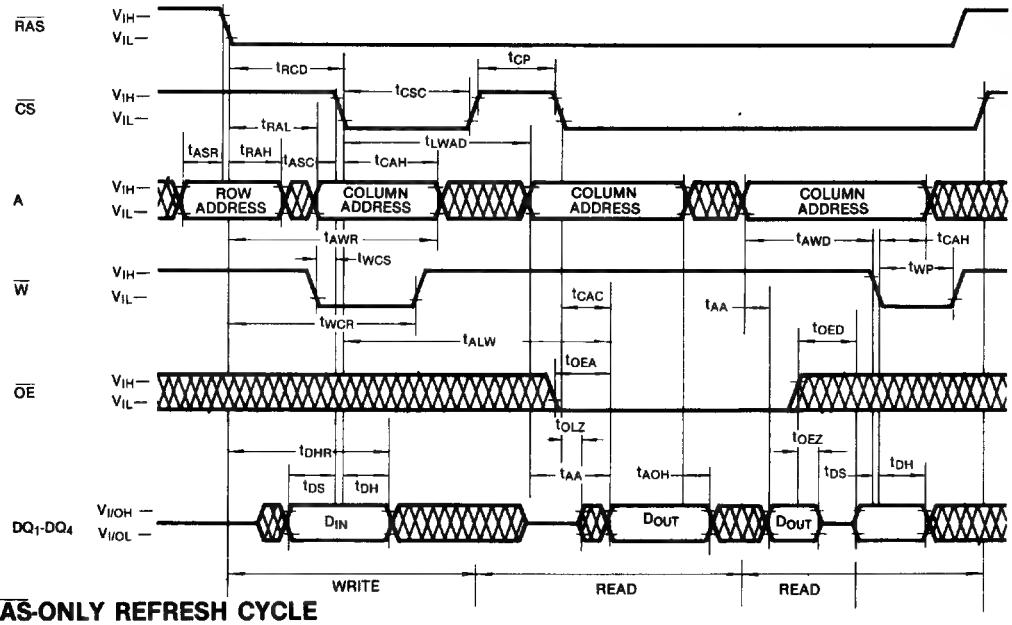


STATIC COLUMN MODE WRITE CYCLE ($\overline{CS}$ controlled early write)



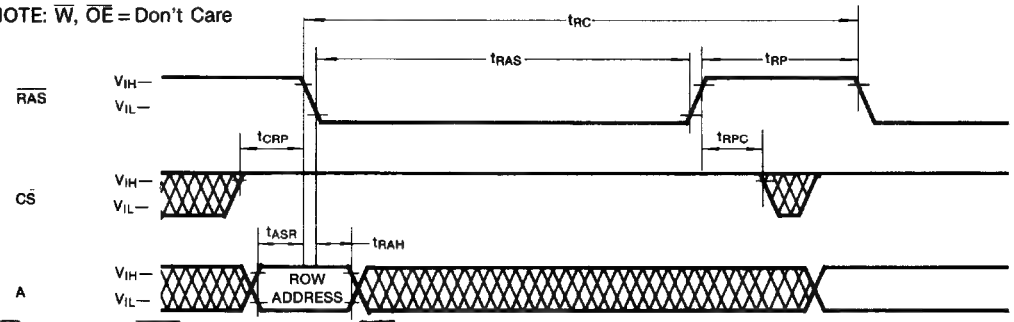
TIMING DIAGRAMS (Continued)

STATIC COLUMN MODE MIXED CYCLE



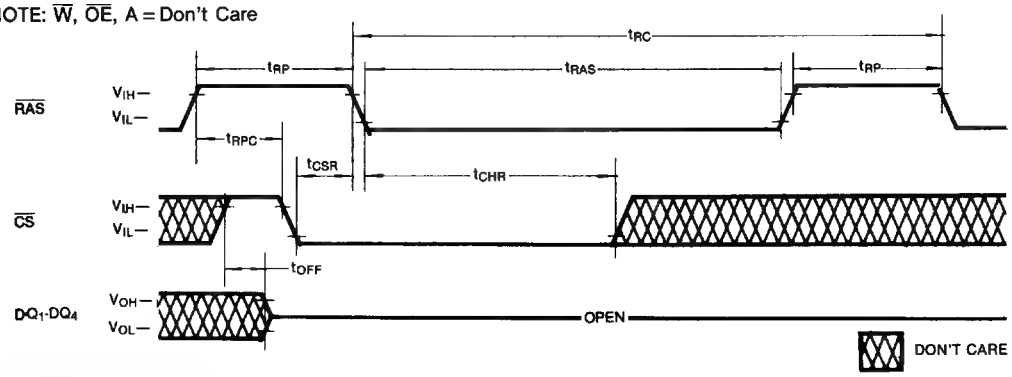
RAS-ONLY REFRESH CYCLE

NOTE: W, OE = Don't Care



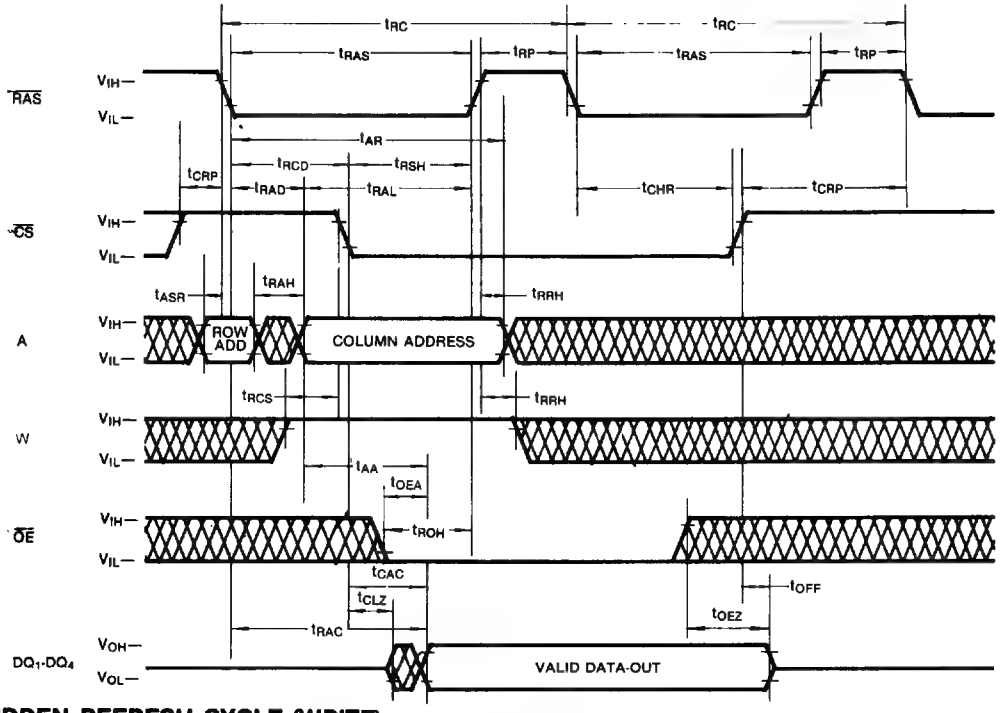
CS-BEFORE-RAS REFRESH CYCLE

NOTE: W, OE, A = Don't Care

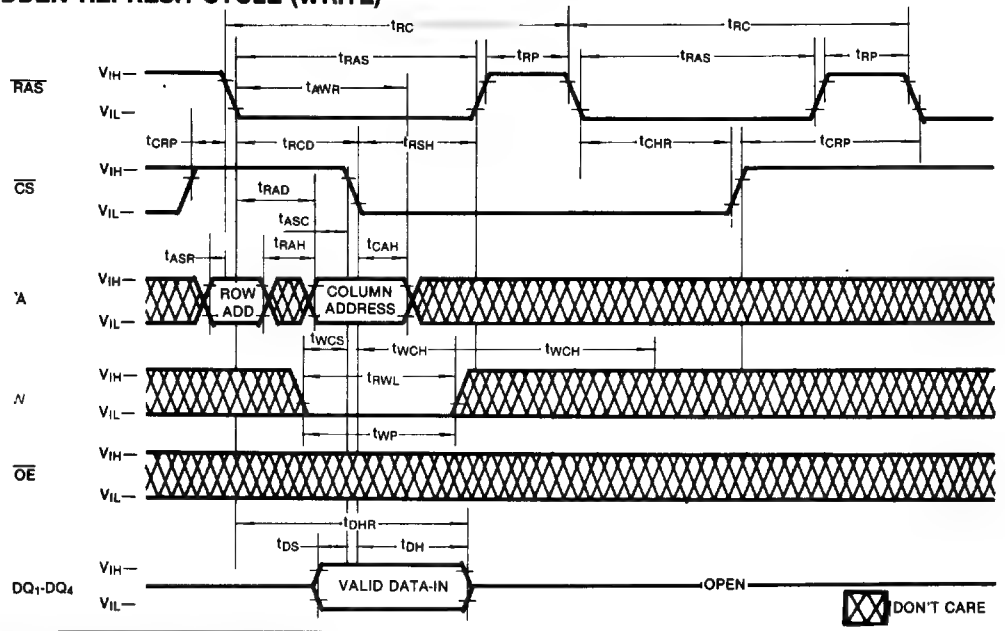


TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)

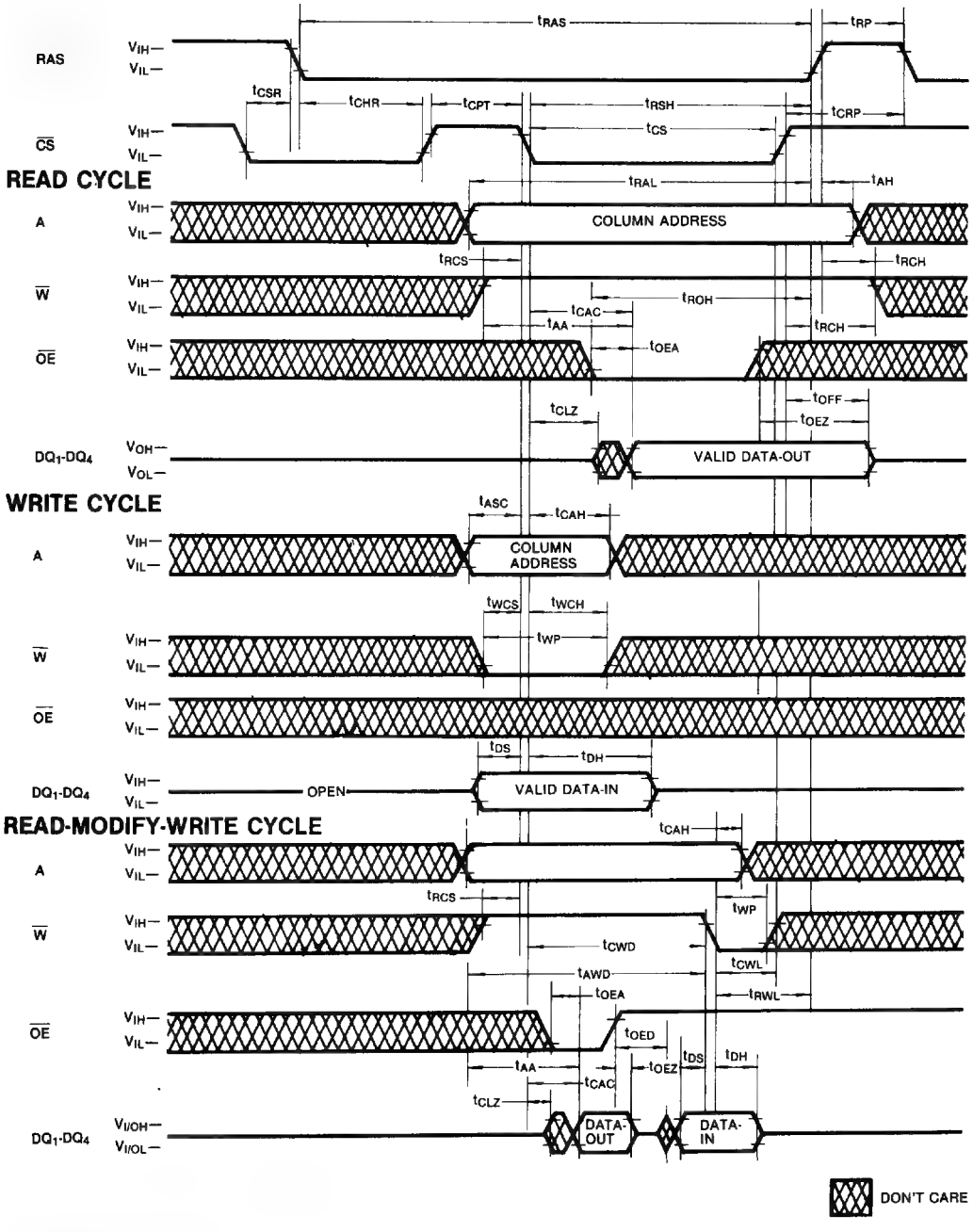


HIDDEN REFRESH CYCLE (WRITE)



TIMING DIAGRAMS (Continued)

$\overline{CS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE



KM44C258A OPERATION

Device Operation

The KM44C258A contains 1,048,576 memory locationsorganized as 262,144 four-bit words. Eighteen address bits are required to address a particular 4-bit word in the memory array. Since the KM44C258A has only 9 address input pins, time multiplexed addressing is used to input 9 row and 9 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{RAS}$), the column address strobe ($\overline{CS}$) and the valid address inputs.

Operation of the KM44C258A begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{CS}$ remains high. Then the address on the 9 address input pins is changed from a row address to a column address and is strobed in by $\overline{CS}$. This is the beginning of any KM44C258A cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both $\overline{RAS}$ and $\overline{CS}$ have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time (t_{RP}) requirement.

$\overline{RAS}$ and $\overline{CS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CS}$ pulse widths are specified by t_{RAS}(min) and t_{CS}(min) respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CS}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, t_{RP}, has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM44C258A begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input($\overline{W}$) high during a $\overline{RAS}$/$\overline{CS}$ cycle. The access time is normally specified with respect to the falling edge of $\overline{RAS}$. But the access time also depends on the falling edge of $\overline{CS}$ and on the valid column address transition.

If $\overline{CS}$ goes low before t_{RCD}(max) and if the column address is valid before t_{RAD}(max) then the access time to valid data is specified by t_{RAC}(min). However, if $\overline{CS}$ goes low after t_{RCD}(max) or if the column address becomes valid after t_{RAD}(max), access is specified by t_{CAC} or tAA. In order to achieve the minimum access time, t_{RAC}(min), it is necessary to meet both t_{RCD}(max) and t_{RAD}(max).

The KM44C258A has common data I/O pins. For this reason an output enable control input ($\overline{OE}$) has been provided so the output buffer can be precisely controlled. For data to appear at the outputs, $\overline{OE}$ must be low for the period of time defined by t_{OEA} and t_{OEZ}.

Write

The KM44C258A can perform early write, and read-modify-write cycles. The differece between these cycles is in the state of data-out and is determined by the timing relationship between $\overline{W}$, $\overline{OE}$ and $\overline{CS}$. In any type of write cycle, Data-in must be valid at or before the falling edge of $\overline{W}$ or $\overline{CS}$, whichever is later.

Early Write: An early write cycle is performed by bringing W low before $\overline{CS}$. The 4-bit wide data at the data input pins is written into the addressed memory cells. Throughout the early write cycle the output remains in the Hi-Z state. In the early write cycle the output buffers remain in he Hi-Z state regardless of the state of the $\overline{OE}$ input.

Read-Modify-Write: In this cycle, valid data from the addressed cell appears at the output before and during the time that data is being written into the same cell location. This cycle is achieved by bringing $\overline{W}$ low after $\overline{CS}$ and meeting the data sheet read-modify-write timing requirements. This output enable input ($\overline{OE}$) must be low during the time defined by t_{OEA} and t_{OEZ} for data to appear at the outputs. If t_{CWD} and t_{RWD} are not met the output may contain invalid data. Conforming to the $\overline{OE}$ timing requirements prevents bus contention on the KM44C258A DQ pins.

Data Output

The KM44C258A has a tri-state output buffer which are controlled by $\overline{CS}$ and $\overline{OE}$. When either $\overline{CS}$ or $\overline{OE}$ is high (V_{IH}) the output are in the high impedance (Hi-Z) state.

In any cycle in which valid data appears at the output, the output goes into the low impedance state in a time specified by t_{CLZ} after the falling edge of $\overline{CS}$. Invalid data may be present at the output during the time after t_{CLZ} and before the valid data appears at the output. The timing parameters t_{CAC}, t_{RAC} and t_{AA} specify when the valid data will be present at the output. This is true even if a new $\overline{RAS}$ cycle occurs (as in hidden refresh). Each of the KM44C258A operating cycles is listed below after the corresponding output state produced by the cycle.

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Fast Page Mode Read, Fast Page Mode Read-Modify-Write.

Hi-Z Output State: Early Write, $\overline{RAS}$-only Refresh, Fast Page Mode Write, $\overline{CS}$-only cycle.

Indeterminate Output State: Delayed Write (t_{CWD} or t_{RWD} are not met)

KM44C258A OPERATION

Refresh

The data in the KM44C258A is stored on a tiny capacitor within each memory cell. Due to leakage the data may leak off after a period of time. To maintain data integrity it is necessary to refresh each of the rows every 8 ms. There are several ways to accomplish this.

$\overline{RAS}$-Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{RAS}$ while $\overline{CS}$ remains high. This cycle must be repeated for each of the 512 row addresses, (A_0-A_8).

$\overline{CS}$-before-$\overline{RAS}$ Refresh: The KM44C258A has $\overline{CS}$-before-RAS on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{CS}$ is held low for the specified set up time (t_{CSR}) before $\overline{RAS}$ goes low, the on-chip refresh circuitry is enabled. An internal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next $\overline{CS}$-before-$\overline{RAS}$ refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the $\overline{CS}$ active time and cycling $\overline{RAS}$. The KM44C258A hidden refresh cycle is actually a $\overline{CS}$-before-$\overline{RAS}$ refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter.

Other Refresh Methods: It is also possible to refresh the KM44C258A by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in that row are automatically refreshed. There are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{RAS}$-only or $\overline{CS}$-before-$\overline{RAS}$ refresh is the preferred method.

$\overline{CS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle

A special timing sequence using the $\overline{CS}$-before-$\overline{RAS}$ refresh counter test cycle provides a convenient method of verifying the functionality of the $\overline{CS}$-before-$\overline{RAS}$ refresh activated circuitry. The cycle begins as a $\overline{CS}$-before-$\overline{RAS}$ refresh operation. Then, if $\overline{CS}$ is brought high and then low again while $\overline{RAS}$ is held low, the read and write operations are enabled. In this mode, the row address bits A_0 through A_8 are supplied by the on-chip refresh counter. The A_9 bit is set low internally.

Static Column Mode

Static Column mode allows high speed read, write or read-modify-write random access to all the memory cells within a selected row. Operation within a selected row is similar to a static RAM.

A Static Column mode read cycle starts as a normal cycle. Additional cells within the selected row are written by applying a new column address while $\overline{W} = V_{IH}$ and $\overline{RAS} = V_{IL}$.

A Static Column mode write cycle starts as a normal cycle. Additional cells within the selected row are written by applying a new column address while $\overline{RAS} = V_{IL}$ and toggiling either $\overline{W}$ or $\overline{CS}$. The data is written into the cell triggered by the latter falling edge of W or $\overline{CS}$.

Power-up

If $\overline{RAS} = V_{SS}$ during power-up, the KM44C258A could begin an active cycle. This condition results in higher than necessary current demands from the power supply during power-up. It is recommended that $\overline{RAS}$ and $\overline{CS}$ track with V_{CC} during power-up or be held at a valid V_{IH} in order to minimize the power-up current.

An initial pause of 200 μsec is required after power-up followed by 8 initialization cycles before proper device operation is assured. Eight initialization cycles are also required after any 8 msec period in which there are no $\overline{RAS}$ cycles. An initialization cycle is any cycle in which $\overline{RAS}$ is cycled.

Termination

The lines from the TTL driver circuits to the KM44C258A inputs act like unterminated transmission lines resulting in significant positive and negative overshoot at the inputs. To minimize overshoot it is advisable to terminate the input lines and to keep them as short as possible. Although either series or parallel termination may be used, series termination is generally recommended since it is simple and draws no additional power. It consists of a resistor in series with the input line placed close to the KM44C258A input pin. The optimum value depends on the board layout. It must be determined experimentally and is usually in the range of 20 to 40 ohms.

Board Layout

It is important to lay out the power and ground lines on memory boards in such a way that switching transient effects are minimized. The recommended methods are gridded power and ground lines or separate power and ground planes. The power and ground lines act like transmission lines to the high frequency transients generated by DRAMS. The impedance is minimized if all the power supply traces to all the DRAMS run both horizontally and vertically and are connected at each intersection or better yet if power and ground planes are used.

Address and control lines should be as short as possible to avoid skew. In boards with many DRAMS these lines should fan out from a central point like a fork or comb rather than being connected in a serpentine pattern. Also the control logic should be centrally located on large memory boards to facilitate the shortest possible address and control lines to all the DRAMS.

Device Operation (Continued)

Decoupling

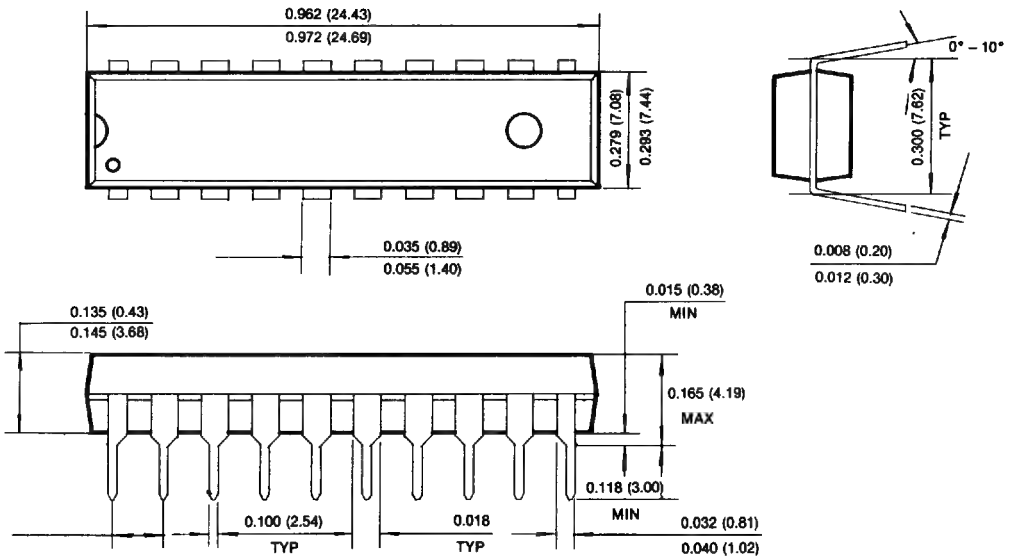
The importance of proper decoupling can not be over emphasized. Excessive transient noise or voltage droop on the V_{CC} line can cause loss of data integrity (soft errors). It is recommended that the total combined voltage changes over time in the V_{CC} to V_{SS} voltage (measured at the device pins) should not exceed 500mV.

A high frequency 0.3μF ceramic decoupling capacitor should be connected between the V_{CC} and ground pins of each KM44C258A using the shortest possible traces. These capacitors act as a low impedance shunt for the high frequency switching transients generated by the KM44C258A and they supply much of the current used by the KM44C258A during cycling.

In addition, a large tantalum capacitor with a value of 47μF to 100μF should be used for bulk decoupling to recharge the 0.3μF capacitors between cycles, thereby reducing power line droop. The bulk decoupling capacitor should be placed near the point where the power traces meet the power grid or power plane. Even better results may be achieved by distributing more than one tantalum capacitor around the memory array.

PACKAGE DIMENSIONS

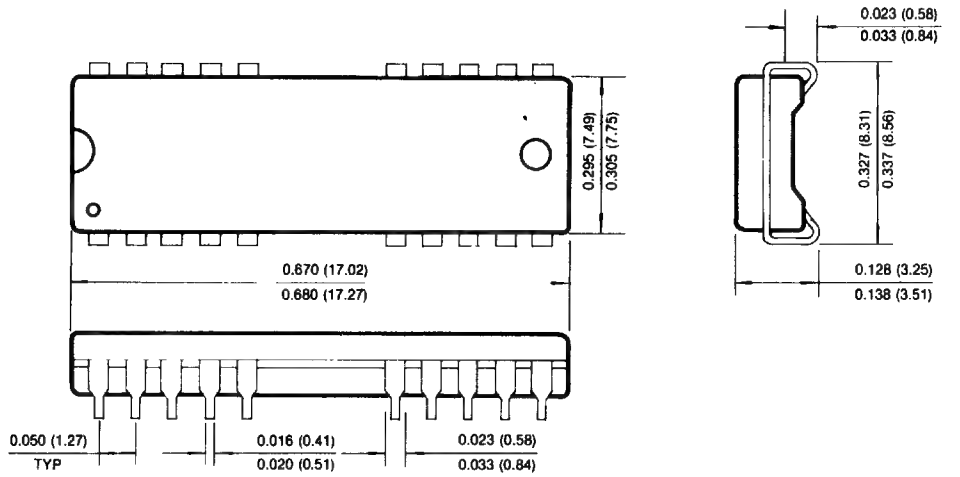
20-LEAD PLASTIC DUAL IN-LINE PACKAGE



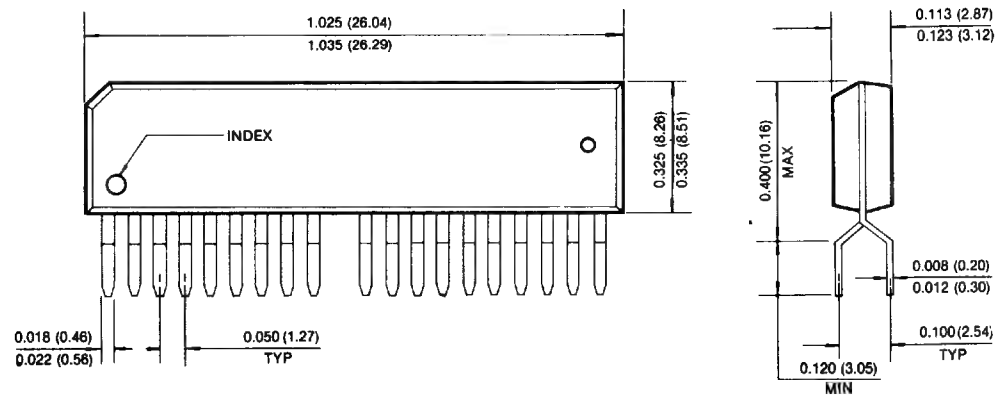
PACKAGE DIAGRAMS (Continued)

20-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



20-PIN PLASTIC ZIGZAG-IN-LINE PACKAGE



4M × 1 Bit Dynamic RAM with Fast Page Mode

FEATURES

- **Performance range:**

	t_{RAC}	t_{CAC}	t_{RC}
KM41C4000-8	80ns	20ns	160ns
KM41C4000-10	100ns	25ns	190ns
KM41C4000-12	120ns	30ns	220ns

- **Fast Page Mode operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **8 bit fast parallel test mode**
- **TTL compatible inputs and output**
- **Common I/O using early write**
- **Single +5V ± 10% power supply**
- **1,024 cycle/16ms refresh**
- **JEDEC standard pinout available in Plastic SOJ package.**

GENERAL DESCRIPTION

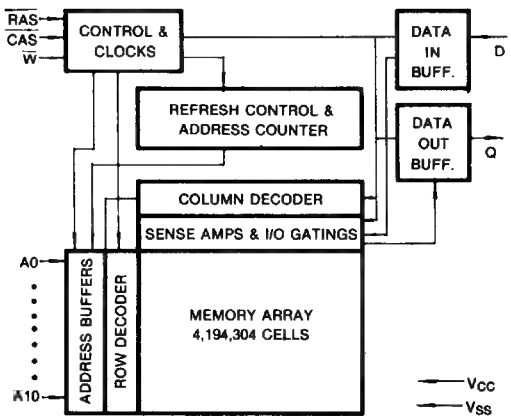
The Samsung KM41C4000 is a CMOS high speed 4,194,304 × 1 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes and mini computers, graphics and high performance microprocessor systems.

The KM41C4000 features Fast Page Mode operation which allows high speed random access of memory cells within the same row.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only Refresh. All inputs and output are fully TTL compatible.

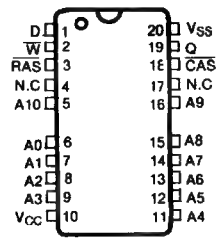
The KM41C4000 is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION

- **KM41C4000J**



Pin Name	Pin Function
A_0-A_{10}	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{W}$	Read/Write Input
D	Data In
Q	Data Out
V_{CC}	Power (+5V)
V_{SS}	Ground
T.F.	Test Function
N.C.	No Connection

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Units
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7.0	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	−1 to +7.0	V
Storage Temperature	T_{stg}	−55 to +150	°C
Power Dissipation	P_D	0.6	W
Short Circuit Output Current	I_{OS}	50	mA

*Note: Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC}+1	V
Input Low Voltage	V_{IL}	−1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Min	Max	Units
OPERATING CURRENT* ($\overline{RAS}$, $\overline{CAS}$, Address cyling @t_{RC} = min.)	KM41C4000-8 KM41C4000-10 KM41C4000-12	I_{CC1}	—	100 85 70	mA
STANDBY CURRENT ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		I_{CC2}	—	2	mA
RAS-ONLY REFRESH CURRENT* ($\overline{CAS}$ = V_{IH}, $\overline{RAS}$ cycling @t_{RC} = min.)	KM41C4000-8 KM41C4000-10 KM41C4000-12	I_{CC3}	—	100 85 70	mA
FAST PAGE MODE CURRENT* ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling; @t_{PC} = min.)	KM41C4000-8 KM41C4000-10 KM41C4000-12	I_{CC4}	—	70 60 50	mA
STANDBY CURRENT ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} − 0.2V)		I_{CC5}	—	1	mA
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CURRENT* ($\overline{RAS}$ and $\overline{CAS}$ cycling @t_{RC} = min.)	KM41C4000-8 KM41C4000-10 KM41C4000-12	I_{CC6}	—	100 85 70	mA
INPUT LEAKAGE CURRENT (Any input 0≤V_{IN}≤6.5V, all other pins not under test = 0 volts.)		I_{IL}	−10	10	μA
OUTPUT LEAKAGE CURRENT (Data out is disabled, 0V≤V_{OUT}≤5.5V		I_{OL}	−10	10	μA
OUTPUT HIGH VOLTAGE LEVEL (I_{OH} = −5mA)		V_{OH}	2.4	—	V
OUTPUT LOW VOLTAGE LEVEL (I_{OL} = 4.2mA)		V_{OL}	—	0.4	V

*Note: I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC8} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current.

CAPACITANCE ($T_A = 25°C$)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (D)	C_{IN1}	—	5	pF
Input Capacitance ($A_0 - A_{10}$)	C_{IN2}	—	5	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{W}$)	C_{IN3}	—	7	pF
Output Capacitance (Q)	C_{OUT}	—	7	pF

AC CHARACTERISTICS

STANDARD OPERATION ($0°C \leq T_A \leq 70°C$, $V_{CC} = 5.0V \pm 10\%$. See notes 1, 2)

Parameter	Symbol	KM41C4000-8		KM41C4000-10		KM41C4000-12		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	160		190		220		ns	
Read-modify-write cycle time	t_{RWC}	185		220		255		ns	
Access time from $\overline{RAS}$	t_{RAC}		80		100		120	ns	3,4
Access time from $\overline{CAS}$	t_{CAC}		20		25		30	ns	3,4
Access time from column address	t_{AA}		40		50		60	ns	3,10
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	5		5		5		ns	3
Output buffer turn-off delay	t_{OFF}	0	20	0	25	0	30	ns	6
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	70		80		90		ns	
$\overline{RAS}$ pulse width	t_{RAS}	80	10,000	100	10,000	120	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		25		30		ns	
$\overline{CAS}$ precharge time	t_{CPN}	15		15		20		ns	
$\overline{CAS}$ hold time	t_{CSH}	80		100		120		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	25	10,000	30	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	60	25	75	25	90	ns	4,5
$\overline{RAS}$ to column address delay time	t_{RAD}	15	40	20	50	25	60	ns	10
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		15		20		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		20		25		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	60		75		90		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	40		50		60		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	8

STANDARD OPERATION (Continued)

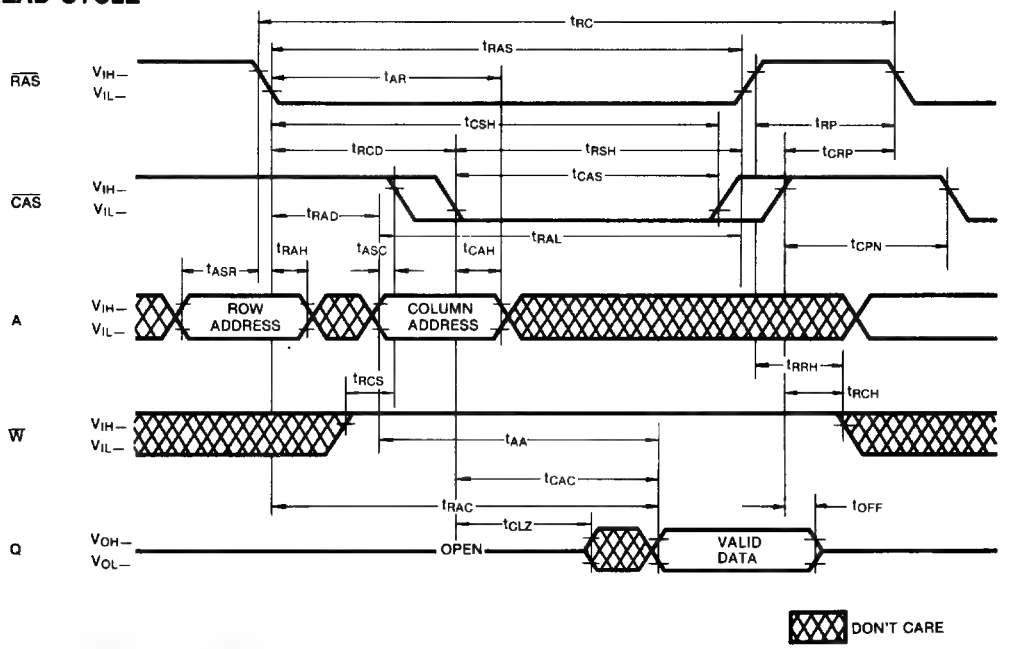
Parameter	Symbol	KM41C4000-8		KM41C4000-10		KM41C4000-12		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	8
Write command hold time	t_{WCH}	15		20		25		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	60		75		90		ns	
Write command pulse width	t_{WP}	15		20		25		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		25		30		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	20		25		30		ns	
Data-in set-up time	t_{DS}	0		0		0		ns	9
Data-in hold time	t_{DH}	15		20		25		ns	9
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	60		75		90		ns	
Refresh period (1024 cycles)	t_{REF}		16		16		16	ms	
Write command set-up time	t_{WCS}	0		0		0		ns	7
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	20		25		30		ns	7
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	80		100		120		ns	7
Column address to $\overline{W}$ delay time	t_{AWD}	40		50		60		ns	7
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	t_{CSR}	10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	t_{CHR}	30		30		30		ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	0		0		0		ns	
Refresh counter test $\overline{CAS}$ precharge time	t_{CPT}	40		50		60		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		40		50		60	ns	3
Fast Page mode cycle time	t_{PC}	50		60		70		ns	
$\overline{CAS}$ precharge time (Fast page mode)	t_{CP}	10		10		15		ns	
Fast page mode read-modify-write	t_{PRWC}	75		90		105		ns	
$\overline{RAS}$ pulse width (Fast page mode)	t_{RASP}	80	200,000	100	200,000	120	200,000	ns	
Write command set-up time (Test mode in)	t_{WTS}	10		10		10		ns	
Write command hold time (Test mode in)	t_{WTH}	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	t_{WRP}	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	t_{WRH}	10		10		10		ns	

NOTES

1. An initial pause of 200μs is required after power up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max), and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$(max).
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
7. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data output will remain open circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$(min) and $t_{RWD} \geq t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$ (min), then the cycle is a read-write cycle and the data output will contain data read from the selected cell. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
8. Either t_{RCH} or t_{RRH} must be satisfied a read cycle.
9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
10. Operation within the t_{RAD} (max) limit insures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled by t_{AA}.

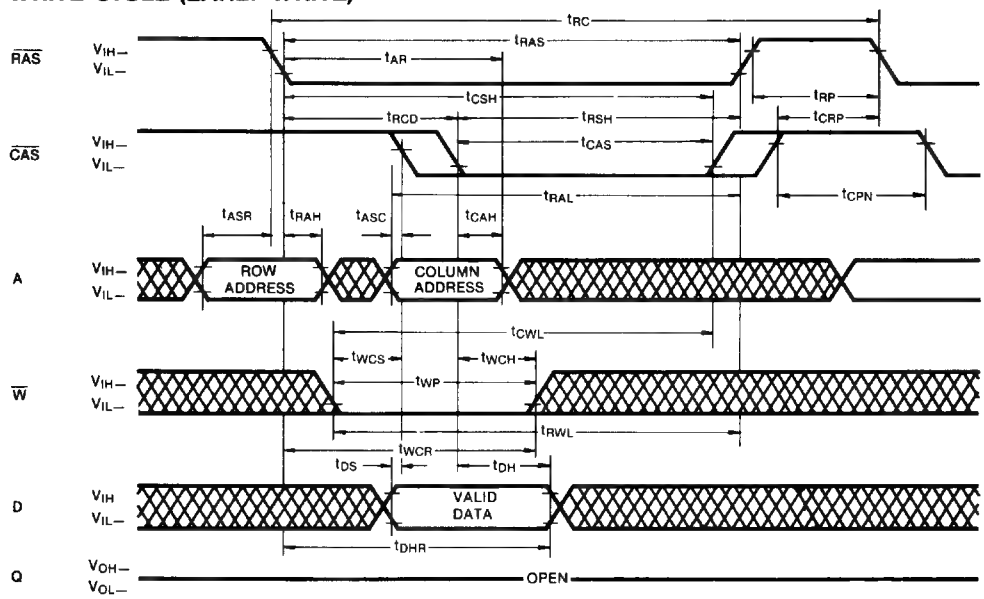
TIMING DIAGRAMS

READ CYCLE

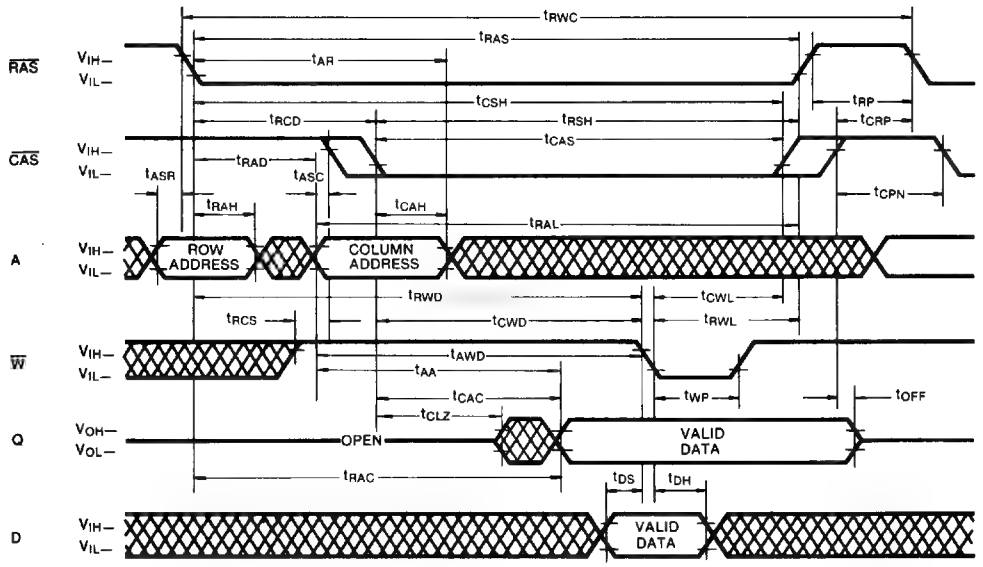


TIMING DIAGRAMS (Continued)

WRITE CYCLE (EARLY WRITE)

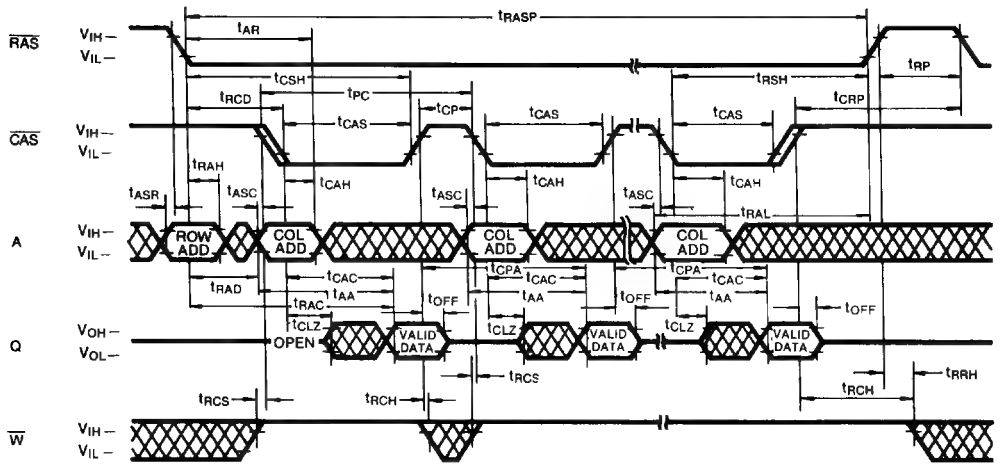


READ-WRITE/READ-MODIFY-WRITE CYCLE

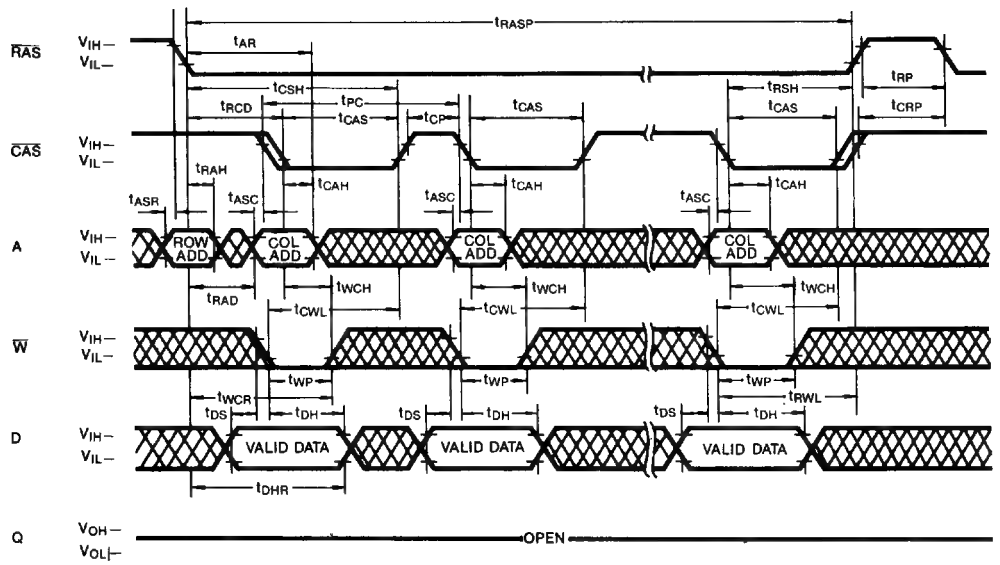


TIMING DIAGRAMS

FAST PAGE MODE READ CYCLE



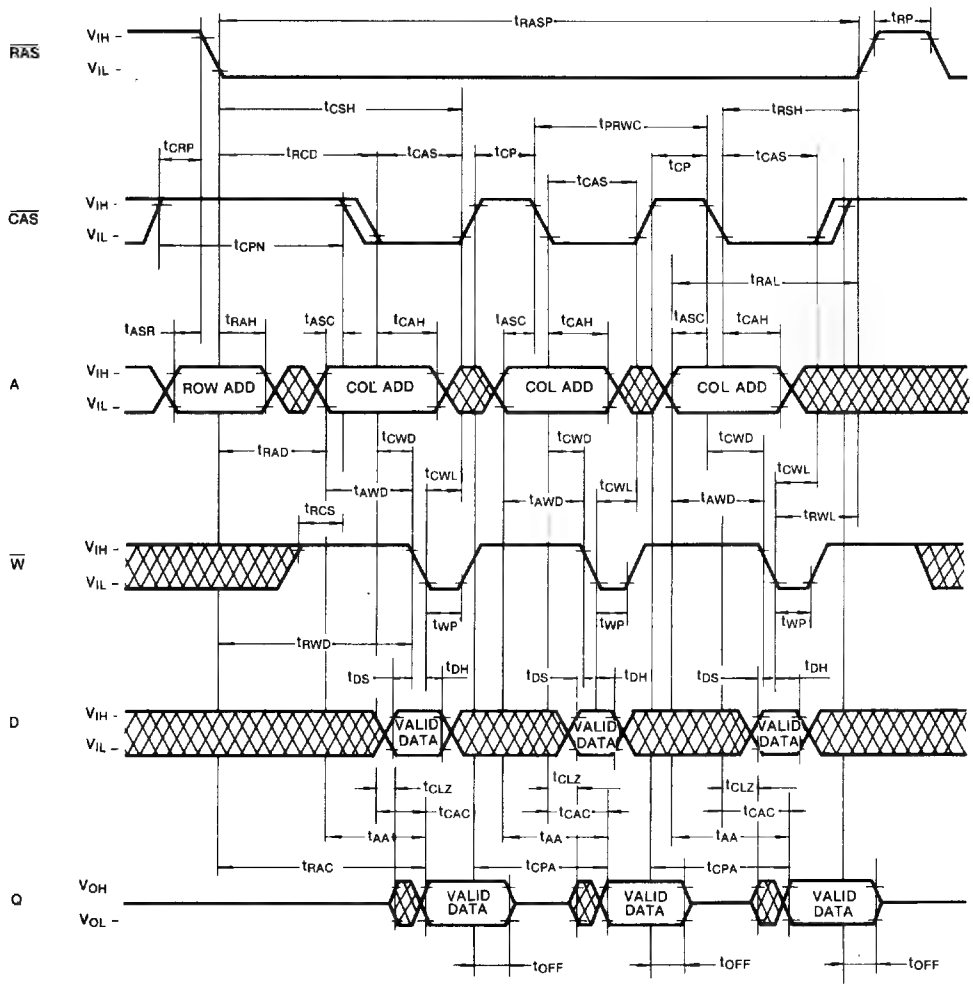
FAST PAGE MODE WRITE CYCLE



DON'T CARE

TIMING DIAGRAMS (Continued)

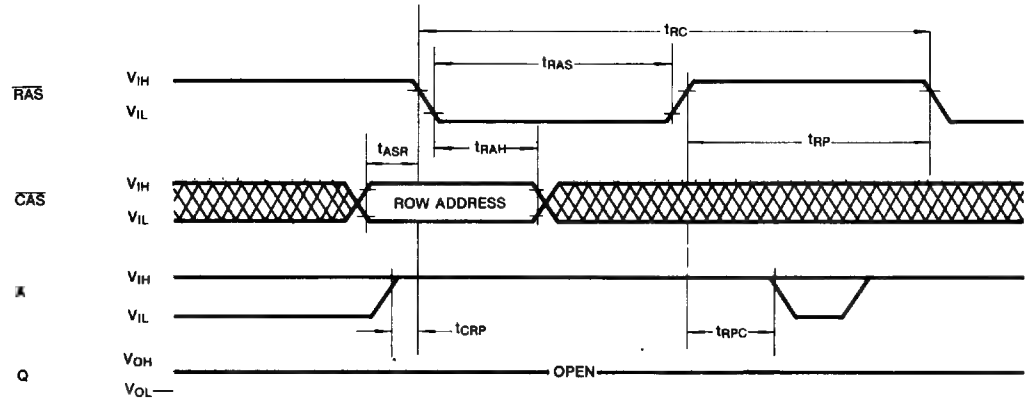
FAST PAGE MODE READ-WRITE CYCLE



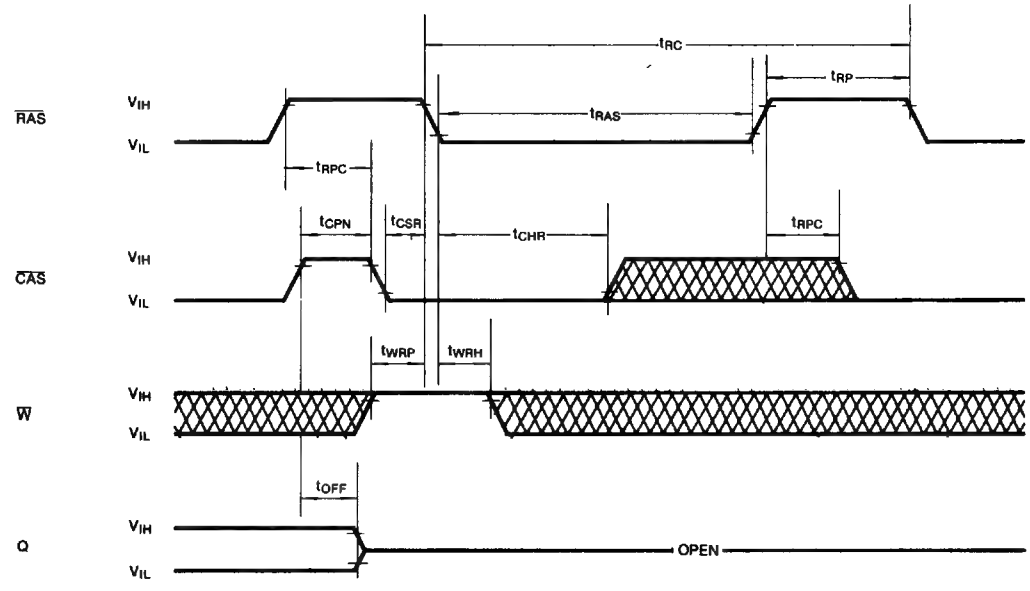
TIMING DIAGRAMS (Continued)

$\overline{RAS}$-ONLY REFRESH CYCLE

Note: $\overline{W}$, D, A_{10} = Don't Care

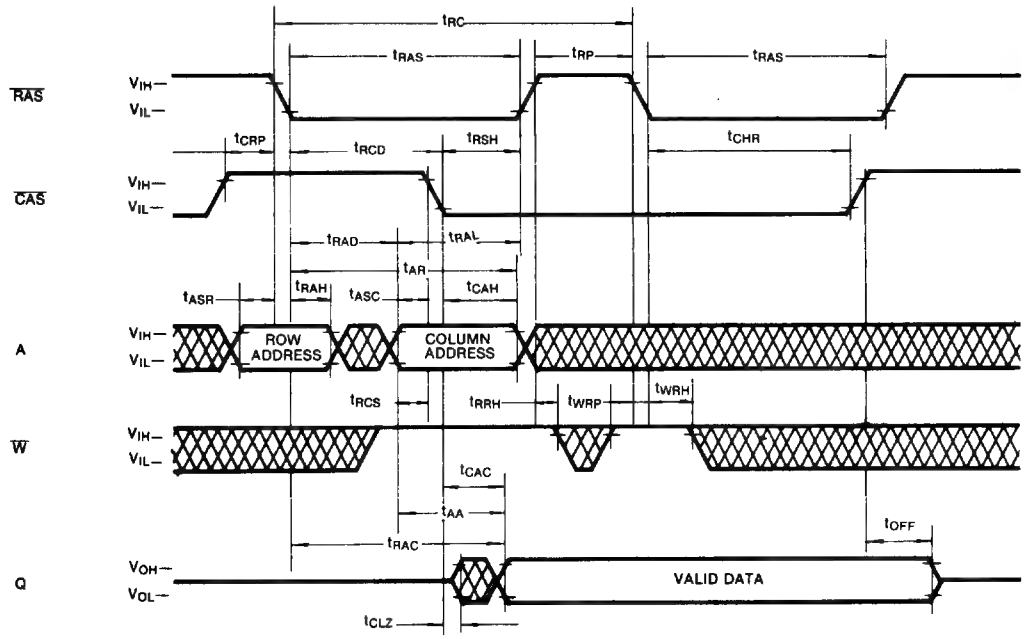


$\overline{CAS}$-BEFORE $\overline{RAS}$-REFRESH CYCLE

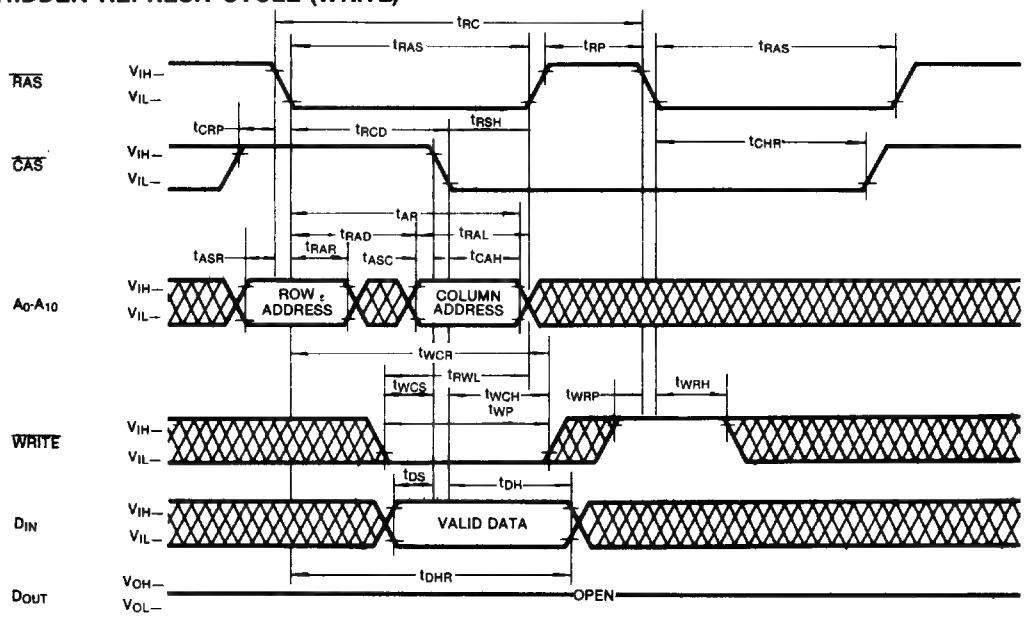


TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)

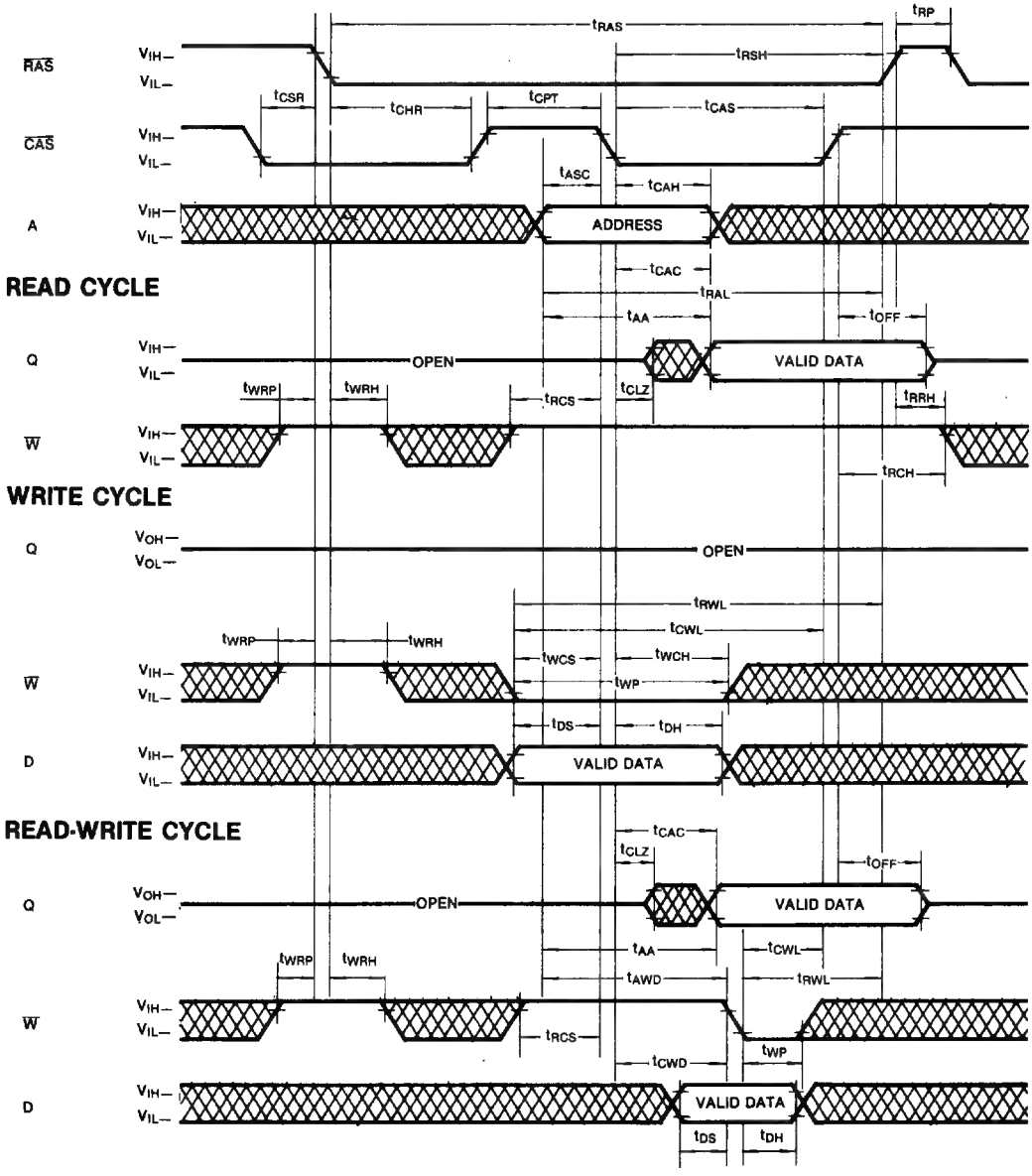


HIDDEN REFRESH CYCLE (WRITE)



TIMING DIAGRAMS (Continued)

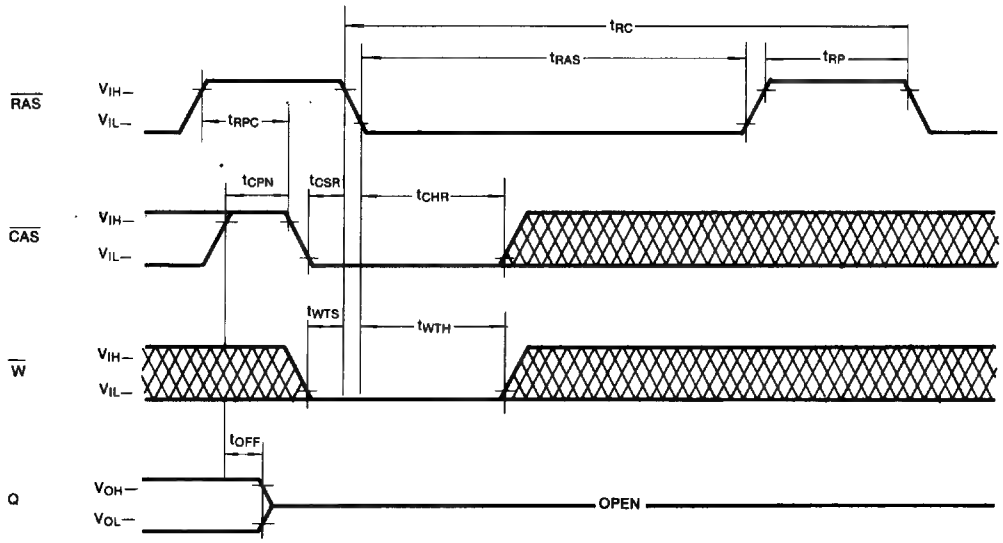
$\overline{CAS}$-BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



TIMING DIAGRAMS (Continued)

TEST MODE IN CYCLE

NOTE: D, Address: Don't Care



DON'T CARE

KM41C4000 OPERATION

Device Operation

The KM41C4000 contains 4,194,304 memory locations. Twenty two address bits are required to address a particular memory location. Since the KM41C4000 has only 11 address input pins, time multiplexed addressing is used to input 11 row and 11 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{RAS}$), the column address strobe ($\overline{CAS}$) and the valid row and column address inputs.

Operation of the KM41C4000 begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. Then the address on the 11 address input pins is changed from a row address to a column address and is strobed in by $\overline{CAS}$. This is the beginning of any KM41C4000 cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both $\overline{RAS}$ and $\overline{CAS}$ have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time (tRP) requirement.

$\overline{RAS}$ and $\overline{CAS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths are specified by tRAS(min) and tCAS(min) respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, tRP, has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM41C4000 begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input($\overline{W}$) high during a $\overline{RAS}$/$\overline{CAS}$ cycle. The access time is normally specified with respect to the falling edge of $\overline{RAS}$. But the access time also depends on the falling edge of $\overline{CAS}$ and on the valid column address transition.

If $\overline{CAS}$ goes low before tRCD(max) and if the column address is valid before tRAD(max) then the access time to valid data is specified by tRAC(min). However, if $\overline{CAS}$ goes low after tRCD(max) or if the column address becomes valid after tRAD(max), access is specified by tCAC or tAA. In order to achieve the minimum access time, tRAC(min), it is necessary to meet both tRCD(max) and tRAD(max).

Write

The KM41C4000 can perform early write, late write and read-modify-write cycles. The difference between these cycles is in the state of data-out and is determined by the timing relationship between W and $\overline{CAS}$. In any type of write cycle, Data-in must be valid at or before the falling edge of $\overline{W}$ or $\overline{CAS}$, whichever is later.

Early Write: An early write cycle is performed by bringing $\overline{W}$ low before $\overline{CAS}$. The data at the data input pin (D) is written into the addressed memory cell. Throughout the early write cycle the output remains in the Hi-Z state. This cycle is good for common I/O applications because the data-in and data-out pins may be tied together without bus contention.

Read-Modify-Write: In this cycle, valid data from the addressed cell appears at the output before and during the time that data is being written into the same cell location. This cycle is achieved by bringing $\overline{W}$ low after $\overline{CAS}$ and meeting the data sheet read-modify-write cycle timing requirements. This cycle requires using a separate I/O to avoid bus contention.

Late Write: If $\overline{W}$ is brought low after $\overline{CAS}$, a late write cycle will occur. The late write cycle is very similar to the read-modify-write cycle except that the timing parameters, tCWD and tAWD are not necessarily met. The state of data-out is indeterminate since the output can be either Hi-Z or contain data depending on the timing conditions. This cycle requires a separate I/O to avoid bus contention.

Data Output

The KM41C4000 has a tri-state output buffer which is controlled by $\overline{CAS}$. Whenever $\overline{CAS}$ is high (VIH) the output is in the high impedance (Hi-Z) state. In any cycle in which valid data appears at the output, the output goes into the low impedance state in a time specified by tCLZ after the falling edge of $\overline{CAS}$. Invalid data may be present at the output during the time after tCLZ and before the valid data appears at the output. The timing parameters tCAC, tRAC and tAA specify when the valid data will be present at the output. The valid data remains at the output until $\overline{CAS}$ returns high. This is true even if a new $\overline{RAS}$ cycle occurs (as in hidden refresh). Each of the KM41C4000 operating cycles is listed below after the corresponding output state produced by the cycle.

DEVICE OPERATION (Continued)

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Fast Page Mode Read, Fast Page Mode Read-Modify-Write.

Hi-Z Output State: Early Write, $\overline{RAS}$-only Refresh, Fast Page Mode Write, $\overline{CAS}$-before-$\overline{RAS}$ Refresh, $\overline{CAS}$-only cycle.

Indeterminate Output State: Delayed Write

Refresh

The data in the KM41C4000 is stored on a tiny capacitor within each memory cell. Due to leakage the data may leak off after a period of time. To maintain data integrity it is necessary to refresh each of the rows every 16 ms. There are several ways to accomplish this.

$\overline{RAS}$-Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. This cycle must be repeated for each of the 1,024 row addresses, (A0-A9). The state of address A10 is ignored during refresh.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh: The KM41C4000 has $\overline{CAS}$-before-$\overline{RAS}$ on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{CAS}$ is held low for the specified set up time (tCSR) before $\overline{RAS}$ goes low, the on-chip refresh circuitry is enabled. An internal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next CAS-before-$\overline{RAS}$ refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the $\overline{CAS}$ active time and cycling $\overline{RAS}$. The KM41C4000 hidden refresh cycle is actually a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter.

Other Refresh Methods: It is also possible to refresh the KM41C4000 by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in that row are automatically refreshed. There are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh is the preferred method.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle

A special timing sequence using the $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle provides a convenient method of verifying the functionality of the $\overline{CAS}$-before-$\overline{RAS}$ refresh activated circuitry. The cycle begins as a $\overline{CAS}$-before-$\overline{RAS}$ refresh operation. Then, if $\overline{CAS}$ is brought high and then low again while $\overline{RAS}$ is held low, the read and write operations are enabled. In this mode, the row address bits A0 through A9 are supplied by the on-chip refresh counter. The A10 bit is set low internally.

Fast Page Mode

The KM41C4000 has Fast Page mode capability which provides high speed read, write or read-modify-write access to all memory cells within a selected row. These cycles may be mixed in any order. A fast page mode cycle begins with a normal cycle. Then, while $\overline{RAS}$ is kept low to maintain the row address, $\overline{CAS}$ is cycled to strobe in additional column addresses. This eliminates the time required to set up and strobe sequential row addresses for the same page.

Power-up

If $\overline{RAS} = V_{SS}$ during power-up, the KM41C4000 could begin an active cycle. This condition results in higher than necessary current demands from the power supply during power-up. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{CC} during power-up or be held at a valid VIH in order to minimize the power-up current.

An initial pause of 200 μsec is required after power-up followed by 8 initialization cycles before proper device operation is assured. Eight initialization cycles are also required after any 16 msec period in which there are no $\overline{RAS}$ cycles. An initialization cycle is any cycle in which $\overline{RAS}$ is cycled.

Termination

The lines from the TTL driver circuits to the KM41C4000 inputs act like unterminated transmission lines resulting in significant positive and negative overshoot at the inputs. To minimize overshoot it is advisable to terminate the input lines and to keep them as short as possible. Although either series or parallel termination may be used, series termination is generally recommended since it is simple and draws no additional power. It consists of a resistor in series with the input line placed close to the KM41C4000 input pin. The optimum value depends on the board layout. It must be determined experimentally and is usually in the range of 20 to 40 ohms.

DEVICE OPERATION (Continued)

Board Layout

It is important to lay out the power and ground lines on memory boards in such a way that switching transient effects are minimized. The recommended methods are gridded power and ground lines or separate power and ground planes. The power and ground lines act like transmission lines to the high frequency transients generated by DRAMS. The impedance is minimized if all the power supply traces to all the DRAMS run both horizontally and vertically and are connected at each intersection or better yet if power and ground planes are used.

Address and control lines should be as short as possible to avoid skew. In boards with many DRAMS these lines should fan out from a central point like a fork or comb rather than being connected in a serpentine pattern. Also the control logic should be centrally located on large memory boards to facilitate the shortest possible address and control lines to all the DRAMS.

Decoupling

The importance of proper decoupling can not be over emphasized. Excessive transient noise or voltage droop on the V_{CC} line can cause loss of data integrity (soft errors). It is recommended that the total combined voltage changes over time in the VCC to VSS voltage (measured at the device pins) should not exceed 500mV.

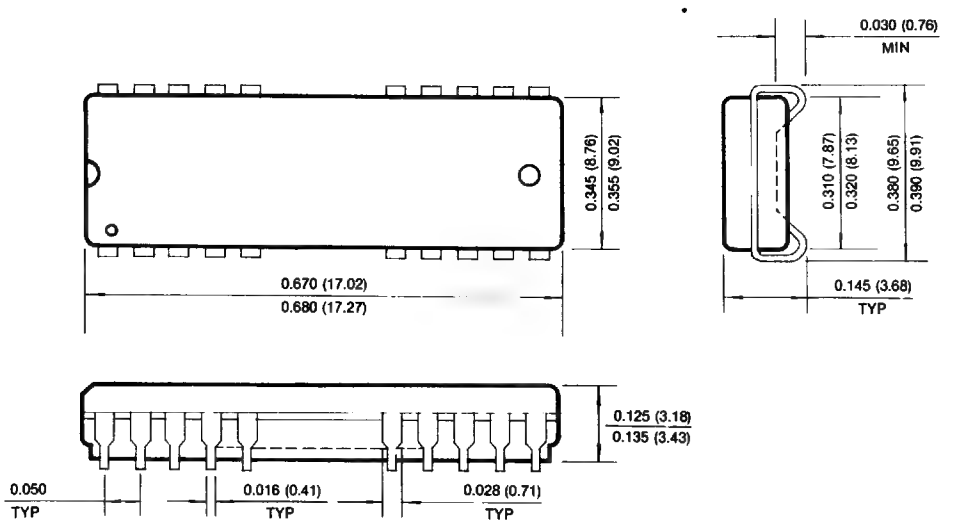
A high frequency 0.3μF ceramic decoupling capacitor should be connected between the V_{CC} and ground pins of each KM41C4000 using the shortest possible traces. These capacitors act as a low impedance shunt for the high frequency switching transients generated by the KM41C4000 and they supply much of the current used by the KM41C4000 during cycling.

In addition, a large tantalum capacitor with a value of 47μF to 100μF should be used for bulk decoupling to recharge the 0.3μF capacitors between cycles, thereby reducing power line droop. The bulk decoupling capacitor should be placed near the point where the power traces meet the power grid or power plane. Even better results may be achieved by distributing more than one tantalum capacitor around the memory array.

PACKAGE DIMENSIONS

20-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



1M x 4 Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

- **Performance range:**

	t_{RAC}	t_{CAC}	t_{RC}
KM44C1000-8	80ns	20ns	160ns
KM44C1000-10	100ns	25ns	190ns
KM44C1000-12	120ns	30ns	220ns

- **Fast Page Mode operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **8-bit fast parallel test mode**
- **TTL compatible inputs and output**
- **Early Write or output Enable Controlled Write**
- **Single +5V ± 10% power supply**
- **1024 cycles/16ms refresh**
- **JEDEC standard pinout**
- **Available in Plastic SOJ**

GENERAL DESCRIPTION

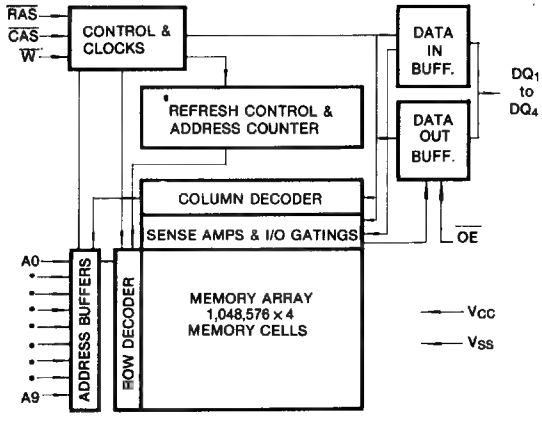
The Samsung KM44C1000 is a CMOS high speed 1,048,576 x 4 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes and mini computers, graphics and high performance microprocessor systems.

The KM44C1000 features Fast Page Mode operation which allows high speed random access of memory cells within the same row.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only Refresh. All inputs and output are fully TTL compatible.

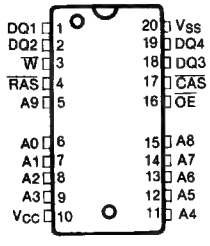
The KM44C1000 is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION

- **KM44C1000**



Pin Name	Pin Function
A_0-A_9	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Output Enable
DQ_1-DQ_4	Data In/Data Out
V_{CC}	Power (+5V)

256K x 4 Bit CMOS Multiport DRAM

FEATURES

- **Dual Port Architecture**
  256K x 4 bits Dynamic RAM port (RAM)
  512K x 4 bits Serial Access Memory port (SAM)
- **Performance range:**

	t_{RAC}	t_{CAC}	t_{RC}
RAM access time (t_{RAC})	80ns	100ns	120ns
$\overline{RAM}$ access time (t_{CAC})	20ns	25ns	30ns
$\overline{RAM}$ cycle time (t_{RC})	165ns	190ns	220ns
RAM page mode cycle (t_{PC})	50ns	55ns	70ns
SAM access time	20ns	25ns	35ns
SAM cycle time	25ns	30ns	40ns
RAM active current	80ns	65mA	55mA
SAM active current	45ns	40mA	35mA
RAM & SAM standby	3mA	3mA	3mA

- **Fast Page Mode**
- **RAM Read, Write, Read-Modify-Write**
- **Serial Read and Serial Write**
- **Read Transfer and Write Transfer**
- **Write per Bit masking on RAM write cycles**
- **$\overline{CAS}$-before-$\overline{RAS}$, $\overline{RAS}$-only and Hidden Refresh**
- **Common data I/O using 3-state RAM output control**
- **All inputs and outputs TTL and CMOS compatible**
- **Refresh: 512 cycles/8ms**
- **Single +5V ± 10% supply voltage**
- **Plastic 28-pin 400 mil DIP and SOJ, 28-pin ZIP**

Pin Name	Pin Function
SC	Serial Clock
SDQ_0-SDQ_3	Serial Data Input-Output
$\overline{DT/OE}$	Data Transfer Output Enable
$\overline{WB/WE}$	Write Mask Enable/Write Enable
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
W_0/DQ_0-W_3/DQ_3	Data Write Mask/Input-Output
$\overline{SE}$	Serial Output Enable
A_0-A_8	Row, Column, Tap Address
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connect

GENERAL DESCRIPTION

The Samsung KM424C256 is a CMOS 256K x 4 bit Dual Port DRAM. It consists of a 256K x 4 dynamic RAM port and 512 x 4 static serial access memory (SAM) port. The RAM and SAM ports operate asynchronously except during data transfer between the ports.

The RAM array consists of 512 rows of 2048 bits. It operates like a conventional 256K x 4 CMOS DRAM. The RAM port has a write per bit mask capability.

The SAM port consists of four 512 bit high speed shift registers that are connected to the RAM array through a 2048 bit data transfer gate.

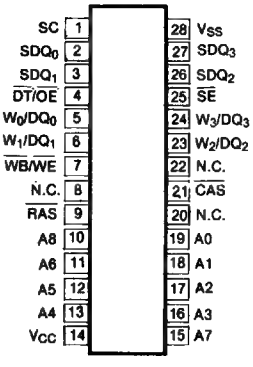
Data may be internally transferred bi-directionally between the RAM and SAM ports using either conventional read or write transfers.

Refresh is accomplished by familiar DRAM refresh modes. The KM424C256 supports $\overline{RAS}$-only, Hidden, and $\overline{CAS}$-before-$\overline{RAS}$ refresh for the RAM memory array port. The SAM port does not require refresh.

All inputs and I/O's are TTL and CMOS level compatible. All address lines and Data Inputs are latched on chip to simplify system design. The outputs are unlatched to allow greater system flexibility.

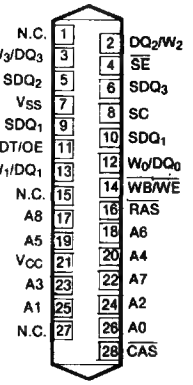
PIN CONFIGURATION

- **KM424C256P/J**



DIP & SOJ

- **KM424C256Z**



ZIP

256K x 8 Bit DRAM SIP and SIMM Memory Modules

FEATURES

- **262,144 x 8-bit Organization**
- **Performance range:**

	t_{RAC}	t_{CAC}	t_{RC}
KMM48256-12	120ns	60ns	230ns
KMM58256-12	120ns	60ns	230ns
KMM48256-15	150ns	75ns	260ns
KMM58256-15	150ns	75ns	260ns

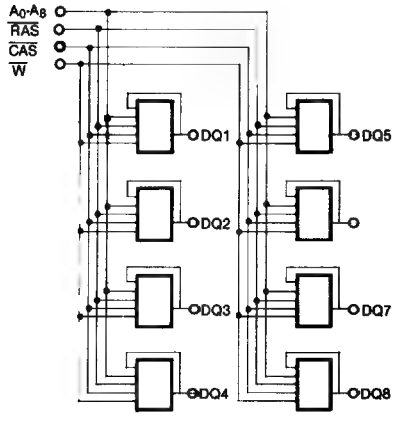
- **Page Mode capability: KMM48256 and KMM58256**
- **$\overline{CAS}$-before-$\overline{RAS}$ Refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **TTL compatible inputs and outputs**
- **Single +5V ± 10% power supply**
- **256 cycles/4ms refresh**

GENERAL DESCRIPTION

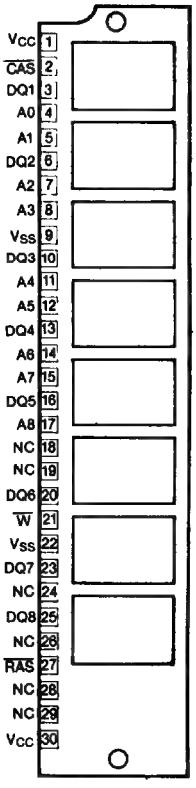
The Samsung KMM48256 and KMM58256 are 256K x 8 dynamic RAM high density memory modules. Samsung's 256K x 8 memory modules consists of eight KM41256AJ DRAMs in 18-pin PLCC packages mounted on a 30 pin glass-epoxy substrate. A 0.22μF decoupling capacitor is mounted under each DRAM.

The 256K x 8 DRAM modules are available in two package styles. The KMM48256 is SIPs with leads suitable for through hole mounting or for mounting in a socket. The KMM58256 is SIMMs with edge connections and are intended for mounting into 30 pin edge connector sockets.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



PART NUMBERS

KMM48256-12	120ns	SIP	Page Mode
KMM48256-15	150ns	SIP	Page Mode
KMM58256-12	120ns	SIMM	Page Mode
KMM58256-15	150ns	SIMM	Page Mode

PIN NAMES

Pin Name	Pin Function
A_0-A_8	Address Inputs
DQ	Data In/Out
$\overline{W}$	Read/Write Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Units
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7.0	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	−1 to +7.0	V
Storage Temperature	T_{stg}	−55 to +150	°C
Power Dissipation	P_D	8	W
Short Circuit Output Current	I_{OS}	50	mA

*Note: Permanent device damage may occur of ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS}, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC} + 1	V
Input Low Voltage	V_{IL}	−1	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Min	Max	Units
OPERATING CURRENT* ($\overline{RAS}$ and $\overline{CAS}$ cycling; @t_{RC} = min)	KMM48256-12, KMM58256-12	I_{CC1}	—	600	mA
	KMM48256-15, KMM58256-15		—	520	mA
STANDBY CURRENT ($\overline{RAS}$-$\overline{CAS}$ = V_{IH} after 8 RAS cycles min)		I_{CC2}	—	36	mA
$\overline{RAS}$-ONLY REFRESH CURRENT* ($\overline{CAS}$ = V_{IH}, $\overline{RAS}$ cycling @t_{RC} = min.)	KMM48256-12, KMM58256-12	I_{CC3}	—	520	mA
	KMM48256-15, KMM58256-15		—	480	mA
PAGE MODE CURRENT* ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling; @t_{PC} = min)	KMM48256-12, KMM58256-12	I_{CC4}	—	440	mA
	KMM48256-15, KMM58256-15		—	360	mA
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CURRENT* ($\overline{RAS}$ cycling; @t_{RC} = min)	KMM48256-12, KMM58256-12	I_{CC5}	—	520	mA
	KMM48256-15, KMM58256-15		—	480	mA
INPUT LEAKAGE CURRENT (Any input, 0≤V_{IN}≤5.5V, V_{CC} = 5.5V, V_{SS} = 0V, all other pins not under test = 0 volts.)		I_{IL}	−80	80	μA
OUTPUT LEAKAGE CURRENT (Data out is disabled, 0V≤V_{OUT}≤5.5V, V_{CC} = 5.5V, V_{SS} = 0V)		I_{OL}	−10	10	μA
OUTPUT HIGH VOLTAGE LEVEL (I_{OH} = −5mA)		V_{OH}	2.4	—	V
OUTPUT LOW VOLTAGE LEVEL (I_{OL} = 4.2mA)		V_{OL}	—	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC5} are dependent on output loading and cycle rates. Specified values are obtained with the output open I_{CC} is specified as average current.

CAPACITANCE ($T_A = 25°C$)

Parameter	Symbol	Min	Max	Unit
Input capacitance ($A_0 - A_9$)	C_A	—	56	pF
Input capacitance ($\overline{RAS}$)	C_{RAS}	—	64	pF
Input capacitance ($\overline{CAS}$)	C_{CAS}	—	64	pF
Input capacitance ($\overline{W}$)	C_W	—	64	pF
Input capacitance ($DQ_1 - DQ_8$)	C_{DQ}	—	17	pF

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC} = 5.0V \pm 10\%$. See notes 1,2.)
STANDARD OPERATION

Parameter	Symbol	KMM48256-12 KMM58256-12		KMM48256-15 KMM58256-15		Unit	Notes
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	230		260		ns	
Access time from $\overline{RAS}$	t_{RAC}		120		150	ns	3,4
Access time from $\overline{CAS}$	t_{CAC}		60		75	ns	3,5
Output buffer turn-off delay time	t_{OFF}	0	30	0	40	ns	6
Transition time (rise and fall)	t_T	3	50	3	50	ns	
$\overline{RAS}$ precharge time	t_{RP}	100		100		ns	
$\overline{RAS}$ pulse width	t_{RAS}	120	10,000	150	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	60		75		ns	
$\overline{CAS}$ precharge time (all cycles except page mode)	t_{CPN}	50		60		ns	
$\overline{CAS}$ pulse width	t_{CAS}	60	10,000	75	10,000	ns	
$\overline{CAS}$ hold time	t_{CSH}	120		150		ns	
$\overline{RAS}$ to CAS delay time	t_{RCD}	25	60	25	75	ns	4
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		ns	
Row address set-up time	t_{ASR}	0		0		ns	
Row address hold time	t_{RAH}	15		15		ns	
Column address set-up time	t_{ASC}	0		0		ns	
Column address hold time	t_{CAH}	20		25		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	80		100		ns	
Read command set-up time	t_{RCS}	0		0		ns	
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	20		20		ns	
Write command set-up time	t_{WCS}	0		0		ns	
Write command hold time	t_{WCH}	40		45		ns	
Write command pulse width	t_{WP}	40		45		ns	

STANDARD OPERATION (Continued)

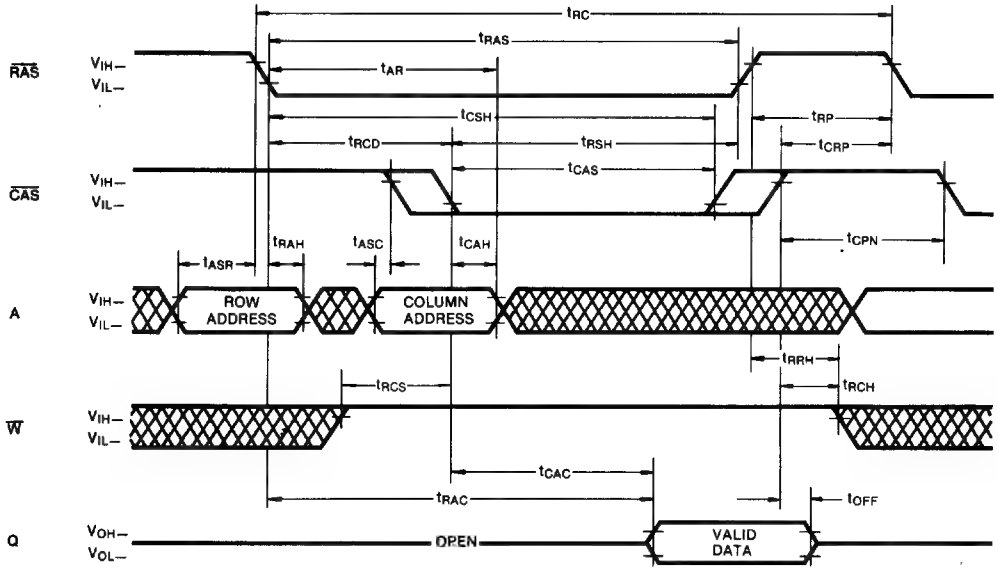
Parameter	Symbol	KMM48256-12 KMM58256-12		KMM48256-15 KMM58256-15		Units	Notes
		Min	Max	Min	Max		
Write command to $\overline{RAS}$ lead time	t_{RWL}	40		45		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	40		45		ns	
Data-in set-up time	t_{DS}	0		0		ns	
Data-in hold time	t_{DH}	40		45		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	100		120		ns	
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	100		120		ns	
Refresh period (256 cycles)	t_{REF}		4		4	ms	
$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	25		30		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	55		60		ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ active time	t_{RPC}	20		20		ns	
Page mode cycle time	t_{PC}	120		145		ns	
$\overline{CAS}$ precharge time (page mode only)	t_{CP}	50		60		ns	

NOTES

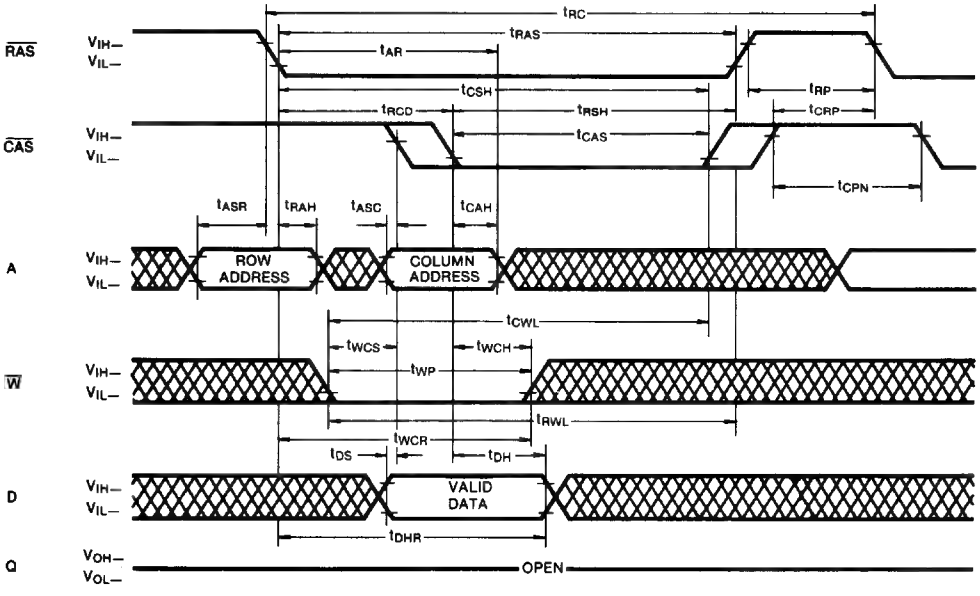
1. An initial pause of 100μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved. Before using the internal refresh counter, 8 $\overline{CAS}$-before-$\overline{RAS}$ refresh initialization cycles are required (instead of 8 $\overline{RAS}$ cycles).
2. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} (min) and V_{IL} (max), and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.

TIMING DIAGRAMS

READ CYCLE

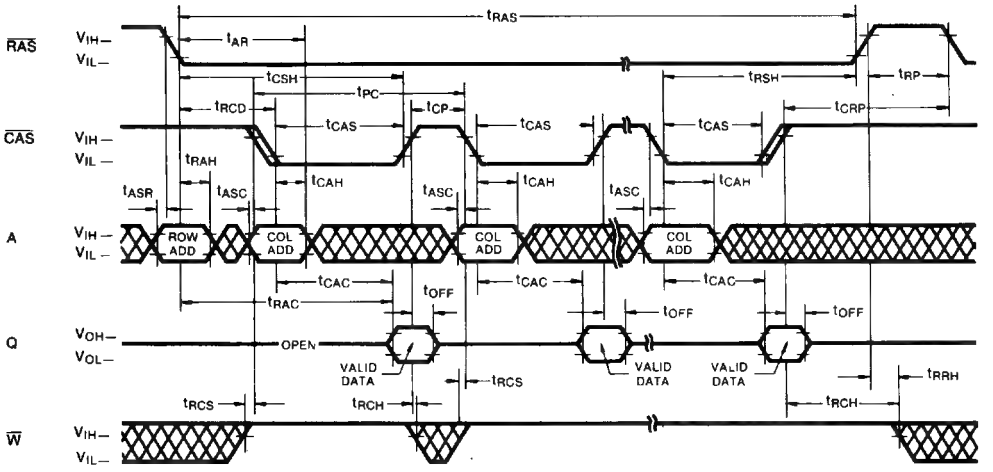


WRITE CYCLE (EARLY WRITE)

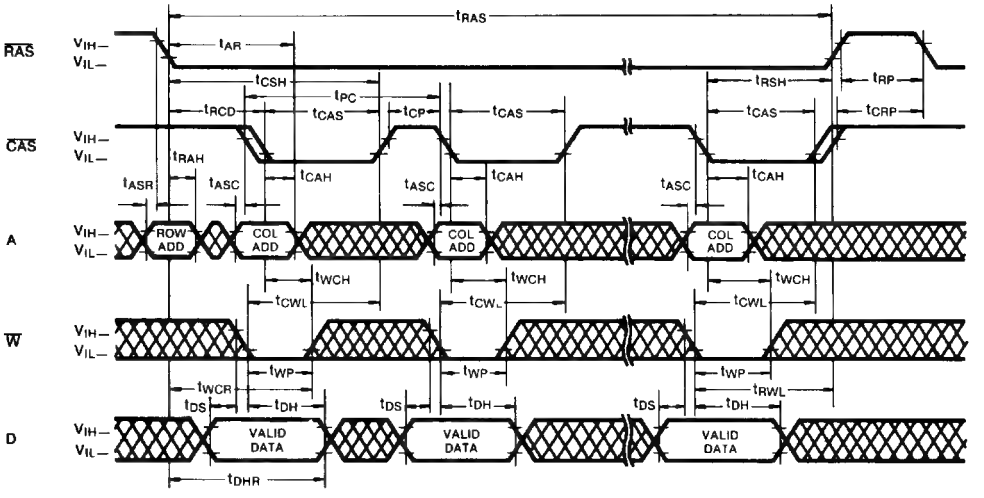


TIMING DIAGRAMS (Continued)

PAGE MODE READ CYCLE



PAGE MODE WRITE CYCLE

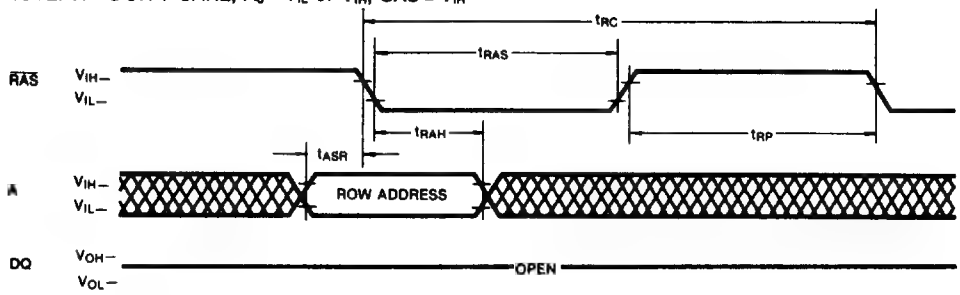


DON'T CARE

TIMING DIAGRAMS (Continued)

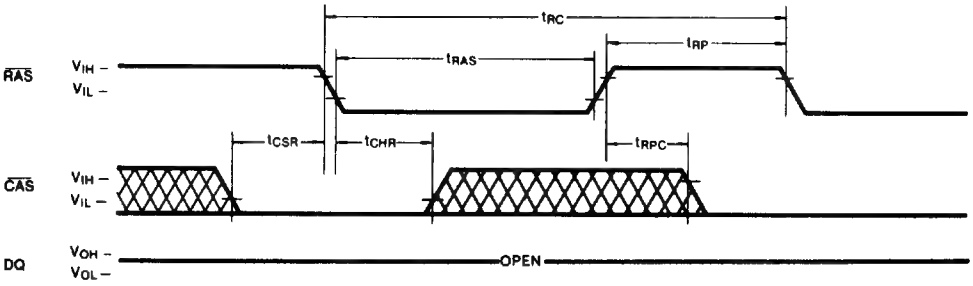
$\overline{RAS}$-ONLY REFRESH CYCLE

NOTE: $\overline{W}$ = DON'T CARE, $A_8 = V_{IL}$ or V_{IH}, $\overline{CAS} = V_{IH}$

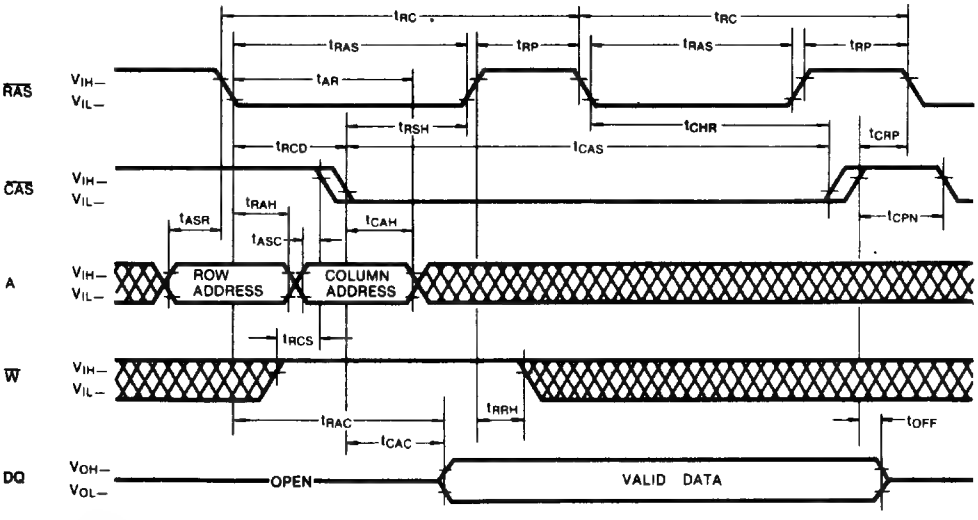


$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

NOTE: ADDRESS, $\overline{W}$ = DON'T CARE



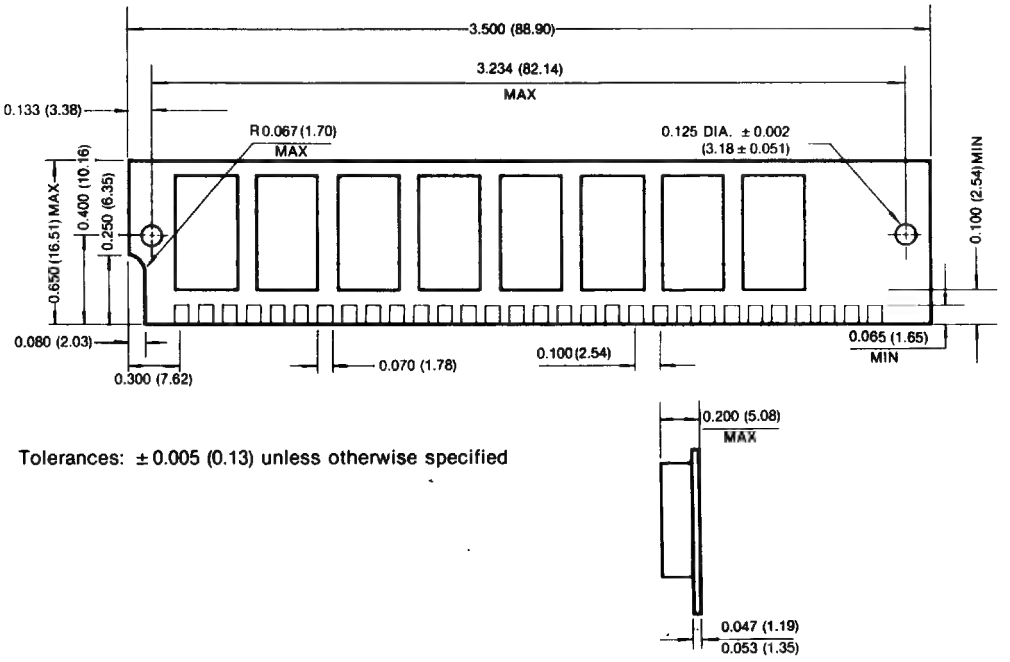
HIDDEN REFRESH CYCLE



PACKAGE DIMENSIONS

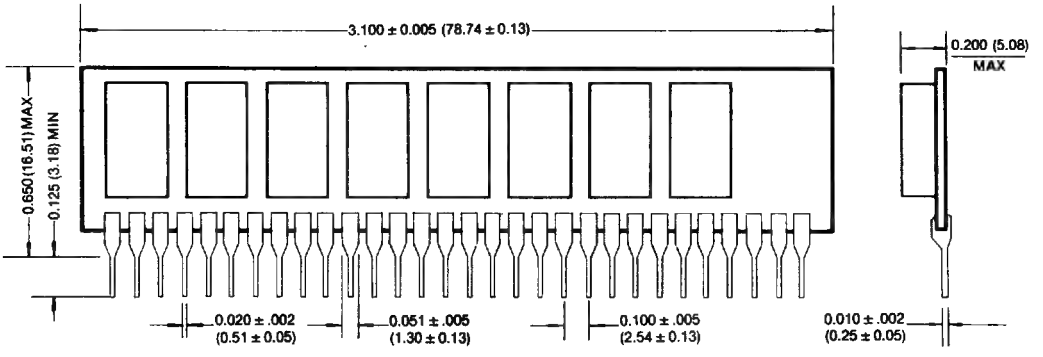
KMM58256 (256K x 8 SIMM)

Units: Inches (millimeters)



Tolerances: ± 0.005 (0.13) unless otherwise specified

KMM48256 (256K x 8 SIP)



256K x 9 Bit DRAM SIP and SIMM Memory Modules

FEATURES

- **262,144 x 9-bit Organization**
- **Ninth device has separate D, Q and $\overline{CAS}$ for Parity applications.**
- **Performance range:**

	t_{RAC}	t_{CAC}	t_{RC}
KMM49256-12	120ns	60ns	230ns
KMM59256-12	120ns	60ns	230ns
KMM49256-15	150ns	75ns	260ns
KMM59256-15	150ns	75ns	260ns

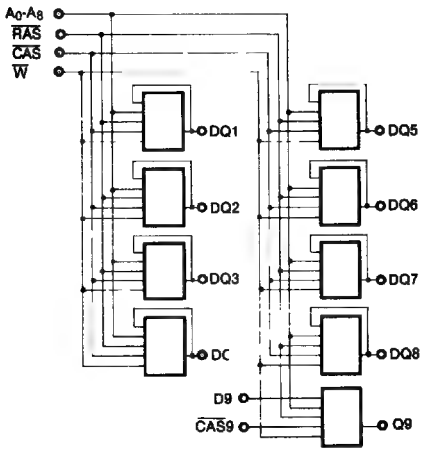
- **Page Mode capability: KMM49256 and KMM59256**
- **$\overline{CAS}$-before-$\overline{RAS}$ Refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **TTL compatible inputs and outputs**
- **Single +5V ± 10% power supply**
- **256 cycles/4ms refresh**

GENERAL DESCRIPTION

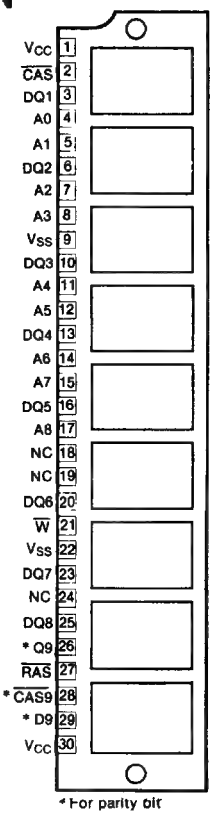
The Samsung KMM49256 and KMM59256 is 256K x 9 dynamic RAM high density memory modules. The ninth bit is generally used for parity and is controlled by $\overline{CAS}_9$. Samsung's 256K x 9 memory modules consists of nine KM41256AJ DRAMs in 18-pin PLCC packages mounted on a 30 pin glass-epoxy substrate. A 0.22μF decoupling capacitor is mounted under each DRAM.

The 256K x 9 DRAM modules are available in two package styles. The KMM49256 is SIPs with leads suitable for through hole mounting or for mounting in a socket. The KMM59256 is SIMMs with edge connections and are intended for mounting into 30 pin edge connector sockets.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



* For parity bit

PIN NAMES

Pin Name	Pin Function
A_0-A_8	Address Inputs
D_9	Data In
Q_9	Data Out
DQ	Data In/Out
$\overline{W}$	Read/Write Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{CAS}_9$	Column Address Strobe
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

PART NUMBERS

KMM49256-12	120ns	SIP	Page Mode
KMM49256-15	150ns	SIP	Page Mode
KMM59256-12	120ns	SIMM	Page Mode
KMM59256-15	150ns	SIMM	Page Mode

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Units
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7.0	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	−1 to +7.0	V
Storage Temperature	T_{stg}	−55 to +150	°C
Power Dissipation	P_D	9	W
Short Circuit Output Current	I_{OS}	50	mA

*Note: Permanent device damage may occur of ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS}, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC} + 1	V
Input Low Voltage	V_{IL}	−1	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Min	Max	Units
OPERATING CURRENT* ($\overline{RAS}$ and $\overline{CAS}$ cycling; @t_{RC} = min)	KMM49256-12, KMM59256-12	I_{CC1}	—	675	mA
	KMM49256-15, KMM59256-15		—	585	mA
STANDBY CURRENT ($\overline{RAS}$-$\overline{CAS}$ = V_{IH} after 8 $\overline{RAS}$ cycles min)		I_{CC2}	—	41	mA
$\overline{RAS}$-ONLY REFRESH CURRENT* ($\overline{CAS}$= V_{IH} $\overline{RAS}$ cycling; @t_{RC} = min)	KMM49256-12, KMM59256-12	I_{CC3}	—	585	mA
	KMM49256-15, KMM59256-15		—	540	mA
PAGE MODE CURRENT* ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling; @t_{PC} = min)	KMM49256-12, KMM59256-12	I_{CC4}	—	495	mA
	KMM49256-15, KMM59256-15		—	405	mA
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CURRENT* ($\overline{RAS}$ cycling; @t_{RC} = min)	KMM49256-12, KMM59256-12	I_{CC5}	—	585	mA
	KMM49256-15, KMM59256-15		—	540	mA
INPUT LEAKAGE CURRENT (D_9, $\overline{CAS_9}$ input, 0≤V_{IN}≤5.5V, V_{CC} = 5.5V, V_{SS} = 0V, all other pins not under test = 0 volts.)		I_{IL1}	−10	10	μA
INPUT LEAKAGE CURRENT (A, $\overline{RAS}$, $\overline{CAS}$, W inputs, 0≤V_{IN}≤5.5V, V_{CC} = 5.5V, V_{SS} = 0V, all other pins not under test = 0 volts.)		I_{IL2}	−90	90	μA
OUTPUT LEAKAGE CURRENT (DQ, Q_9, Data out is disabled, 0V≤V_{OUT}≤5.5V, V_{CC} = 5.5V, V_{SS} = 0V)		I_{OL}	−10	10	μA
OUTPUT HIGH VOLTAGE LEVEL (I_{OH} = −5mA)		V_{OH}	2.4	—	V
OUTPUT LOW VOLTAGE LEVEL (I_{OL} = 4.2mA)		V_{OL}	—	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC5} are dependent on output loading and cycle rates. Specified values are obtained with the output open I_{CC} is specified as average current.

CAPACITANCE ($T_A = 25°C$)

Parameter	Symbol	Min	Max	Unit
Input capacitance ($A_0 - A_8$)	C_A	—	63	pF
Input capacitance ($\overline{RAS}$)	C_{RAS}	—	72	pF
Input capacitance ($\overline{CAS}$)	C_{CAS}	—	64	pF
Input capacitance ($\overline{W}$)	C_W	—	72	pF
Input capacitance ($\overline{CAS_9}$)	C_{CAS9}	—	10	pF
Input capacitance (D_9)	C_{D9}	—	7	pF
Input capacitance (DQ_1-DQ_8)	C_{DQ}	—	17	pF
Output capacitance (Q_9)	C_{Q9}	—	10	pF

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC} = 5.0V \pm 10\%$. See notes 1,2.)

Parameter	Symbol	KMM49256-12 KMM59256-12		KMM49256-15 KMM59256-15		Unit	Notes
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	230		260		ns	
Access time from $\overline{RAS}$	t_{RAC}		120		150	ns	3,4
Access time from $\overline{CAS}$	t_{CAC}		60		75	ns	3,5
Output buffer turn-off delay time	t_{OFF}	0	30	0	40	ns	6
Transition time (rise and fall)	t_T	3	50	3	50	ns	
$\overline{RAS}$ precharge time	t_{RP}	100		100		ns	
$\overline{RAS}$ pulse width	t_{RAS}	120	10,000	150	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	60		75		ns	
$\overline{CAS}$ precharge time (all cycles except page mode)	t_{CPN}	50		60		ns	
$\overline{CAS}$ pulse width	t_{CAS}	60	10,000	75	10,000	ns	
$\overline{CAS}$ hold time	t_{CSH}	120		150		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	25	60	25	75	ns	4
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		ns	
Row address set-up time	t_{ASR}	0		0		ns	
Row address hold time	t_{RAH}	15		15		ns	
Column address set-up time	t_{ASC}	0		0		ns	
Column address hold time	t_{CAH}	20		25		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	80		100		ns	
Read command set-up time	t_{RCS}	0		0		ns	
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	20		20		ns	

STANDARD OPERATION (Continued)

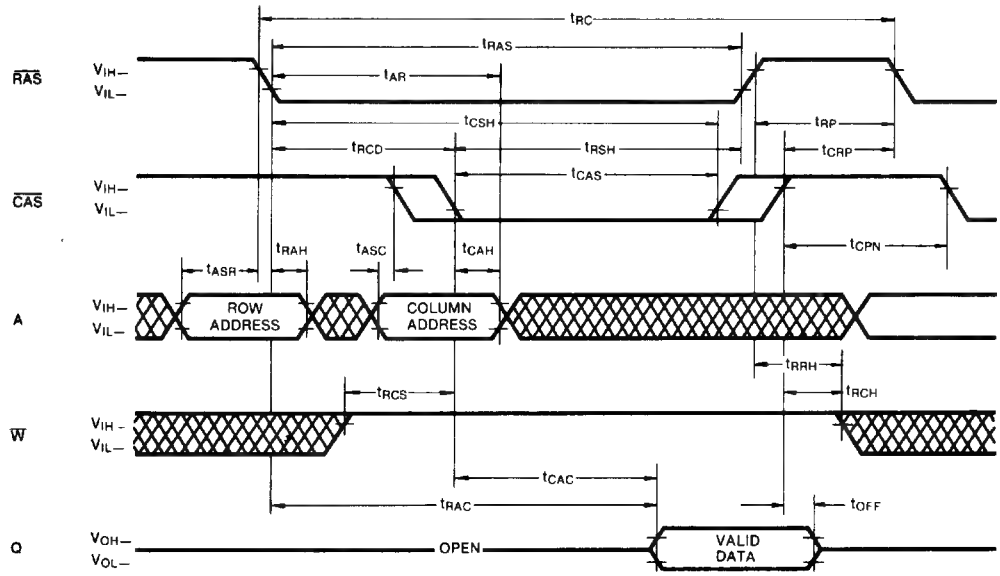
Parameter	Symbol	KMM49256-12 KMM59256-12		KMM49256-15 KMM59256-15		Units	Notes
		Min	Max	Min	Max		
Write command set-up time	t_{WCS}	0		0		ns	
Write command hold time	t_{WCH}	40		45		ns	
Write command pulse width	t_{WP}	40		45		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	40		45		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	40		45		ns	
Data-in set-up time	t_{DS}	0		0		ns	
Data-in hold time	t_{DH}	40		45		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	100		120		ns	
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	100		120		ns	
Refresh period (256 cycles)	t_{REF}		4		4	ms	
$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	25		30		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	55		60		ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ active time	t_{RPC}	20		20		ns	
Page mode cycle time	t_{PC}	120		145		ns	
$\overline{CAS}$ precharge time (page mode only)	t_{CP}	50		60		ns	

NOTES

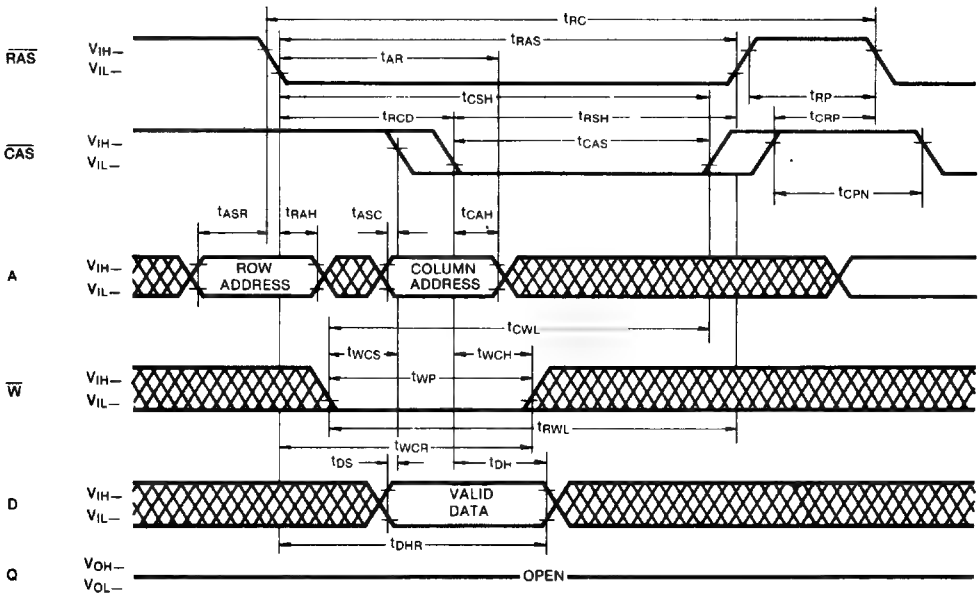
1. An initial pause of 100μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved. Before using the internal refresh counter, 8 $\overline{CAS}$-before-$\overline{RAS}$ refresh initialization cycles are required (instead of 8 $\overline{RAS}$ cycles).
2. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} (min) and V_{IL} (max), and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.

TIMING DIAGRAMS

READ CYCLE



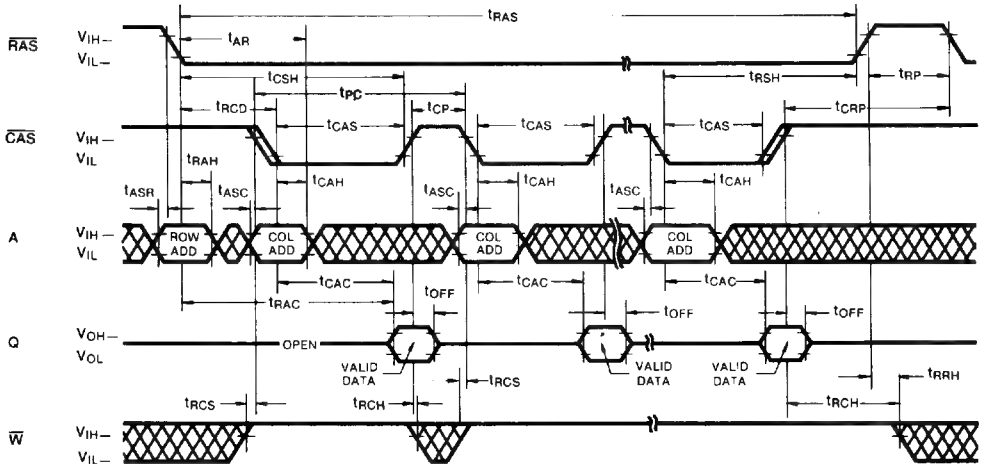
WRITE CYCLE (EARLY WRITE)



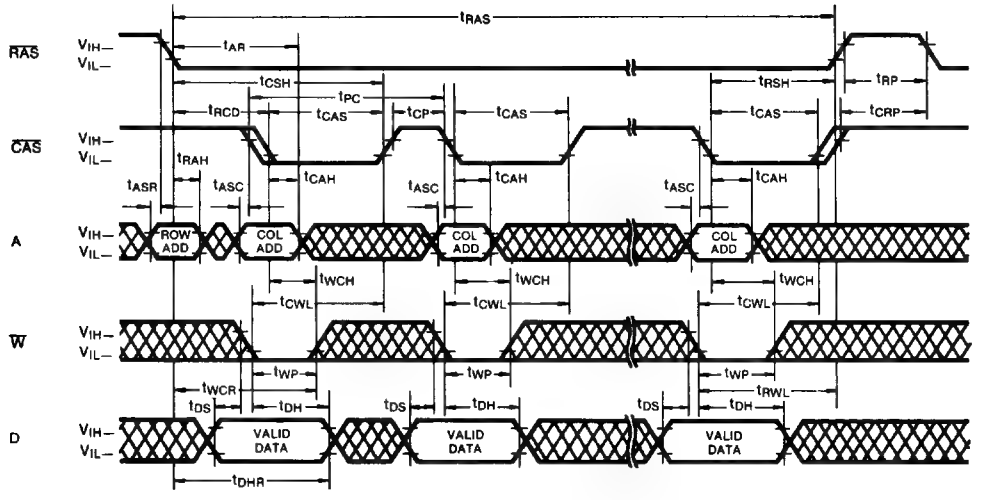
DON'T CARE

TIMING DIAGRAMS (Continued)

PAGE MODE READ CYCLE



PAGE MODE WRITE CYCLE

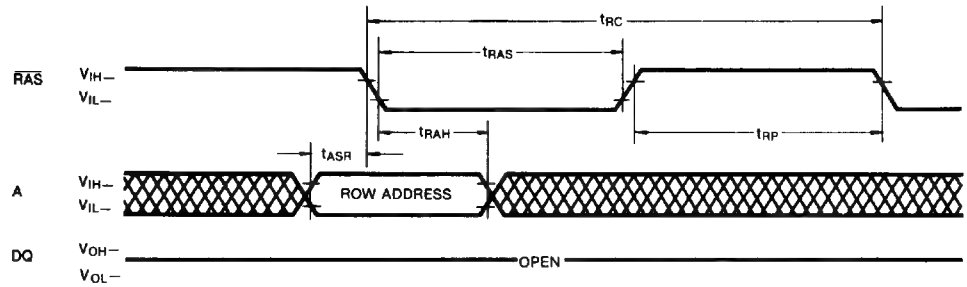


DON'T CARE

TIMING DIAGRAMS (Continued)

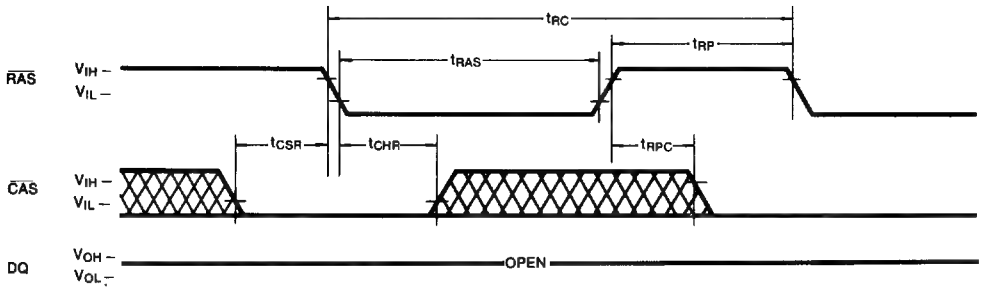
$\overline{RAS}$-ONLY REFRESH CYCLE

NOTE: $\overline{W}$ = DON'T CARE, $A_8 = V_{IL}$ or V_{IH}, $\overline{CAS} = V_{IH}$

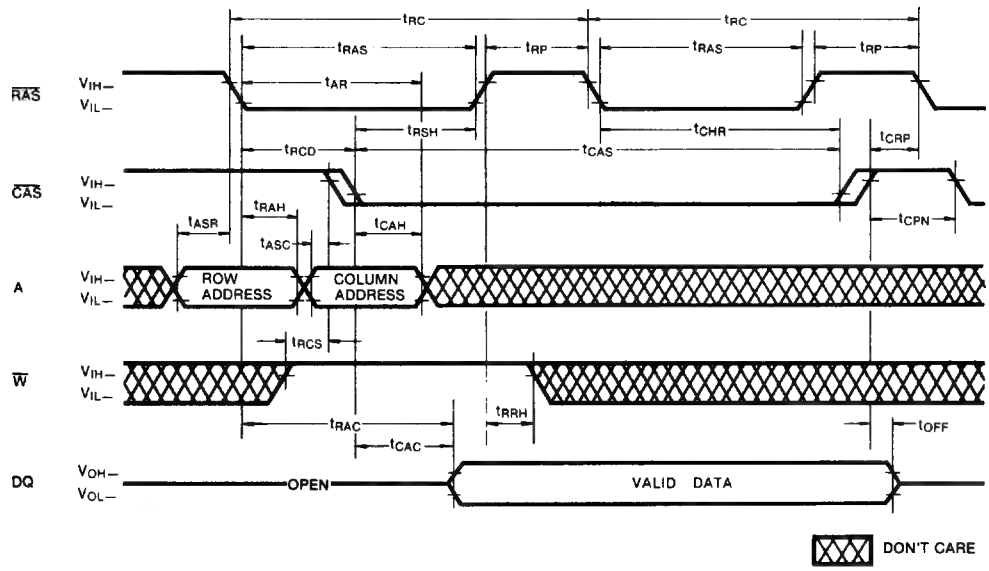


$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

NOTE: ADDRESS, $\overline{W}$ = DON'T CARE



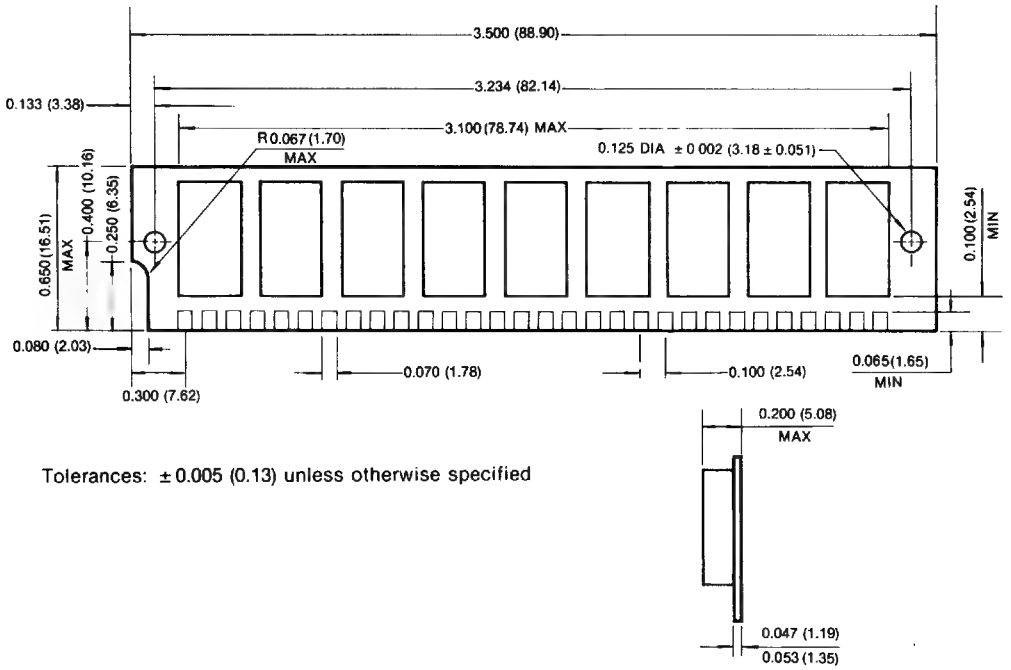
HIDDEN REFRESH CYCLE



PACKAGE DIMENSIONS

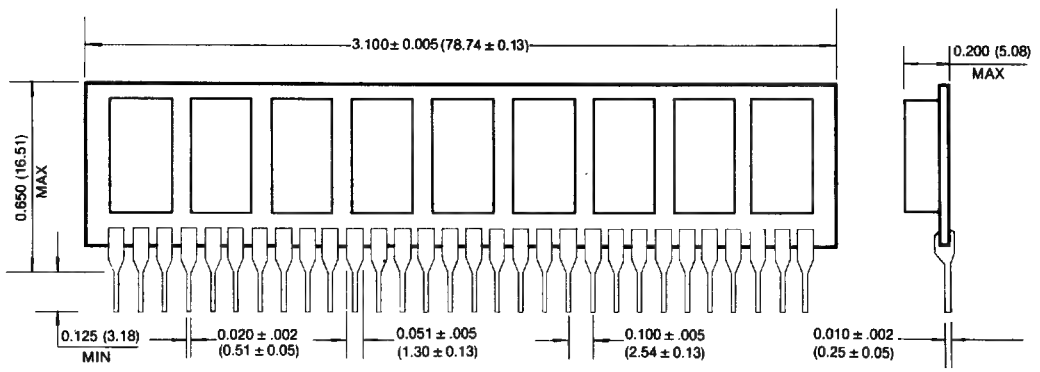
KMM59256 (256K x 9 SIMM)

Units: Inches (millimeters)



Tolerances: ±0.005 (0.13) unless otherwise specified

KMM49256 (256K x 9 SIP)



1M×8 Bit DRAM SIP and SIMM Memory Modules

FEATURES

- **1,048,576 x 8-bit Organization**
- **Performance range:**

	t_{RAC}	t_{CAC}	t_{RC}
KMM481000A-8	80ns	20ns	150ns
KMM581000A-8	80ns	20ns	150ns
KMM481000A-10	100ns	25ns	180ns
KMM581000A-10	100ns	25ns	180ns

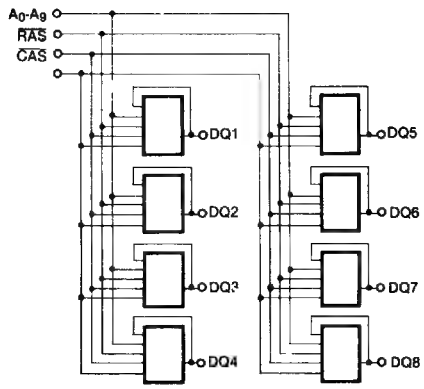
- **Fast Page Mode capability**
- **$\overline{CAS}$-before-$\overline{RAS}$ Refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **TTL compatible inputs and outputs**
- **Single +5V±10% power supply**
- **512 cycles/8ms refresh**
- **JEDEC standard pinout**

GENERAL DESCRIPTION

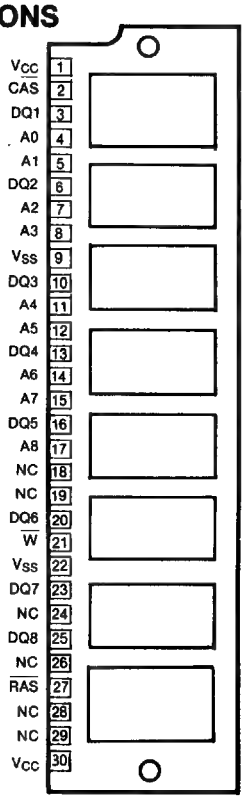
The Samsung KMM481000A and KMM581000A are 1M×8 dynamic RAM high density memory modules. Samsung 1M×8 memory modules consist of eight KM41C1000AJ DRAMs in 20-pin SOJ packages mounted on a 30 pin glass-epoxy substrate. A 0.22μF decoupling capacitor is mounted under each DRAM.

The 1M×8 DRAM modules are available in two package styles. The KMM481000A is SIP with leads suitable for through hole mounting or for mounting in a socket. The KMM581000A is SIMM with edge connections and is intended for mounting into 30 pin edge connector socket.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



PIN NAMES

Pin Name	Pin Function
A_0-A_9	Address Inputs
DQ	Data In/Out
$\overline{W}$	Read/Write Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

PART NUMBERS

KMM481000A-8	80ns	SIP	Page Mode
KMM481000A-10	100ns	SIP	Page Mode
KMM581000A-8	80ns	SIMM	Page Mode
KMM581000A-10	100ns	SIMM	Page Mode

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−1 to +7.0	V
Storage Temperature	T_{stg}	−55 to +150	°C
Power Dissipation	P_D	4.8	mW
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(Voltage referenced to V_{SS}, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	6.5	V
Input Low Voltage	V_{IL}	−1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Unit
Operating Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC} = min)	KMM481000A-8, KMM581000A-8 KMM481000A-10, KMM581000A-10	I_{CC1}	— —	560 480	mA mA
Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		I_{CC2}	—	16	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS}$ = V_{IH}, $\overline{RAS}$ Cycling @t_{RC} = min)	KMM481000A-8, KMM581000A-8 KMM481000A-10, KMM581000A-10	I_{CC3}	— —	560 480	mA mA
Fast Page Mode Current* ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ Cycling @t_{PC} = min)	KMM481000A-8, KMM581000A-8 KMM481000A-10, KMM581000A-10	I_{CC4}	— —	400 320	mA mA
Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} − 0.2V)		I_{CC5}	—	8	mA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC} = min)	KMM481000A-8, KMM581000A-8 KMM481000A-10, KMM581000A-10	I_{CC8}	— —	560 480	mA mA
Input Leakage Current (Any input 0≤V_{IN}≤6.5V, all other pins not under test = 0 volts)		I_{IL}	−80	80	μA
Output Leakage Current (Data out is disabled, 0≤V_{OUT}≤5.5V		I_{OL}	−10	10	μA
Output High Voltage Level (I_{OH} = −5mA)		V_{OH}	2.4	—	V
Output Low Voltage Level (I_{OL} = 4.2mA)		V_{OL}	—	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC8} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current.

CAPACITANCE ($T_A = 25°C$)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A_0-A_9)	C_{IN1}	—	50	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{W}$)	C_{IN2}	—	60	pF
Output Capacitance (DQ_1-DQ_8)	C_{DQ}	—	15	pF

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC} = 5.0V \pm 10\%$. See notes 1, 2)

Parameter	Symbol	KMM4(5)81000A-8		KMM4(5)81000A-10		Units	Notes
		Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RC}	150		180		ns	
Access Time from $\overline{RAS}$	t_{RAC}		80		100	ns	3,4,11
Access Time from $\overline{CAS}$	t_{CAC}		20		25	ns	3,4,5
Access Time from Column Address	t_{AA}		40		50	ns	3,11
Access Time from $\overline{CAS}$ Precharge	t_{CPA}		45		55	ns	3
$\overline{CAS}$ to Output in Low-Z	t_{CLZ}	5		5		ns	3
Output Buffer Turn-off Delay Time	t_{OFF}	0	25	0	30	ns	7
Transition Time (rise and fall)	t_T	3	50	3	50	ns	2
$\overline{RAS}$ Precharge Time	t_{RP}	60		70		ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	80	10,000	100	10,000	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	20		25		ns	
$\overline{CAS}$ Hold Time	t_{CSH}	80		100		ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	20	10,000	25	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	25	60	25	75	ns	4
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	20	40	20	50	ns	11
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	5		5		ns	
Row Address Set-up Time	t_{ASR}	0		0		ns	
Row Address Hold Time	t_{RAH}	15		15		ns	
Column Address Set-up Time	t_{ASC}	0		0		ns	
Column Address Hold Time	t_{CAH}	20		20		ns	
Column Address Hold Time Reference to $\overline{RAS}$	t_{AR}	65		75		ns	6
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	40		50		ns	
Read Command Set-up Time	t_{RCS}	0		0		ns	
Read Command Hold Time Referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	9
Read Command Hold Time Reference to $\overline{RAS}$	t_{RRH}	0		0		ns	9
Write Command Hold Time	t_{WCH}	15		20		ns	

AC CHARACTERISTICS (Continued)

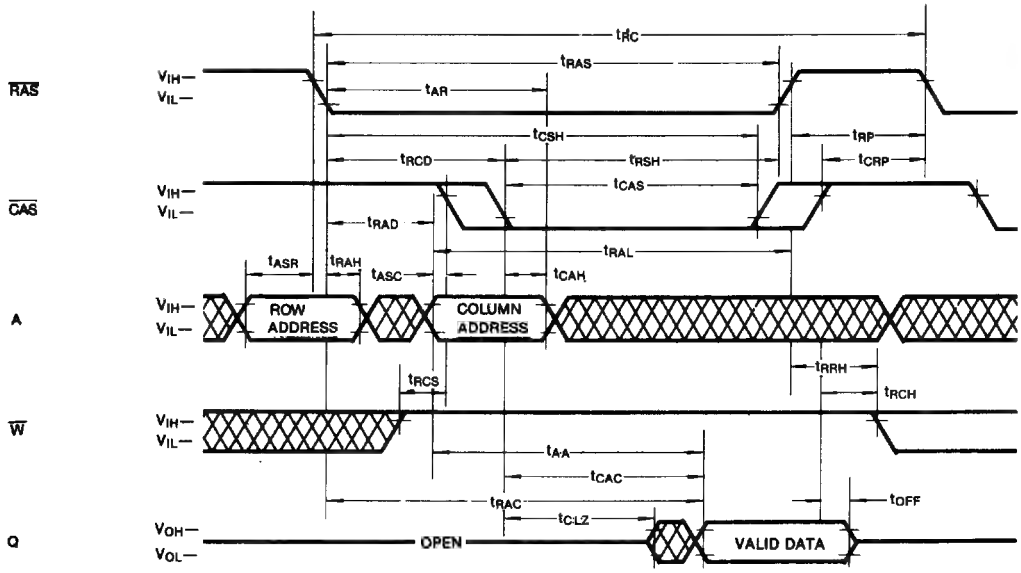
Parameter	Symbol	KMM4(5)81000A-8		KMM4(5)81000A-10		Units	Notes
		Min	Max	Min	Max		
Write Command Hold Time Referenced to $\overline{RAS}$	t_{WCR}	60		75		ns	6
Write Command Pulse Width	t_{WP}	15		20		ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	20		25		ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	20		25		ns	
Data-in Set-up Time	t_{DS}	0		0		ns	10
Data-in Hold Time	t_{DH}	20		20		ns	10
Data-in Hold Time Referenced to $\overline{RAS}$	t_{DHR}	65		75		ns	6
Refresh Period (512 cycles)	t_{REF}		8		8	ms	
Write Command Set-up Time	t_{WCS}	0		0		ns	8
$\overline{CAS}$ Set-up Time ($\overline{CAS}$ before $\overline{RAS}$ refresh)	t_{CSR}	10		10		ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ refresh)	t_{CHR}	25		30		ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	10		10		ns	
Fast Page Mode Cycle Time	t_{PC}	50		60		ns	
$\overline{CAS}$ Precharge Time (fast page mode)	t_{CP}	10		10		ns	
$\overline{RAS}$ Pulse Width (fast page mode)	t_{RASP}	80	100,000	100	100,000	ns	

NOTES

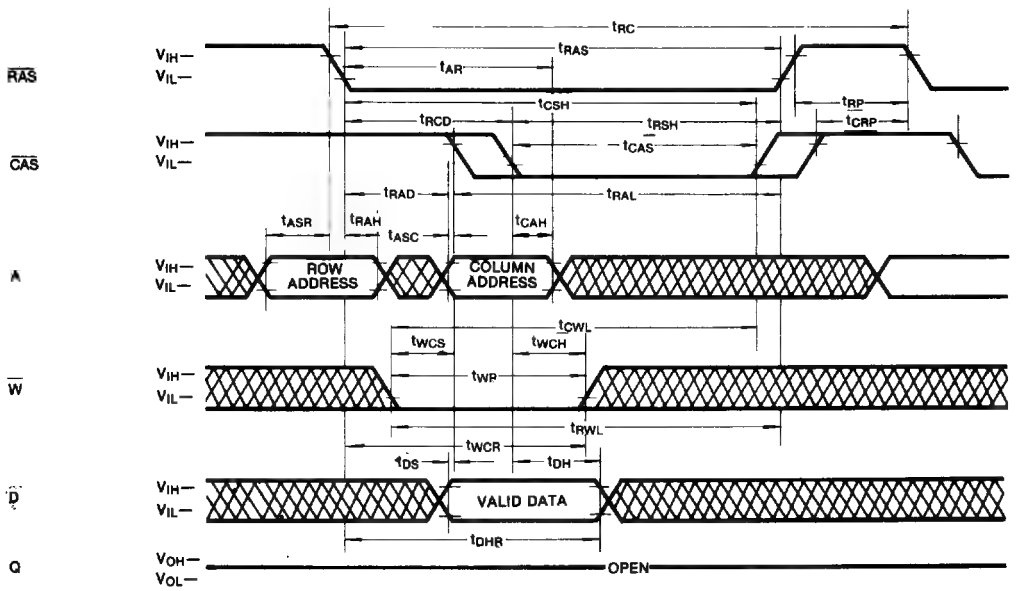
1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$(max).
6. t_{AR}, t_{WCR}, t_{DHR} referenced to t_{RAD}(max).
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS} is non restrictive operating parameters. It is included in the data sheet as electrical characteristics only. If $t_{WCS} > t_{WCS}$(min) the cycle is an early write cycle and the data output will remain open circuit throughout the entire cycle.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the t_{RAD}(max) limit insures that t_{RCD}(max) can be met. t_{RAD}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.

TIMING DIAGRAMS

READ CYCLE

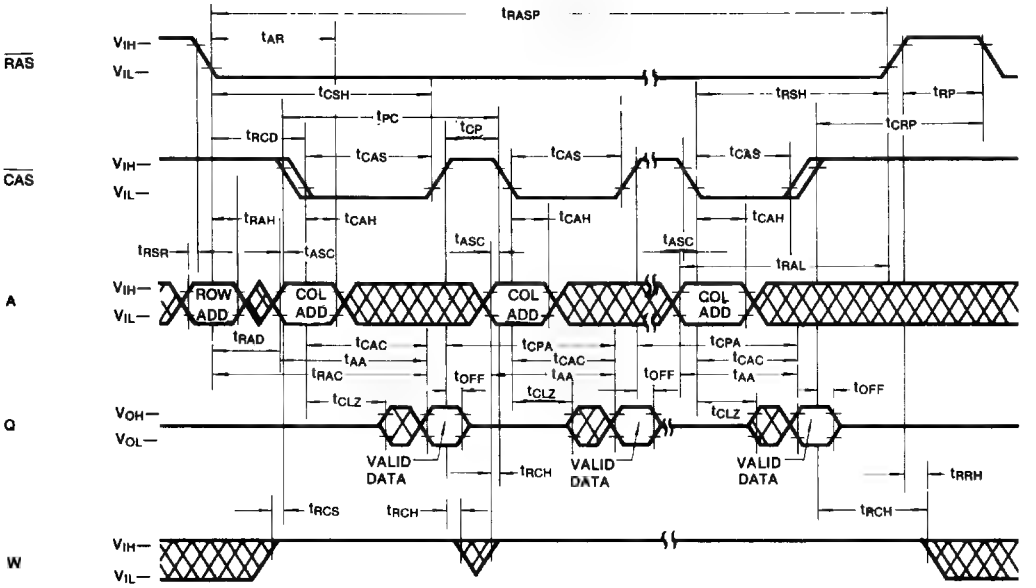


WRITE CYCLE (EARLY WRITE)

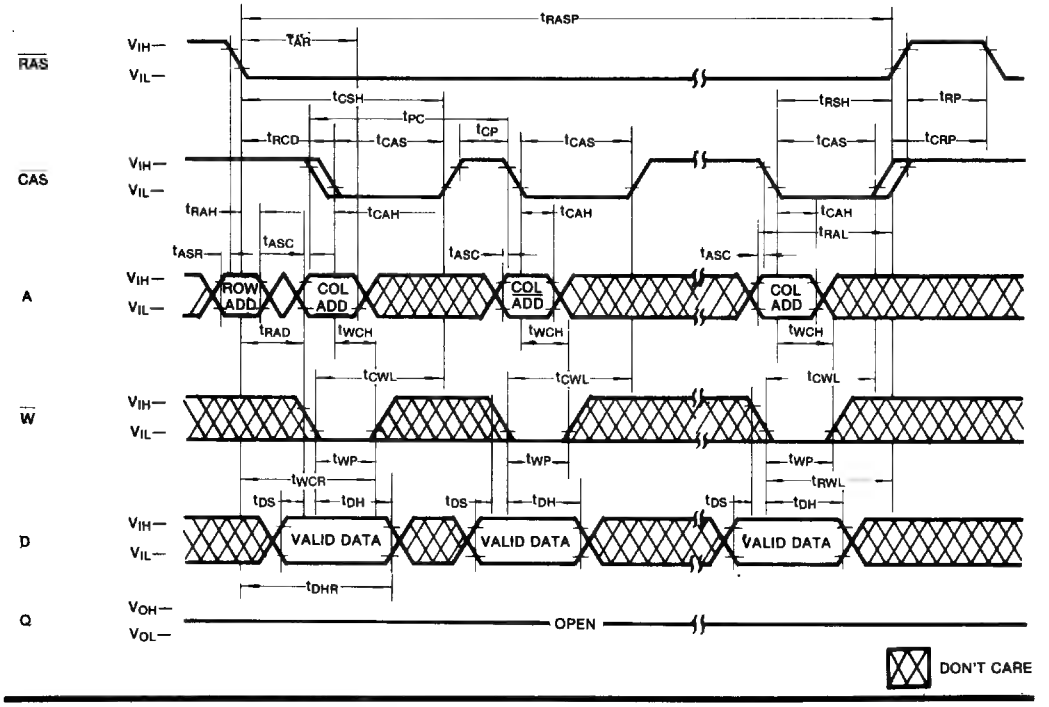


TIMING DIAGRAMS (Continued)

FAST PAGE MODE READ CYCLE



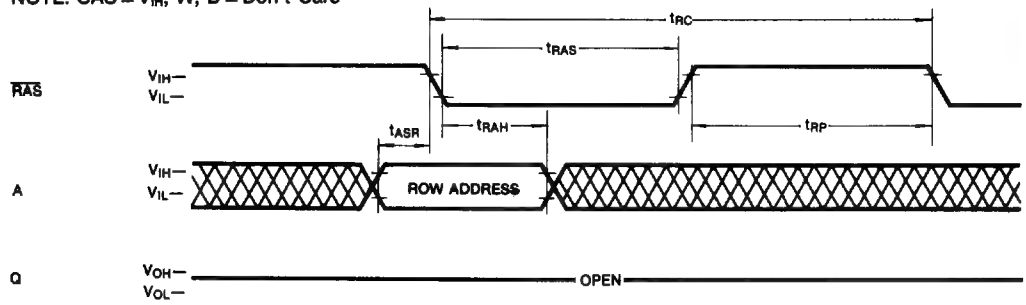
FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



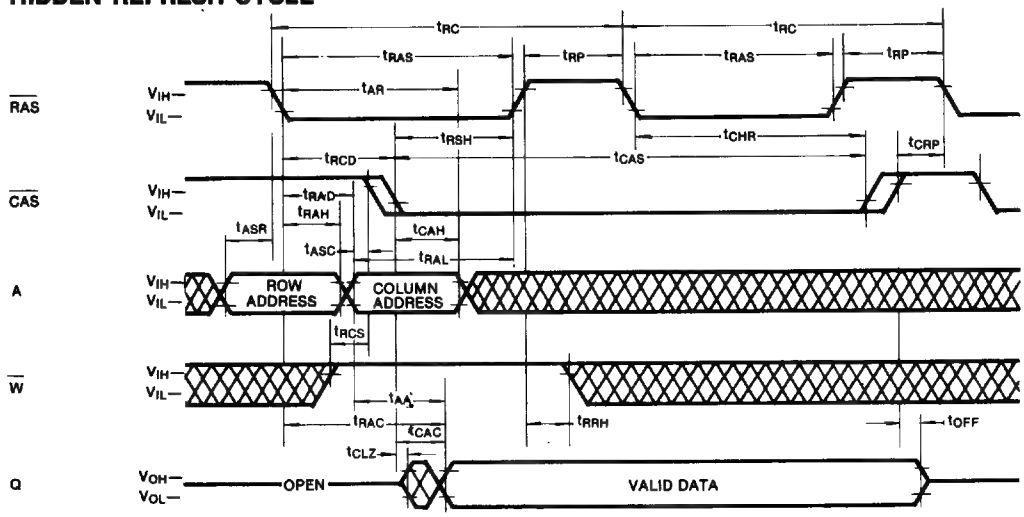
TIMING DIAGRAMS (Continued)

RAS-ONLY REFRESH CYCLE

NOTE: CAS = V_{IH}, W, D = Don't Care

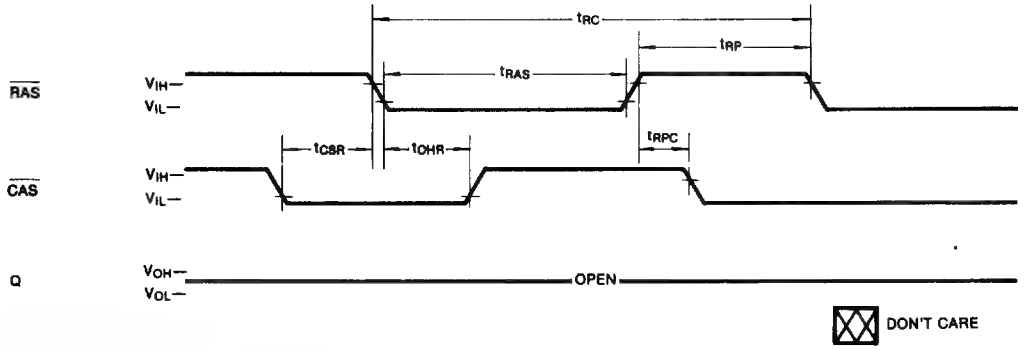


HIDDEN REFRESH CYCLE



CAS-BEFORE-RAS REFRESH CYCLE

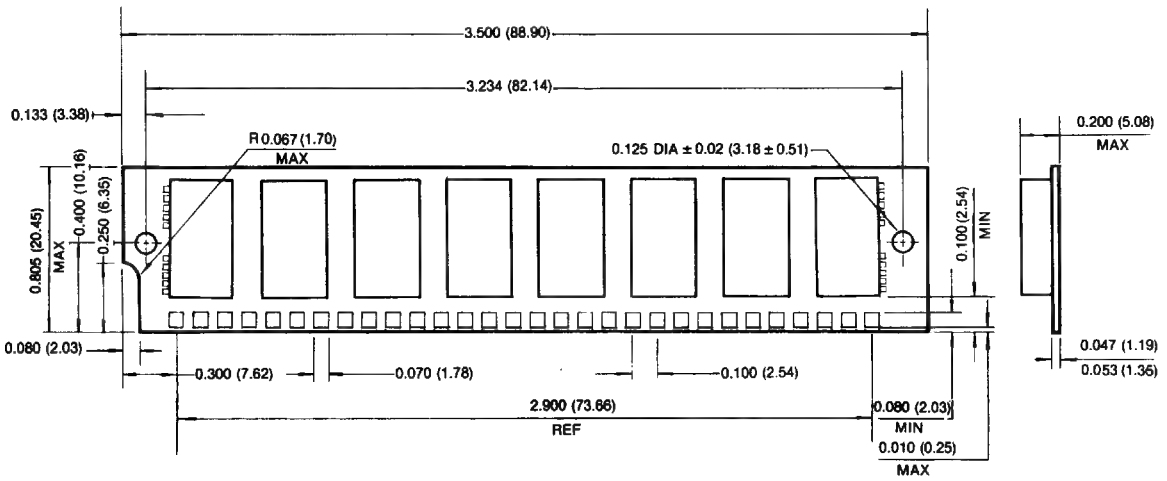
NOTE: Address, W, D = Don't Care



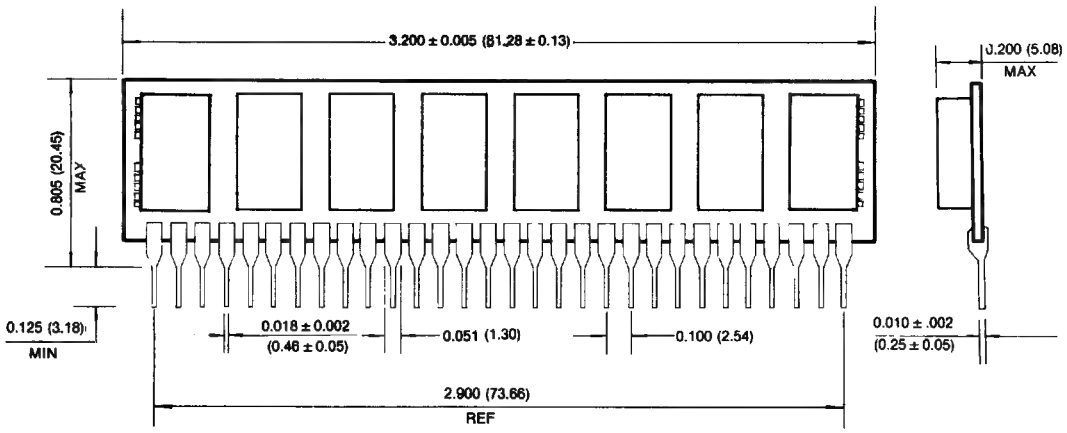
PACKAGE DIMENSIONS

KMM581000A (1M x 8 SIMM)

Units: Inches (millimeters)



KMM481000A (1M x 8 SIP)



TOLERANCES: ±0.005 (0.13) UNLESS OTHERWISE SPECIFIED

1M × 9 DRAM SIP and SIMM Memory Modules

FEATURES

- **1,048,576 x 9-bit Organization**
- **Ninth device has separate D, Q and $\overline{CAS}$ for Parity applications.**
- **Performance range:**

	t_{RAC}	t_{CAC}	t_{RC}
KMM491000A-8	80ns	20ns	150ns
KMM591000A-8	80ns	20ns	150ns
KMM491000A-10	100ns	25ns	180ns
KMM591000A-10	100ns	25ns	180ns

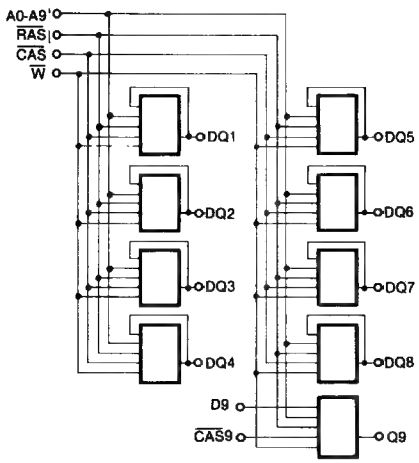
- **Fast Page Mode capability**
- **$\overline{CAS}$-before-$\overline{RAS}$ Refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **TTL compatible inputs and outputs**
- **Single +5V ± 10% power supply**
- **512 cycles/8ms refresh**
- **JEDEC standard pinout**

GENERAL DESCRIPTION

The Samsung KMM491000A and KMM591000A are 1M × 9 dynamic RAM high density memory modules. Samsung 1M × 9 memory modules consist of nine KM41C1000AJ DRAMs in 20-pin SOJ packages mounted on a 30 pin glass-epoxy substrate. A 0.22μF decouping capacitor is mounted under each DRAM.

The 1M × 9 DRAM modules are available in two package styles. The KMM491000A is SIP with leads suitable for through hole mounting or for mounting in a socket. The KMM591000A is SIMM with edge connections and is intended for mounting into 30 pin edge connector socket.

FUNCTIONAL BLOCK DIAGRAM



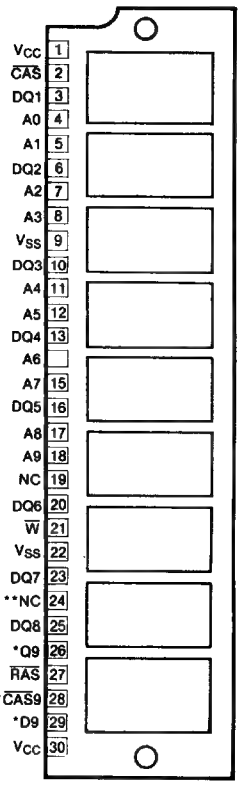
PART NUMBERS

KMM491000A-8	80ns	SIP	Page Mode
KMM491000A-10	100ns	SIP	Page Mode
KMM591000A-8	80ns	SIMM	Page Mode
KMM591000A-10	100ns	SIMM	Page Mode

PIN NAMES

Pin Name	Pin Function
A_0-A_9	Address Inputs
DQ	Data In/Out
D_9	Data In
Q_9	Data Out
$\overline{W}$	Read/Write Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{CAS_9}$	Column Address Strobe
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

PIN CONFIGURATION



* FOR PARITY BIT
** TEST FUNCTION ON PIN 24 ALSO WILL BE AVAILABLE BY OPTION

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−1 to +7.0	V
Storage Temperature	T_{stg}	−55 to +150	°C
Power Dissipation	P_D	5.4	mW
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(Voltage referenced to V_{SS}, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	6.5	V
Input Low Voltage	V_{IL}	−1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Unit
Operating Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC} = min)	KMM491000A-8, KMM591000A-8 KMM491000A-10, KMM591000A-10	I_{CC1}	— —	630 540	mA mA
Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		I_{CC2}	—	18	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS}$ = V_{IH}, $\overline{RAS}$ Cycling @t_{RC} = min)	KMM491000A-8, KMM591000A-8 KMM491000A-10, KMM591000A-10	I_{CC3}	— —	630 540	mA mA
Fast Page Mode Current* ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ Cycling @t_{PC} = min)	KMM491000A-8, KMM591000A-8 KMM491000A-10, KMM591000A-10	I_{CC4}	— —	450 360	mA mA
Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} − 0.2V)		I_{CC5}	—	9	mA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC} = min)	KMM491000A-8, KMM591000A-8 KMM491000A-10, KMM591000A-10	I_{CC8}	— —	630 540	mA mA
Input Leakage Current (Any input 0≤V_{IN}≤6.5V, all other pins not under test = 0 volts)		I_{IL}	−90	90	μA
Output Leakage Current (Data out is disabled, 0≤V_{OUT}≤5.5V		I_{OL}	−10	10	μA
Output High Voltage Level (I_{OH} = −5mA)		V_{OH}	2.4	—	V
Output Low Voltage Level (I_{OL} = 4.2mA)		V_{OL}	—	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC8} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current.

CAPACITANCE ($T_A = 25°C$)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A_0-A_9, $\overline{W}$, $\overline{CAS}$, $\overline{RAS}$)	C_{IN1}	—	60	pF
Input Capacitance (D_9, $\overline{CAS_9}$)	C_{IN2}	—	7	pF
Input Capacitance (DQ_1-DQ_8)	C_{DQ}	—	15	pF
Output Capacitance (Q_9)	C_{Q9}	—	10	pF

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC} = 5.0V \pm 10\%$. See notes 1, 2)

Parameter	Symbol	KMM4(5)91000A-8		KMM4(5)91000A-10		Units	Notes
		Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RC}	150		180		ns	
Access Time from $\overline{RAS}$	t_{RAC}		80		100	ns	3,4,11
Access Time from $\overline{CAS}$	t_{CAC}		20		25	ns	3,4,5
Access Time from Column Address	t_{AA}		40		50	ns	3,11
Access Time from $\overline{CAS}$ Precharge	t_{CPA}		45		55	ns	3
$\overline{CAS}$ to Output in Low-Z	t_{CLZ}	5		5		ns	3
Output Buffer Turn-off Delay Time	t_{OFF}	0	25	0	30	ns	7
Transition Time (rise and fall)	t_T	3	50	3	50	ns	2
$\overline{RAS}$ Precharge Time	t_{RP}	60		70		ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	80	10,000	100	10,000	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	20		25		ns	
$\overline{CAS}$ Hold Time	t_{CSH}	80		100		ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	20	10,000	25	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	25	60	25	75	ns	4
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	20	40	20	50	ns	11
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	5		5		ns	
Row Address Set-up Time	t_{ASR}	0		0		ns	
Row Address Hold Time	t_{RAH}	15		15		ns	
Column Address Set-up Time	t_{ASC}	0		0		ns	
Column Address Hold Time	t_{CAH}	20		20		ns	
Column Address Hold Time Reference to $\overline{RAS}$	t_{AR}	65		75		ns	6
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	40		50		ns	
Read Command Set-up Time	t_{RCS}	0		0		ns	
Read Command Hold Time Referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	9
Read Command Hold Time Reference to $\overline{RAS}$	t_{RRH}	0		0		ns	9
Write Command Hold Time	t_{WCH}	15		20		ns	

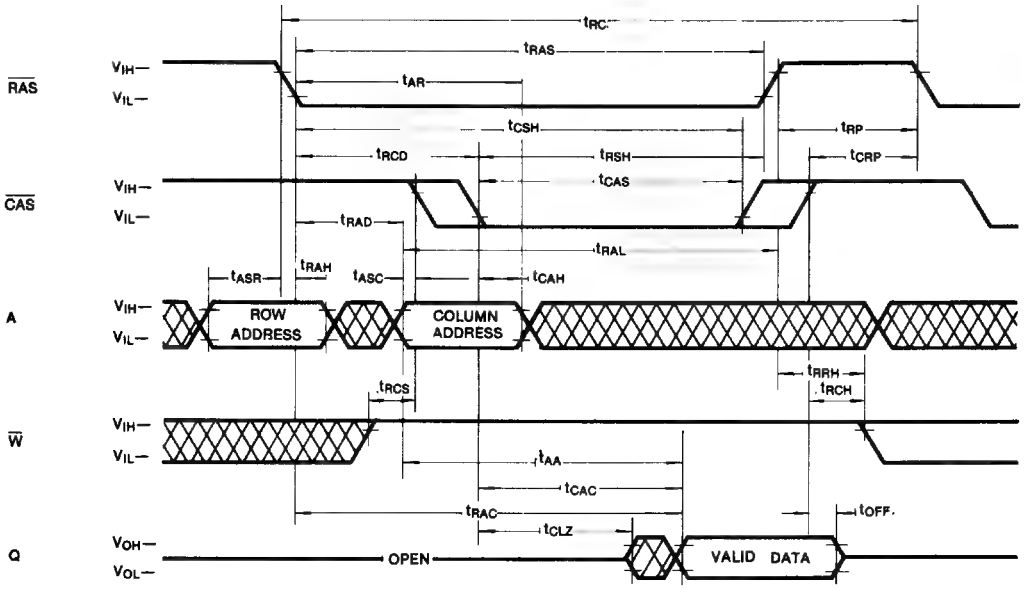
AC CHARACTERISTICS (Continued)

Parameter	Symbol	KMM4(5)91000A-8		KMM4(5)91000A-10		Units	Notes
		Min	Max	Min	Max		
Write Command Hold Time Referenced to $\overline{RAS}$	t_{WCR}	60		75		ns	6
Write Command Pulse Width	t_{WP}	15		20		ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	20		25		ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	20		25		ns	
Data-in Set-up Time	t_{DS}	0		0		ns	10
Data-in Hold Time	t_{DH}	20		20		ns	10
Data-in Hold Time Referenced to $\overline{RAS}$	t_{DHR}	65		75		ns	6
Refresh Period (512 cycles)	t_{REF}		8		8	ms	
Write Command Set-up Time	t_{WCS}	0		0		ns	8
$\overline{CAS}$ Set-up Time ($\overline{CAS}$ before $\overline{RAS}$ refresh)	t_{CSR}	10		10		ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ refresh)	t_{CHR}	25		30		ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	10		10		ns	
Fast Page Mode Cycle Time	t_{PC}	50		60		ns	
$\overline{CAS}$ Precharge Time (fast page mode)	t_{CP}	10		15		ns	
$\overline{RAS}$ Pulse Width (fast page mode)	t_{RASP}	80	100,000	100	100,000	ns	

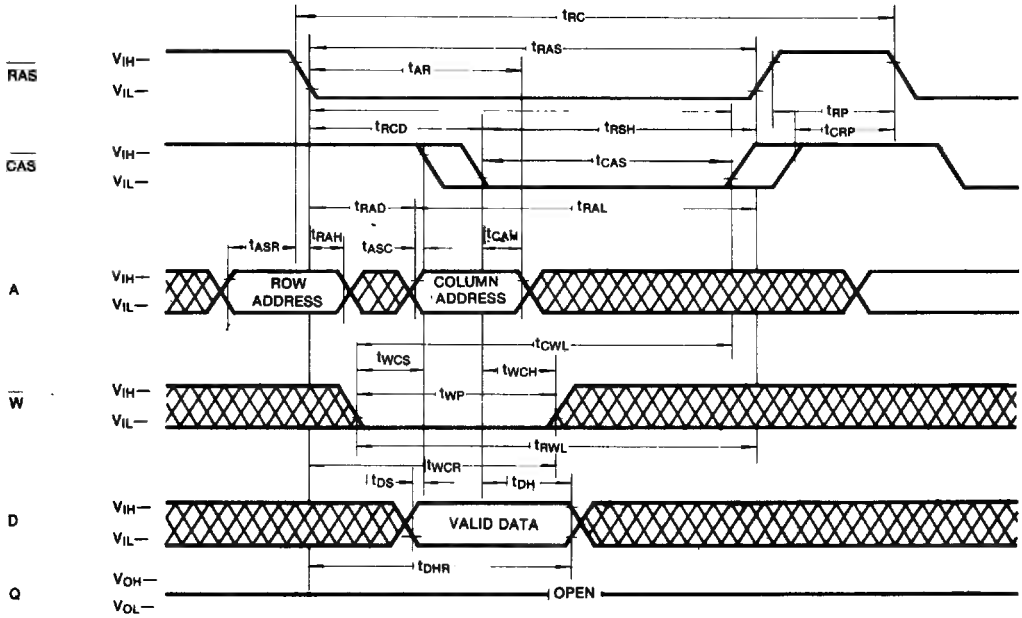
NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$(max).
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to t_{RAD}(max).
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS} is non restrictive operating parameters. It is included in the data sheet as electrical characteristics only. If $t_{WCS} > t_{WCS}$(min) the cycle is an early write cycle and the data output will remain open circuit throughout the entire cycle.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the t_{RAD}(max) limit insures that t_{RCD}(max) can be met. t_{RAD}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
12. Normal operation requires the "T.F." pin to be connected to V_{SS} or TTL logic low level or left unconnected on the printed wiring board.
13. When the "T.F." pin is connected to a defined positive voltage, the internal test function may be activated. Contact Samsung Semiconductor for specific operational details of the "test function."

READ CYCLE

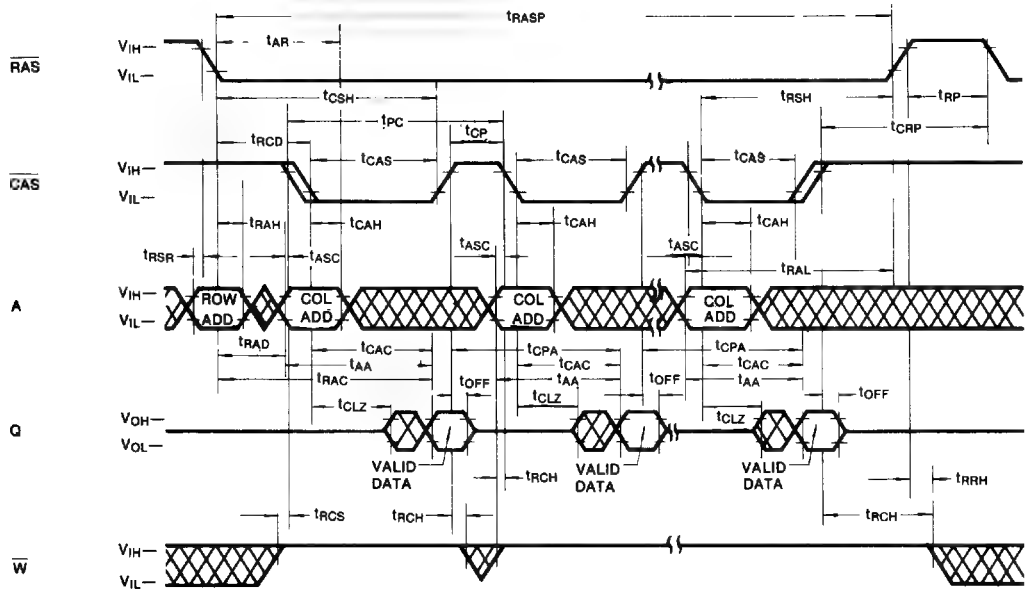


WRITE CYCLE (EARLY WRITE)

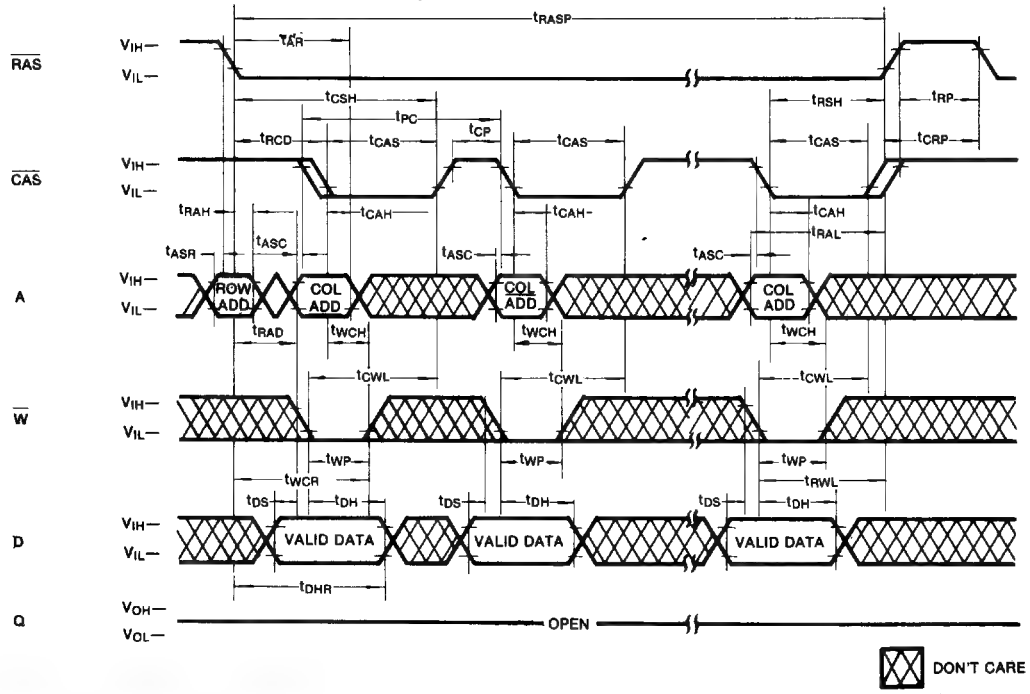


TIMING DIAGRAMS (Continued)

FAST PAGE MODE READ CYCLE



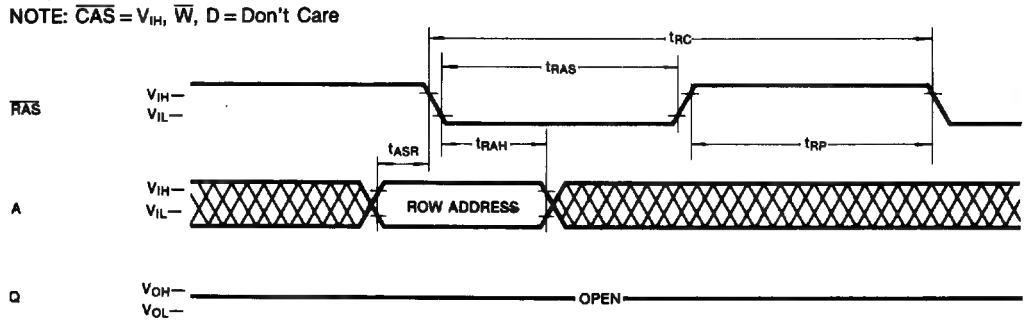
FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



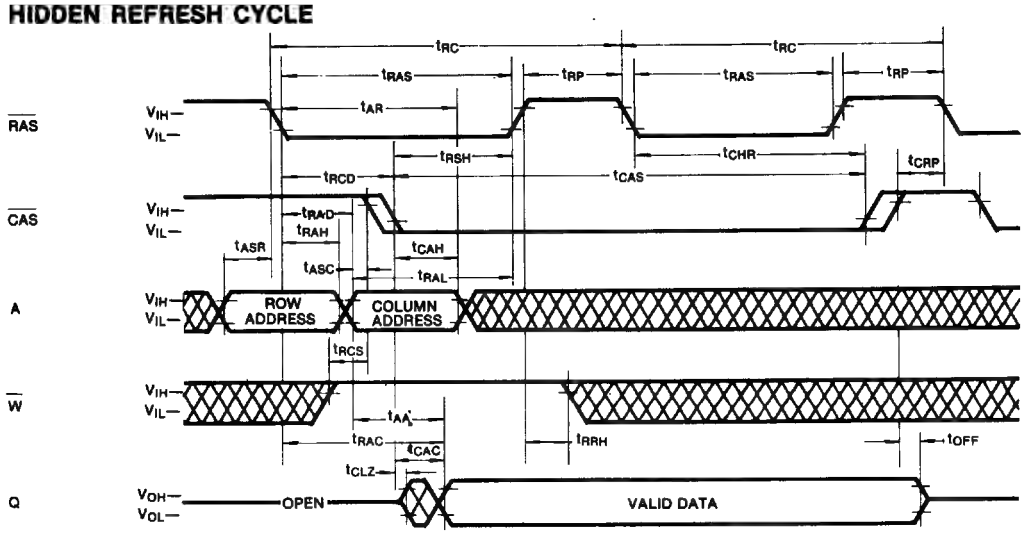
TIMING DIAGRAMS (Continued)

RAS-ONLY REFRESH CYCLE

NOTE: $\overline{CAS} = V_{IH}$, $\overline{W}$, D = Don't Care

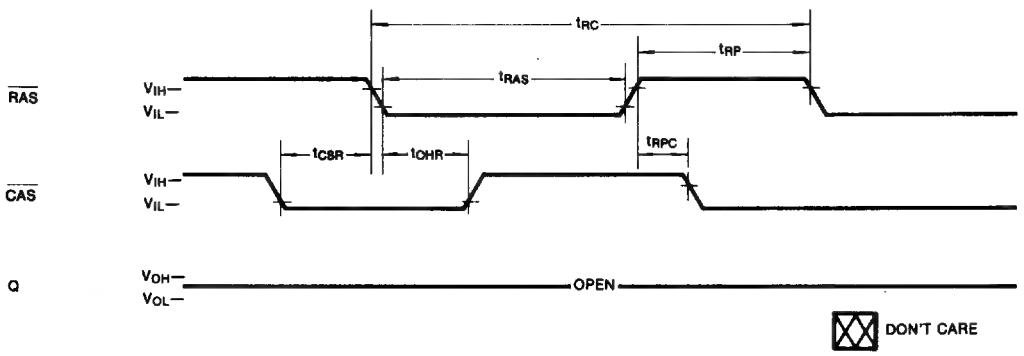


HIDDEN REFRESH CYCLE



CAS-BEFORE-RAS REFRESH CYCLE

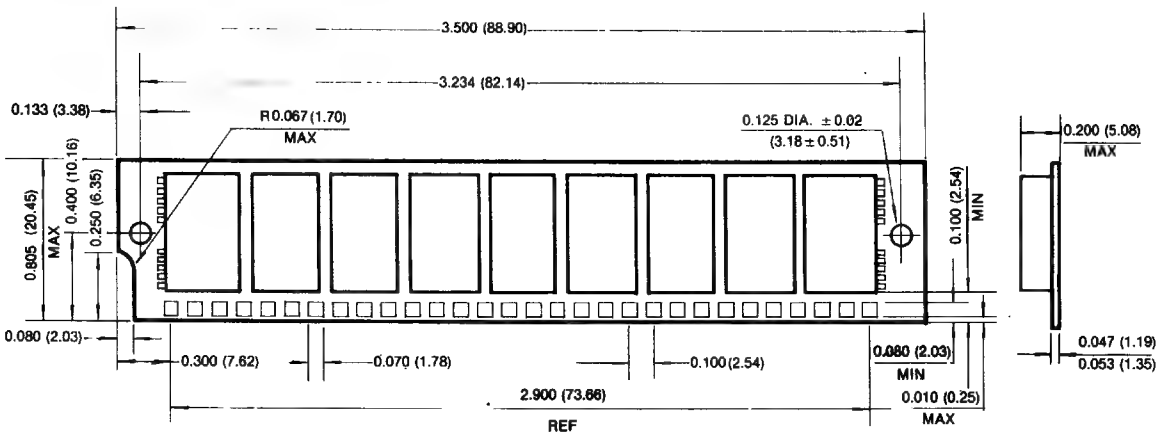
NOTE: Address, $\overline{W}$, $\overline{D}$ = Don't Care



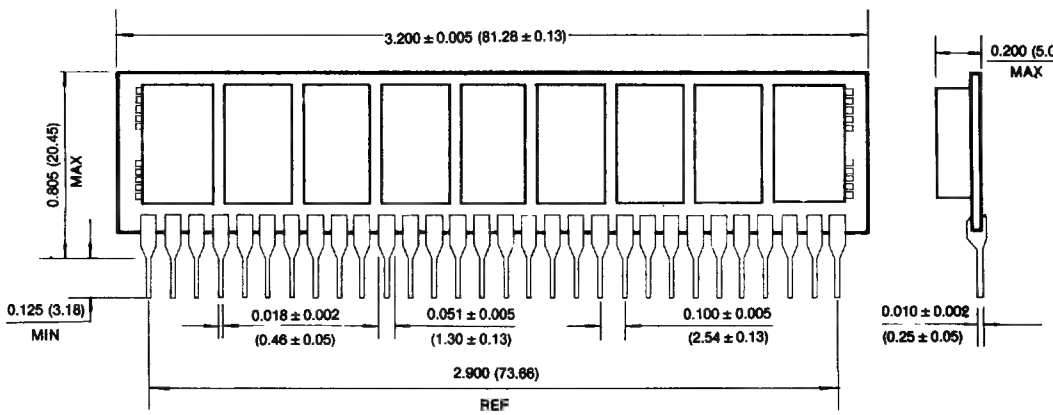
PACKAGE DIMENSIONS

KMM591000 (1M × 9 SIMM)

Units: Inches (millimeters)

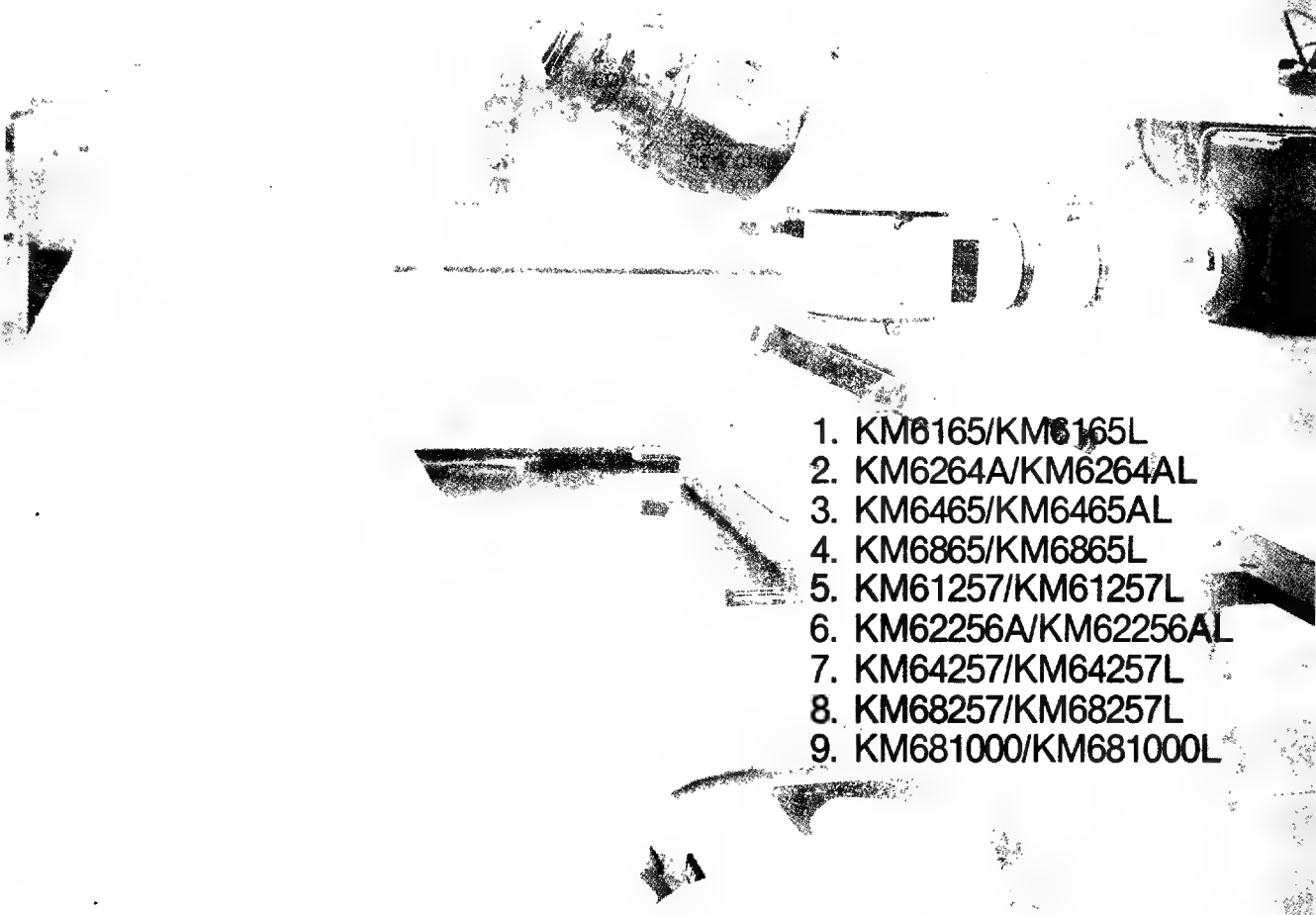


KMM491000A (1M × 9 SIP)



TOLERANCES: ±0.005 (0.13) UNLESS OTHERWISE SPECIFIED

SRAM DATA SHEETS 3



1. KM6165/KM6165L
2. KM6264A/KM6264AL
3. KM6465/KM6465AL
4. KM6865/KM6865L
5. KM61257/KM61257L
6. KM62256A/KM62256AL
7. KM64257/KM64257L
8. KM68257/KM68257L
9. KM681000/KM681000L

Static RAM

Capacity	Part Name	Organization	Speed (ns)	Technology	Current		Package	Remark
					Active, mA Typ (max)	Standby, μA Typ (max)		
64K	†KM6165	64K × 1	25/35/45	CMOS	(100)	(2mA)	SDIP/SOJ	TBA
	†KM6165L	64K × 1	25/35/45	CMOS	(100)	(100)	SDIP/SOJ	TBA
	†KM6465	16K × 4	25/35/45	CMOS	(100)	(2mA)	SDIP	TBA
	†KM6465L	16K × 4	25/35/45	CMOS	(100)	(100)	SDIP	TBA
	†KM6865	8K × 8	35/45/55	CMOS	(120)	(2mA)	SDIP	TBA
	†KM6865L	8K × 8	35/45/55	CMOS	(120)	(100)	SDIP	TBA
	KM6264A	8K × 8	70/100/120	CMOS	(70)	(2mA)	DIP/SOP	Now
	KM6264AL	8K × 8	70/100/120	CMOS	(70)	2(100)	DIP/SOP	Now
256K	*KM61257	256K × 1	25/35/45	CMOS	(100)	(2mA)	SDIP/SOJ	Now
	*KM61257L	256K × 1	25/35/45	CMOS	(100)	(100)	SDIP/SOJ	Now
	*KM64257	64K × 4	25/35/45	CMOS	(120)	(2mA)	SDIP/SOJ	Now
	*KM64257L	64K × 4	25/35/45	CMOS	(120)	(100)	SDIP/SOJ	Now
	†KM68257P	32K × 8	35/45/55	CMOS	(120)	(2mA)	DIP	TBA
	†KM68257LP	32K × 8	35/45/55	CMOS	(120)	(100)	DIP	TBA
	KM62256A	32K × 8	80/100/120	CMOS	(70)	(2mA)	DIP/SOP	Now
	KM62256AL	32K × 8	80/100/120	CMOS	(70)	2(100)	DIP/SOP	Now
1M	††KM681000	128K × 8	70/100/120	CMOS	(70)	(2mA)	DIP/SOP	TBA
	††KM681000L	128K × 8	70/100/120	CMOS	(70)	2(100)	DIP/SOP	TBA

*: New Product
†: Preliminary Product
††: Under Development
TBA: To Be Announced

8K x 8 Bit Static RAM

FEATURES

- **Fast Access Time 70, 100, 120ns (max.)**
- **Low Standby Current: 100μA (max.)**
- **Low Data Retention Current: 50μA (max.)**
- **Capability of Battery Back-up Operation**
- **Data Retention Voltage: 2.0V (min.)**
- **Single 5V ± 10% supply**
- **TTL compatible inputs and outputs**
- **Pin compatible with 64K EPROMS**
- **Fully Static Operation**
- **Standard 28-pin DIP (600 mil) and 28-pin SOP (330 mil)**
- **Common I/O, Tristate Output**

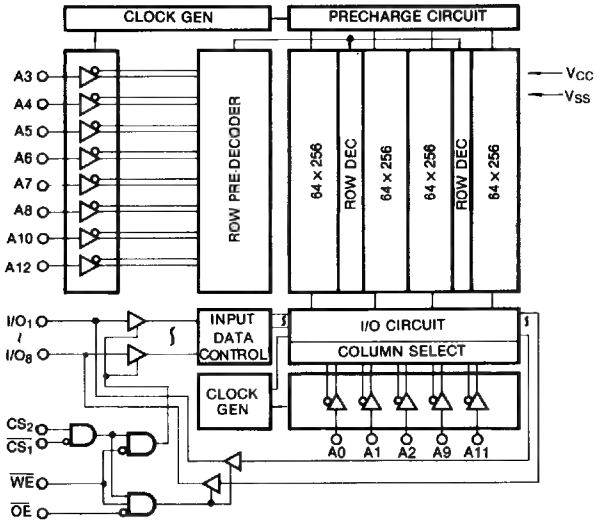
GENERAL DESCRIPTION

The KM6264A/AL is a 65,536-bit high speed Static Random Access Memory organized as 8,192 words by 8 bits. This device is fabricated using Samsung's advanced CMOS process.

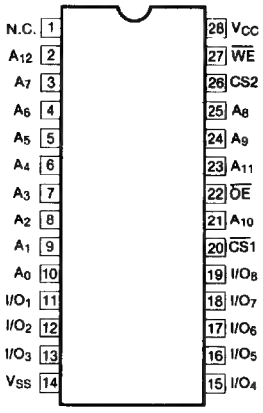
The KM6264A/AL has an output enable input for precise control of the data outputs. It also has chip enable inputs for the minimum current power down mode. The KM6264A/AL has been designed for high speed and low power applications. It is particularly well suited for battery backup non-volatile memory applications.

Two versions are available, the KM6264A and KM6264AL. The L-version is specified with lower standby and data retention currents than the standard version. Otherwise the two versions are identical.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Pin Name	Pin Function
A_0-A_{12}	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS_1}$, CS_2	Chip Select
$\overline{OE}$	Output Enable
I/O_1-I/O_8	Data Inputs/Outputs
V_{CC}	+5V Power Supply
V_{SS}	Ground
N.C.	No Connection

ABSOLUTE MAXIMUM RATINGS* (See Note)

Parameter	Symbol	Rating	Units
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	−0.3 to V_{CC}+0.5	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	−0.5 to +7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	T_{stg}	−55 to +125	°C
Operating Temperature	T_A	0 to +70	°C

*Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS (T_A=0°C to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	—	V_{CC}+0.3	V
Input Low Voltage	V_{IL}	−0.3*	—	0.8	V

*Note: V_{IL} (min) = −3.0V for ≤50ns pulse.

DC CHARACTERISTICS

(T_A=0°C to 70°C, V_{CC}=5V±10%, unless otherwise specified)

Parameter	Symbol	Test Conditions	Device	Min	Typ	Max	Units
Input Leakage Current	I_{LI}	$V_{IN}=V_{SS}$ to V_{CC}				2	μA
Output Leakage Current	I_{LO}	$\overline{CS1}=V_{IH}$ or CS2=V_{IL} or $\overline{OE}=V_{IH}$, $V_{SS}\leq V_{I/O}\leq V_{CC}$				2	μA
Operating Power Supply Current	I_{CC1}	$\overline{CS1}=V_{IL}$, CS2=V_{IH}, I_{OUT}=0mA				40	mA
Average Operating Current	I_{CC2}	Min Cycle, 100% Duty $\overline{CS1}=V_{IL}$, CS2=V_{IH}			35	70	mA
Standby Power Supply Current	I_{SB}	$\overline{CS1}=V_{IH}$ or CS2=V_{IL}				3	mA
	I_{SB1}	$\overline{CS1}\geq V_{CC}-0.2V$	KM6264A			1	mA
		$-0.3V\leq CS2\leq 0.2V$	KM6264AL		2	100	μA
Output High Voltage	V_{OH}	I_{OH}=−1.0mA		2.4			V
Output Low Voltage	V_{OL}	I_{OL}=2.1mA				0.4	V

CAPACITANCE (f=1MHz, T_A=25°C)*

Parameter	Symbol	Test Conditions	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	—	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	—	8	pF

*Note: Capacitance is sampled and not 100% tested.

AC CHARACTERISTICS

(Ta = 0°C to 70°C, V_{CC} = 5V ± 10%, unless otherwise specified.)

TEST CONDITIONS

Parameter	Value
Input Pulse Levels	0.8 to 2.4V
Input Rise and Fall Times	5 ns
Input and Output Timing Reference Level	1.5V
Output Load	1 TTL Load and C_L* = 100pF (including scope and jig capacitance)

*C_L = 30pF for KM6264A-7, KM6264AL-7

READ CYCLE

Parameter	Symbol	KM6264A-7 KM6264AL-7		KM6264A-10 KM6264AL-10		KM6264A-12 KM6264AL-12		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	70		100		120		ns
Address Access Time	t_{AA}		70		100		120	ns
Chip Select to Output	t_{CO1}, t_{CO2}		70		100		120	ns
Output Enable to Valid Output	t_{OE}		35		50		60	ns
Chip Enable to Low-Z Output	t_{LZ1}, t_{LZ2}	5		10		10		ns
Output Enable to Low-Z Output	t_{OLZ}	5		5		5		ns
Chip Disable to High-Z Output	t_{HZ1}, t_{HZ2}	0	30	0	35	0	40	ns
Output Disable to High-Z Output	t_{OHZ}	0	30	0	35	0	40	ns
Output Hold from Address Change	t_{OH}	10		10		15		ns

WRITE CYCLE

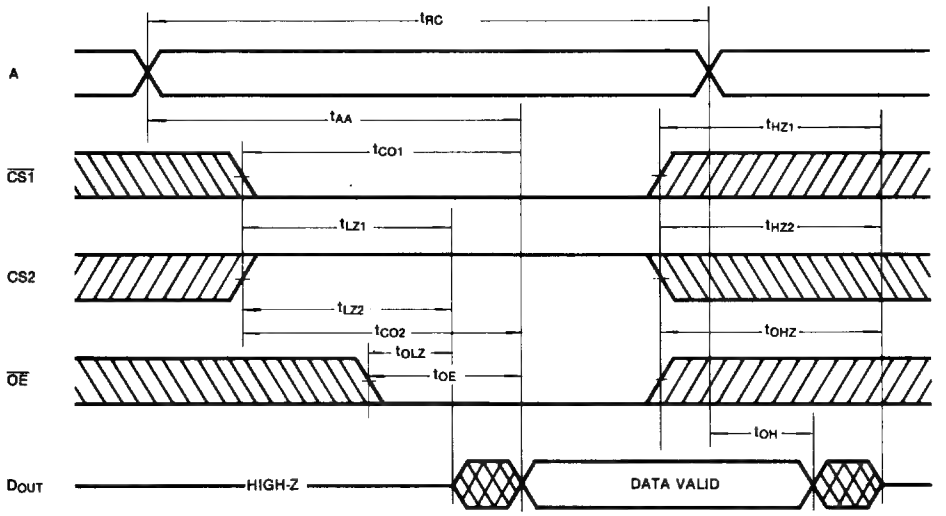
Parameter	Symbol	KM6264A-7 KM6264AL-7		KM6264A-10 KM6264AL-10		KM6264A-12 KM6264AL-12		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	70		100		120		ns
Chip Select to End of Write	t_{CW}	60		80		85		ns
Address Set-up Time	t_{AS}	0		0		0		ns
Address Valid to End of Write	t_{AW}	60		80		85		ns
Write Pulse Width	t_{WP}	40		60		70		ns
Write Recovery from $\overline{CS1}$ or $\overline{WE}$	t_{WR1}, t_{WR}	0		5		5		ns
Write Recovery from CS2	t_{WR2}	10		15		15		ns
Write to Output High-Z	t_{WHZ}	0	30	0	35	0	40	ns
Data to Write Time Overlap	t_{DW}	30		40		50		ns
Data Hold from Write Time	t_{DH}	0		0		0		ns
End of Write to Output Low-Z	t_{OW}	5		5		10		ns

NOTES:

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referenced to the V_{OH} or V_{OL} levels.
2. At any given temperature and voltage condition, t_{HZ} max is less than t_{LZ} min both for a given device and from device to device.
3. A write occurs during the overlap of a low $\overline{CS1}$, a high CS2 and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS1}$ going low, CS2 going high and $\overline{WE}$ going low: A write ends at the earliest transition among $\overline{CS1}$ going high, CS2 going low and $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.
4. t_{CW} is measured from the later of $\overline{CS1}$ going low or CS2 going high to the end of write.
5. t_{AS} is measured from the address valid to the beginning of write.
6. t_{WR} is measured from the end of write to the address change. t_{WR1} applied in case a write ends at $\overline{CS1}$, or $\overline{WE}$ going high, t_{WR2} applied in case a write ends at CS2 going low.
7. If $\overline{OE}$, CS2 and $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase to the outputs must not be applied because bus contention can occur.
8. If $\overline{CS1}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high impedance state.
9. D_{OUT} is the read data of the new address.
10. If $\overline{CS1}$ is low and CS2 is high during this period, I/O pins are in the output state. Therefore, the input signals of opposite phase to the output must not be applied to them.
11. During this period, I/O pins are in the output state, therefore the input signals of opposite phase to the outputs must not be applied.

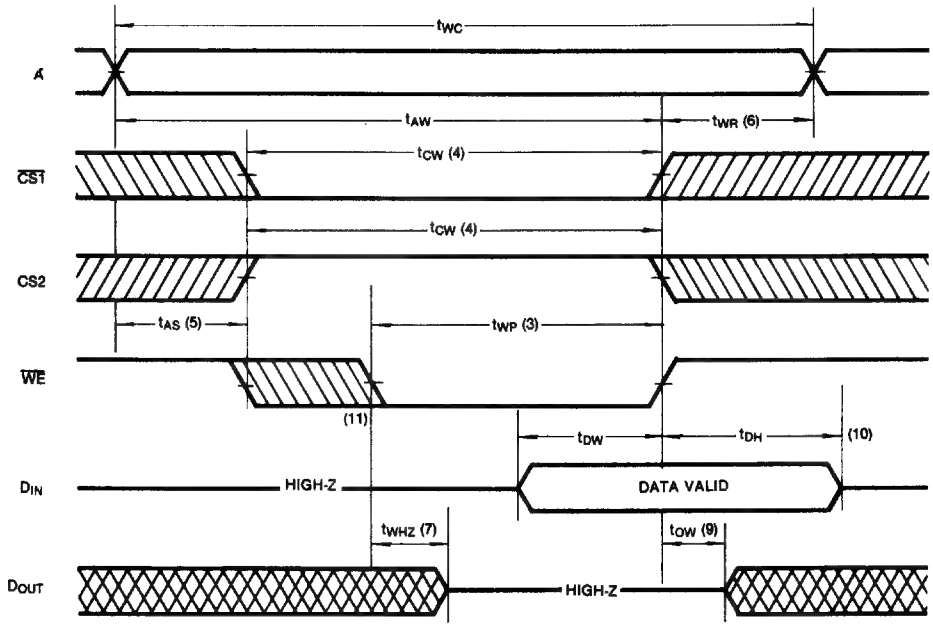
TIMING DIAGRAMS

READ CYCLE ($\overline{WE} = V_{IH}$)

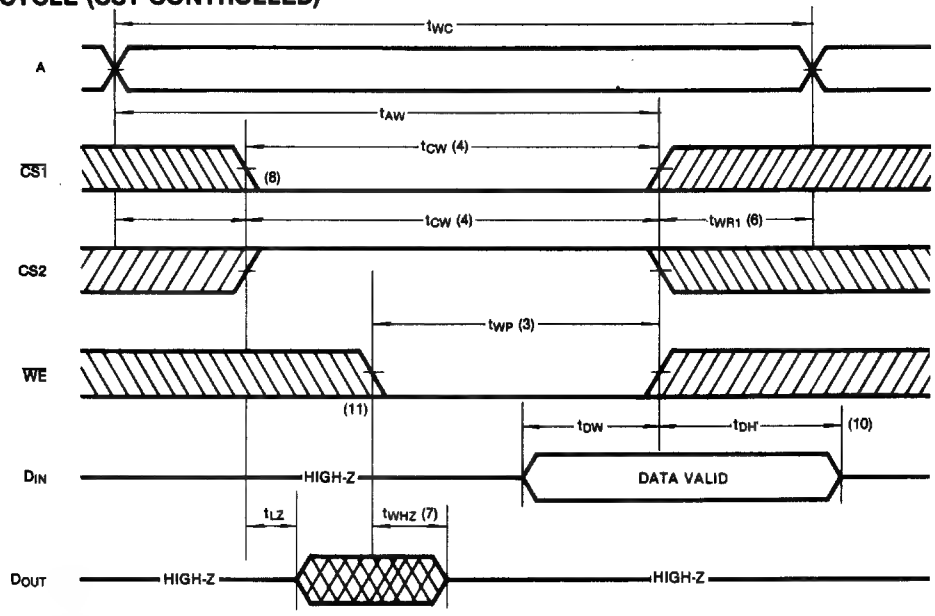


TIMING DIAGRAMS (Continued)

WRITE CYCLE ($\overline{WE}$ CONTROLLED)

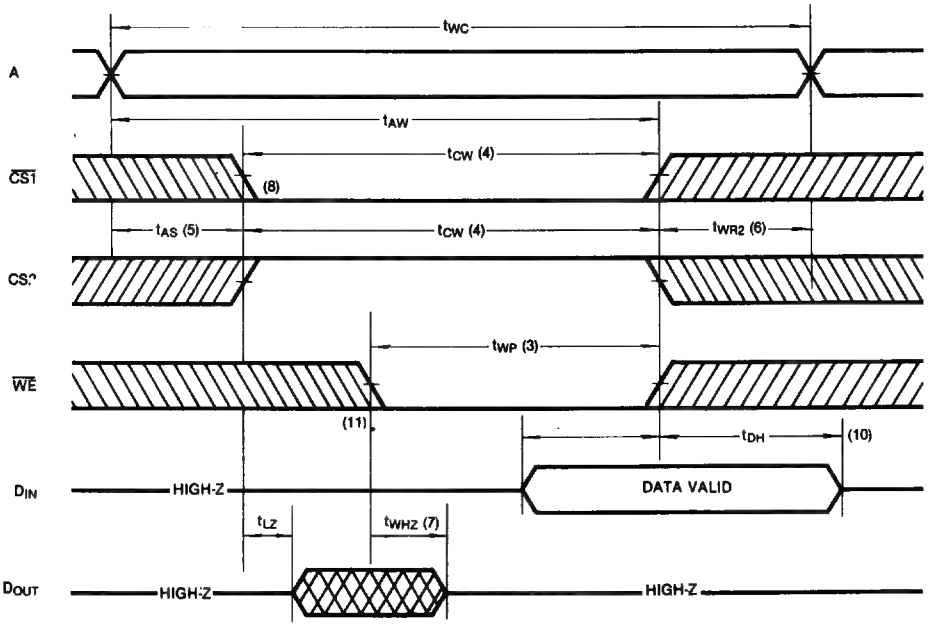


WRITE CYCLE ($\overline{CS1}$ CONTROLLED)



TIMING DIAGRAM (Continued)

WRITE CYCLE ($\overline{CS2}$ CONTROLLED)

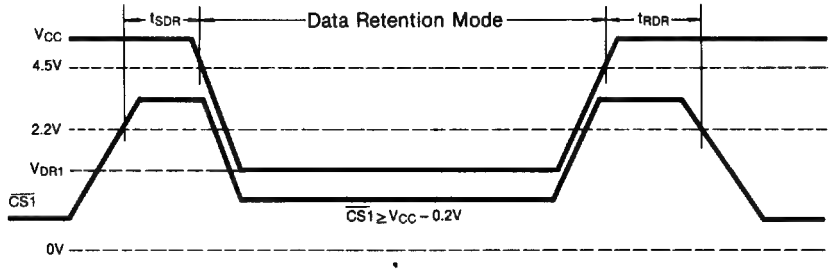


DATA RETENTION CHARACTERISTICS (T_A = 0°C to +70°C)

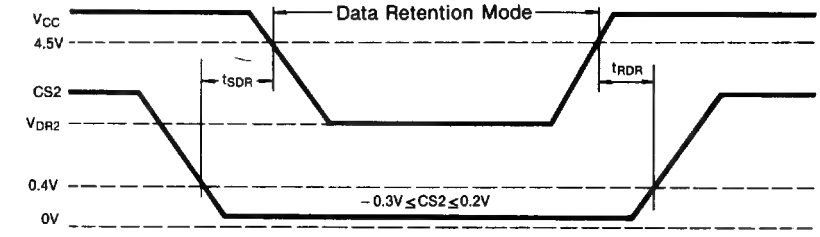
Parameter	Symbol	Test Condition	Min	Typ	Max	Units
V_{CC} for Data Retention	V_{DR1}	$\overline{CS1} \geq V_{CC} - 0.2V$ $CS2 \geq V_{CC} - 0.2V$ or $CS2 \leq 0.2V$	2.0	—	5.5	V
	V_{DR2}	$CS2 \leq 0.2V$	2.0	—	5.5	V
Data Retention Current	I_{DR1}	$V_{CC} = 3.0V$, $\overline{CS1} \geq V_{CC} - 0.2V$, $CS2 \geq V_{CC} - 0.2V$ or $CS2 \leq 0.2V$	—	1	50*	μA
	I_{DR2}	$V_{CC} = 3.0V$, $CS2 \leq 0.2V$	—	1	50*	μA
Data Retention Set-up Time	t_{SDR}	See Data Retention Wave forms (below)	0			ns
Recovery Time	t_{RDR}		t_{RC}**			ns

* 20μA max at T_A = 0 ~ 40°C, KM6264A: 1.0mA (MAX)
** t_{RC} = Read Cycle Time

DATA RETENTION WAVEFORM (1) ($\overline{CS1}$ Controlled)



DATA RETENTION WAVEFORM (2) (CS2 Controlled)



NOTE: In Data Retention Mode, CS2 controls the Address, $\overline{WE}$, $\overline{CS1}$, $\overline{OE}$ and Din buffer. If CS2 controls data retention mode, V_{IN} for these inputs can be in the high impedance state. If $\overline{CS1}$ controls the data retention mode, CS2 must satisfy either $CS2 \geq V_{CC} - 0.2V$ or $CS2 \leq 0.2V$. The other input levels (address, $\overline{WE}$, $\overline{OE}$, I/O) can be in the high impedance state.

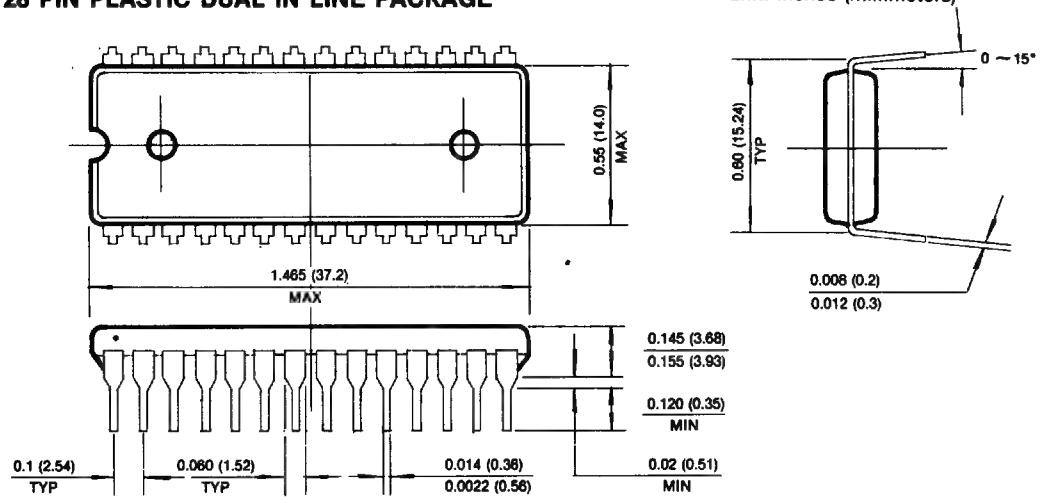
FUNCTION TABLE

$\overline{WE}$	$\overline{CS1}$	CS2	$\overline{OE}$	Mode	I/O Pin	V_{CC} Current
X	H	X	X	Power Down	High-Z	I_{SB}
X	X	L	X	Power Down	High-Z	I_{SB}
H	L	H	H	Output Disabled	High-Z	I_{CC}
H	L	H	L	Read	D_{OUT}	I_{CC}
L	L	H	X	Write	D_{IN}	I_{CC}

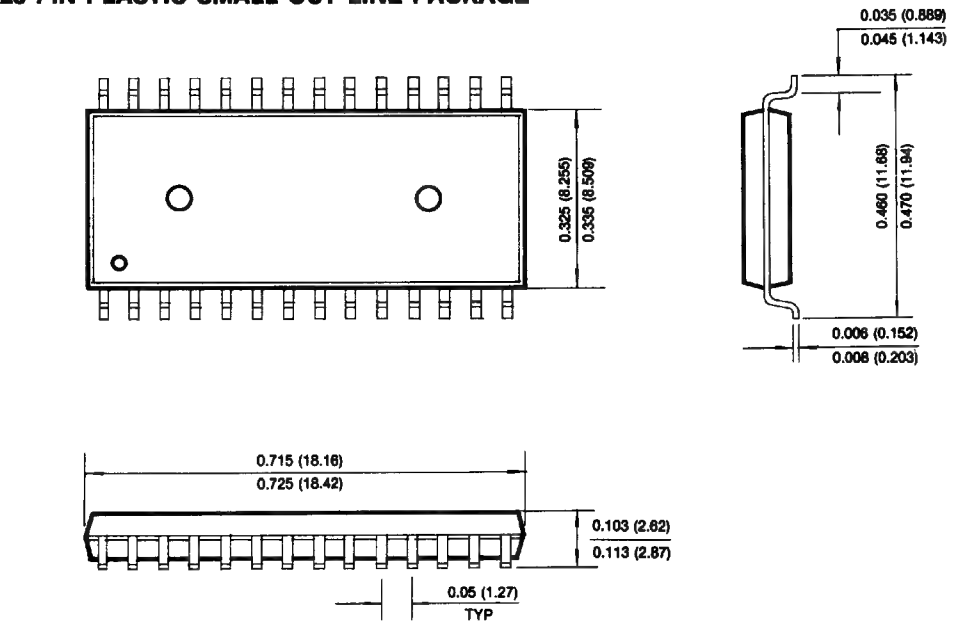
PACKAGE DIMENSIONS

28 PIN PLASTIC DUAL IN LINE PACKAGE

unit: inches (millimeters)



28 PIN PLASTIC SMALL OUT LINE PACKAGE



32K×8 Bit Static RAM

FEATURES

- **Fast Access Time 80, 100, 120 ns (max).**
- **Low Power Dissipation**
  - **Standby: 0.55mW (max.)**
  - **Operating: 248mW (max.)**
- **Low Data Retention Current: 50μA (max.)**
- **Capability of Battery Back-up Operation**
- **Data Retention Voltage: 2.0V (min.)**
- **Single 5V±10% supply**
- **TTL compatible inputs and outputs**
- **Pin compatible with 256K EPROMS**
- **Fully Static Operation**
  - **— No clock or refresh required**
- **Standard 28-pin DIP (600 mil) and 28-pin SOP (330 mil)**
- **Common I/O, Tristate Output**

GENERAL DESCRIPTION

The KM62256A/AL is a 262, 144 bit high speed Static Random Access Memory organized as 32,768 words by 8 bits.

This device is fabricated using advanced SST'S CMOS technology with polysilicon resistors.

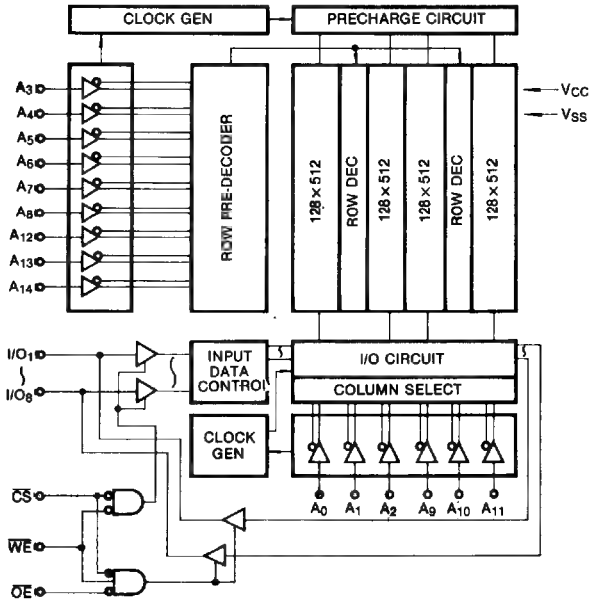
The KM62256A/AL has an output enable for precise control of the data output.

It also has a chip enable for the minimum current power down mode. The KM62256A/AL has been designed for high speed and low power applications. It is particularly well suited for battery back up non-volatile memory applications.

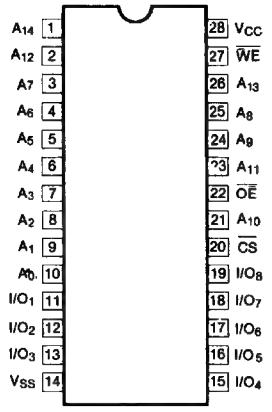
Two versions are available the KM62256A and KM62256AL. The L-version is specified with lower standby and data retention currents than the standard version.

Otherwise the two version are identical.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Pin Name	Pin Function
$A_0 \sim A_{14}$	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
$I/O_1 \sim I/O_8$	Data Inputs/Outputs
V_{CC}	+5V Power Supply
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS (See Note)*

Rating	Symbol	Value	Units
Voltage on any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−0.3 to V_{CC}+0.5	V
Voltage on V_{CC} Supply Relative to V_{CC}	V_{CC}	−0.5 to +7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	T_{stg}	−55 to +125	°C
Operating Temperature	T_A	0 to +70	°C

*Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS (T_A = 0°C to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	—	V_{CC}+0.5	V
Input Low Voltage	V_{IL}	−0.3*	—	0.8	V

* Note: V_{IL}(min) = −3.0V for ≤50ns pulse

DC AND OPERATING CHARACTERISTICS

(T_A = 0°C to 70°C, V_{CC} = 5V ± 10%, unless otherwise specified)

Parameter	Symbol	Test Conditions	Device	Min	Typ	Max	Units
Input Leakage Current	I_{LI}	V_{IN} = V_{SS} to V_{CC}				1	μA
Output Leakage Current	I_{LO}	$\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH} $V_{I/O}$ = V_{SS} to V_{CC}				1	μA
Operating Power Supply Current	I_{CC1}	$\overline{CS}$ = V_{IL}, I_{OUT} = 0mA				45	mA
Average Operating Current	I_{CC2}	Min Cycle, 100% Duty $\overline{CS}$ = V_{IL}, I_{OUT} = 0mA			35	70	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$ = V_{IH}				2	mA
	I_{SB1}	$\overline{CS}$ ≥ V_{CC} − 0.2V	KM62256A			1	mA
			KM62256AL		2	100	μA
Output Low Voltage	V_{OL}	I_{OL} = 2.1mA				0.4	V
Output High Voltage	V_{OH}	I_{OH} = −1.0mA		2.4			V

CAPACITANCE ($T_A = 25°C$, $V_{CC} = 5V$, $f = 1.0$ MHz)

Parameter	Symbol	Conditions	Min	Max	Unit
Input Capacitance	C_{IN}	$V_{IN} = 0V$	—	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O} = 0V$	—	8	pF

Note: Capacitance is periodically sampled and not 100% tested.

AC CHARACTERISTICS

($T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise specified)

TEST CONDITIONS

Parameter	Value
Input Pulse Levels	0.8 to 2.4V
Input Rise and Fall Times	5 ns
Input and Output Timing Reference Levels	1.5V
Output Load	1 TTL Load and $C_L = 100$ pF (Including scope and jig capacitance)

READ CYCLE

Parameter	Symbol	KM62256A-8 KM62256AL-8		KM62256A-10 KM62256AL-10		KM62256A-12 KM62256AL-12		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	80		100		120		ns
Address Access Time	t_{AA}		80		100		120	ns
Chip Select to Output	t_{ACS}		80		100		120	ns
Output Enable to Valid Output	t_{OE}		40		50		60	ns
Chip Enable to Low-Z Output	t_{CLA}	5		10		10		ns
Output Enable to Low-Z Output	t_{OLZ}	5		5		5		ns
Chip Disable to High-Z Output	t_{CHZ}	0	30	0	35	0	40	ns
Output Disable to High-Z Output	t_{OHZ}	0	30	0	35	0	40	ns
Output Hold from Address Change	t_{OH}	5		10		15		ns

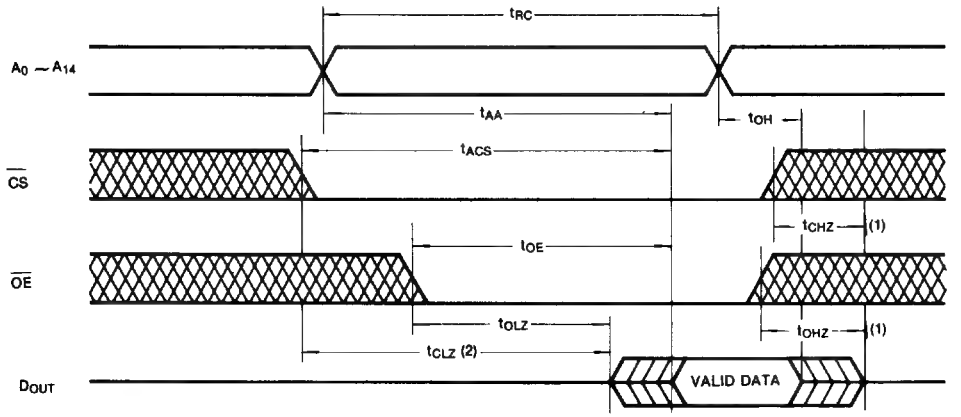
WRITE CYCLE

Parameter	Symbol	KM62256A-8 KM62256AL-8		KM62256A-10 KM62256AL-10		KM62256A-12 KM62256AL-12		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	80		100		120		ns
Chip Select to End of Write	t_{CW}	70		80		85		ns
Address Set-up Time	t_{AS}	0		0		0		ns
Address Valid to End of Write	t_{AW}	70		80		85		ns
Write Pulse Width	t_{WP}	55		60		70		ns
Write Recovery Time	t_{WR}	0		5		5		ns
Write to Output High-Z	t_{WHZ}	0	30	0	35	0	40	ns
Data to Write Time Overlap	t_{DW}	40		50		60		ns
Data Hold from Write Time	t_{DH}	0		0		0		ns
End of Write to Output Low-Z	t_{OW}	5		10		10		ns

NOTES:
1. t_{CHZ} and t_{OHZ} are definded as the time at which the outputs achieve the open circuit condition and are not referenced to the V_{OH} or V_{OL} level.
2. At any given temperature and voltage condition, t_{CHZ} max is less then t_{CLZ} min both for a given device and from device to device.
3. $\overline{WE}$ is high for read cycle.
4. Address valid prior to or coincident with $\overline{CS}$ transition low.
5. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
6. During this period, I/O pins are in the output state. The input signals out of phase must not applied.
7. $\overline{CS}$ or $\overline{WE}$ must be high during address transition.
8. If $\overline{OE}$ is high, I/O pins remain in a high-impedance state.
9. $\overline{OE}$ is continuously low. ($\overline{OE} = V_{IL}$)

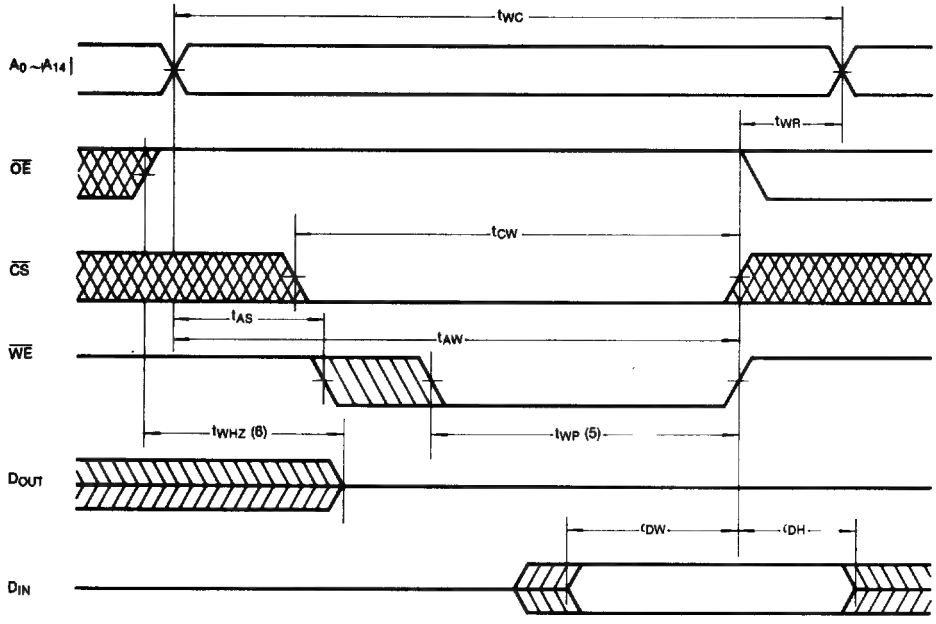
TIMING DIAGRAMS

READ CYCLE (NOTE 1,2,3,4)

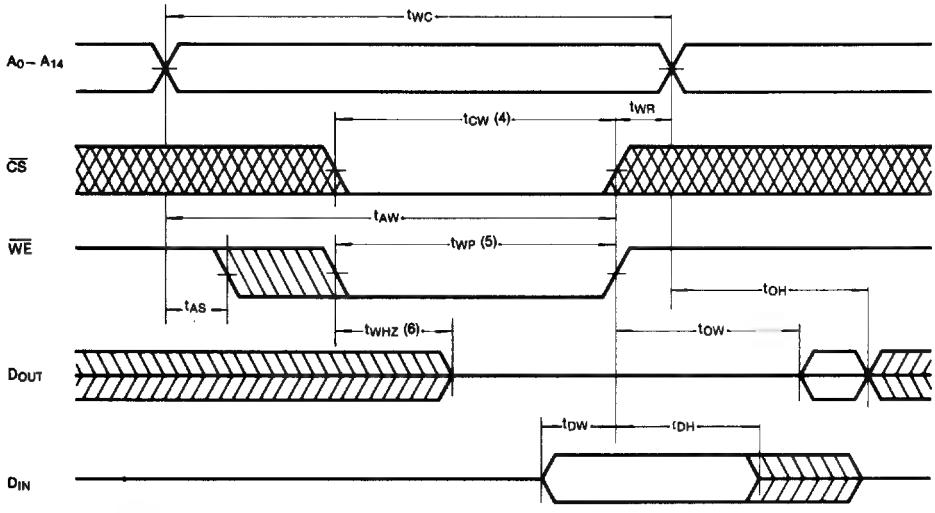


TIMING DIAGRAMS (Continued)

WRITE CYCLE 1 ($\overline{OE}$ Clocked) (NOTE 5,6,7,8)



WRITE CYCLE 2 ($\overline{OE}$ Low Fixed) (NOTE 5,6,7,8,9)



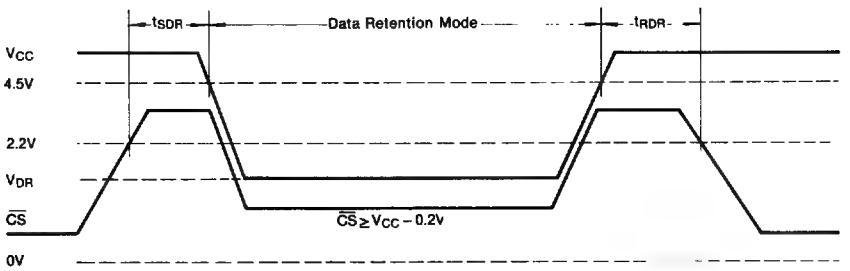
DATA RETENTION CHARACTERISTICS (T_A = 0°C to +70°C)

(This characteristic is guaranted only for L-version)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geq V_{CC} - 0.2V$	2.0		5.5	V
Data Retention Current	I_{DR}	$V_{CC} = 3.0V$ $\overline{CS} \geq V_{CC} - 0.2V$		1	50	μA
Data Retention Set-up Time	t_{SDR}	See Data Retention Wave forms (below)	0			ns
Recovery Time	t_{RDR}		t_{RC}*			ns

* t_{RC} = Read Cycle Time

DATA RETENTION WAVEFORM

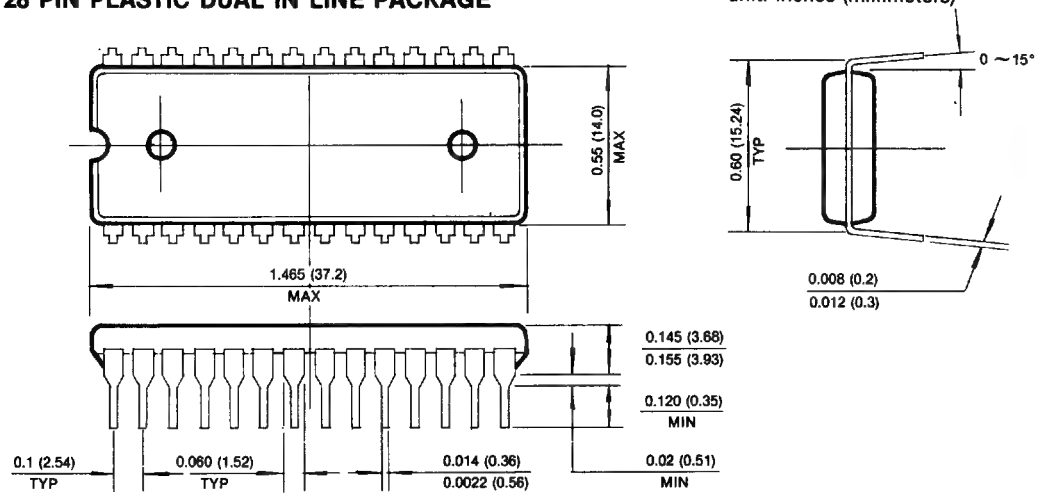


Note: The Other inputs (Address, $\overline{OE}$, $\overline{WE}$, I/O) can be in a high impedance state

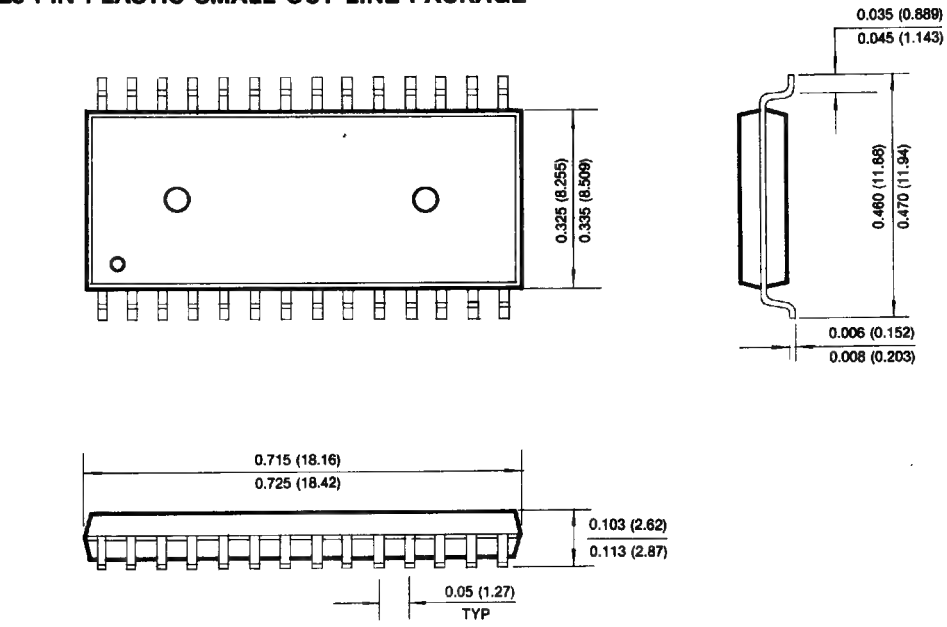
PACKAGE DIMENSIONS

28 PIN PLASTIC DUAL IN LINE PACKAGE

unit: inches (millimeters)



28 PIN PLASTIC SMALL OUT LINE PACKAGE



64K x 1 Bit Static RAM

FEATURES

- **Fast Access Time 25, 35, 45ns (max.)**
- **Low Power Dissipation**
  Standby (TTL): 3mA (max.)
  (CMOS): 100μA (max.)
  Operating : 100mA (max.)
- **Single 5V ± 10% supply**
- **TTL compatible inputs and outputs**
- **Full Static Operation**
  —No clock or refresh required
- **Tristate Output**
- **Low Data Retention Current: 50μA (max.)**
- **Battery Back-up Operation**
  —2V (min.) Data Retention
- **Standard 22-pin DIP (300mil) and 24-pin SOJ (300mil)**

GENERAL DESCRIPTION

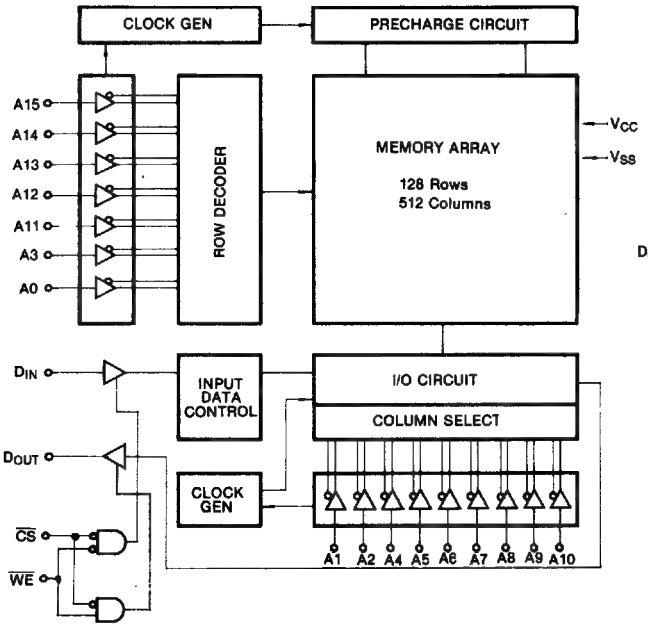
The KM6165 is a 65,536-bit high-speed Static Random Access Memory organized as 65,536 words by 1 bit.

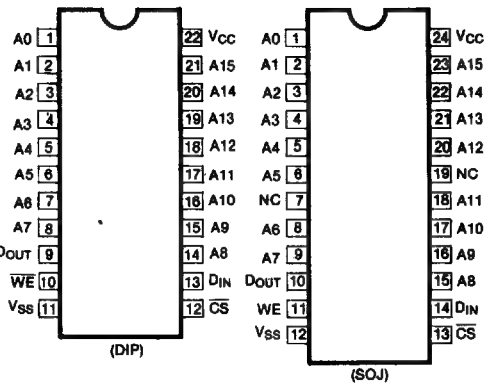
The device is fabricated using Samsung's advanced CMOS process.

The KM6165 has a chip enable input for the minimum current power down mode.

The KM6165 has been designed for high speed applications. It is particularly well suited for the use in high speed and low power applications in which battery back-up for nonvolatility is required.

FUNCTIONAL BLOCK DIAGRAM





PIN NAMES

Pin Name	Pin Function
A_0-A_{15}	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
D_{IN}/D_{OUT}	Data Inputs/Outputs
V_{CC}	+5V Power Supply
V_{SS}	Ground
NC	No Connection

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	$V_{in, out}$	−0.5 to 7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−0.5 to 7.0	V
Power Dissipation	P_d	1.0	W
Storage Temperature	T_{stg}	−55 to +125	°C
Operating Temperature	T_a	0 to 70	°C

*Note: Stresses grater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS (Ta = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2		$V_{CC}+0.3$	V
Input Low Voltage	V_{IL}*	−0.5		0.8	V

* V_{IL}(min) = −3.0V for ≤20ns pulse

DC AND OPERATING CHARACTERISTICS

(Ta = 0 to 70°C, V_{CC} = 5V ± 10%, unless otherwise specified)

Parameter	Symbol	Test Condition	Ver	Min	Max	Unit
Input Leakage Current	I_{LI}	$V_{IN} = V_{SS}$ to V_{CC}			2	μA
Output Leakage Current	I_{LO}	$\overline{CS} = V_{IH}$ or $\overline{WE} = V_{IL}$ $V_{I/O} = V_{SS}$ to V_{CC}			2	μA
Average Operating Current	I_{CC}	Min Cycle, 100% Duty $\overline{CS} = V_{IL}$, I_{OUT} = 0mA			100	mA
Standby Power Supply Current	I_{SB}	$\overline{CS} = V_{IH}$			3	mA
	I_{SB1}	$\overline{CS} \geq V_{CC} - 0.2V$			2	mA
			L		100	μA
Output Low Voltage	V_{OL}	I_{OL} = 8mA			0.4	V
Output High Voltage	V_{OH}	I_{OL} = −4mA		2.4		V

CAPACITANCE (f = 1MHz, Ta = 25°C)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN} = 0V	—	7	pF
Input/Output Capacitance	C_{OUT}	V_{OUT} = 0V	—	7	pF

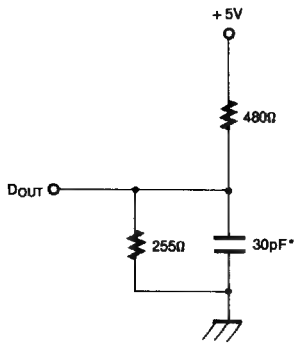
*Note: Capacitance is sampled and not 100% tested.

AC CHARACTERISTICS

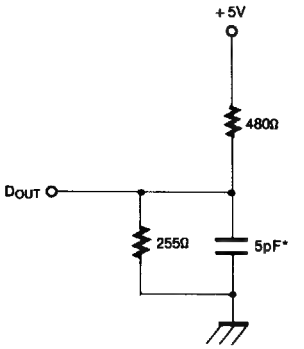
TEST CONDITIONS (Ta = 0 to 70°C, V_{CC} = 5V ± 10%, unless otherwise specified)

Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Time	5 ns
Input and Output Timing Reference Levels	1.5V
Output Load	See below

Output Load(a)



Output Load(b)
(for t_{HZ}, t_{LZ}, t_{WZ} & t_{OW})



*Including Scope and Jig Capacitance

READ CYCLE

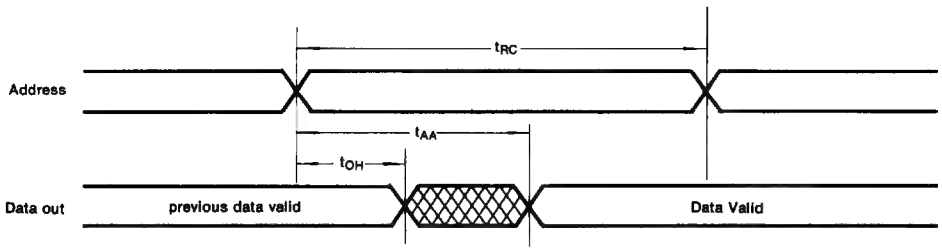
Parameter	Symbol	KM6165-25 KM6165L-25		KM6165-35 KM6165L-35		KM6165-45 KM6565L-45		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	25		35		45		ns
Address Access Time	t_{AA}		25		35		45	ns
Chip Select to Output	t_{ACS}		25		35		45	ns
Chip Enable to Low-Z Output	t_{LZ}	5		5		5		ns
Chip Disable to High-Z Output	t_{HZ}	0	15	0	15	0	20	ns
Output Hold from Address Change	t_{OH}	5		5		5		ns
Chip Selection to Power Up Time	t_{PU}	0		0		0		ns
Chip Desselection to Power Down Time	t_{PD}		25		35		45	ns

WRITE CYCLE

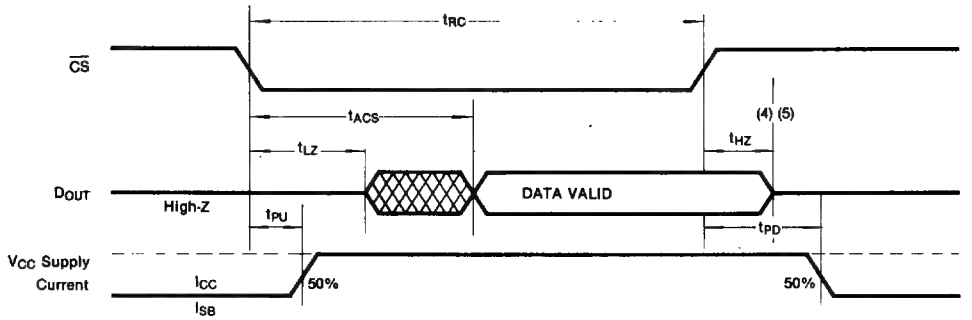
Parameter	Symbol	KM6165-25 KM6165L-25		KM6165-35 KM6165L-35		KM6165-45 KM6565L-45		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	20		30		40		ns
Chip Select to End of Write	t_{CW}	20		30		40		ns
Address Set-Up Time	t_{AS}	0		0		0		ns
Address Valid to End of Write	t_{AW}	20		30		40		ns
Write Pulse Width	t_{WP}	20		25		35		ns
Write Recovery Time	t_{WR}	0		0		0		ns
Write to Output High-Z	t_{WZ}	0	15	0	20	0	20	ns
Data to Write Time Overlap	t_{DW}	15		20		25		ns
Data Hold from Write Time	t_{DH}	0		0		0		ns
End Write to Output Low-Z	t_{OW}	5		5		5		ns

TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE (Address Controlled)



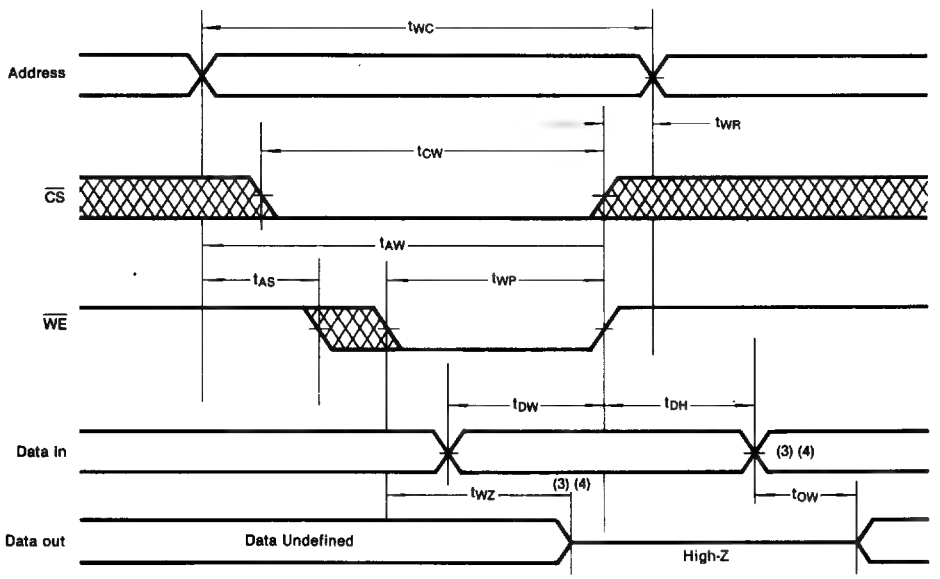
TIMING WAVEFORM OF READ CYCLE ($\overline{CS}$ Controlled)



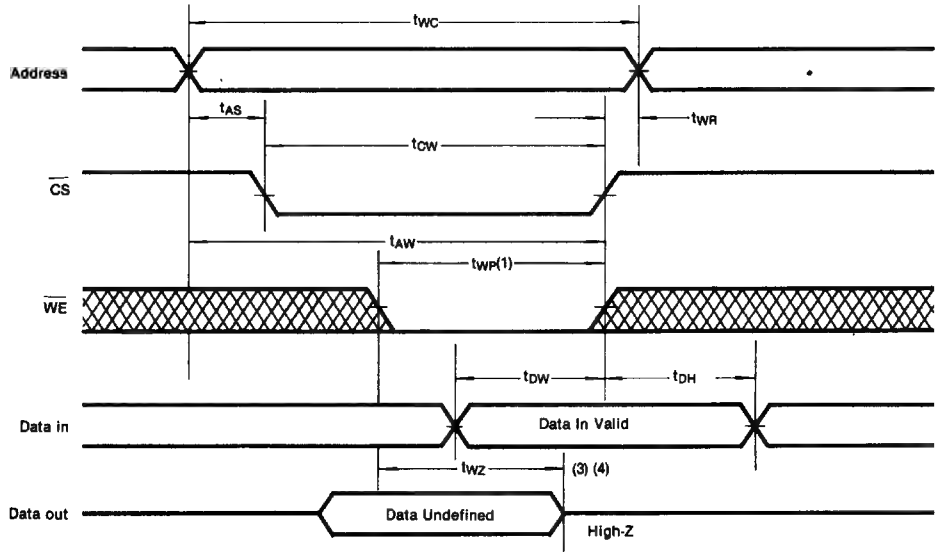
Note (READ CYCLE)

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. At any given temperature and voltage condition, t_{HZ}(max.) is less than t_{LZ}(min.) both for a given device and from device to device.
4. Transition is measured ±200mV from steady state voltage with Load(b).
5. This parameter is sampled and not 100% tested.
6. Device is continuosly selected with $\overline{CS} = V_{IL}$
7. Address valid prior to coincident with $\overline{CS}$ transition low.

TIMING WAVEFORM OF WRITE CYCLE ($\overline{WE}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE ($\overline{CS}$ Controlled)



Note (WRITE CYCLE)

1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and low $\overline{WE}$.
2. All write cycle timing is referenced from the last valid address to the first transition address.
3. Transition is measured ±200mV from steady state voltage with Load(b).
4. This parameter is sampled and not 100% tested.
5. At any given temperature and voltage condition, t_{WZ}(max.) is less than t_{OW}(min.) both for a given device and from device to device.
6. $\overline{CS}$ or $\overline{WE}$ must be in high during address transition.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	I/O PIN	Supply Current	Mode
H	X	High-Z	I_{SB}, I_{SB1}	Not Select
L	H	D_{OUT}	I_{CC1}, I_{CC2}	Read
L	L	D_{IN}	I_{CC1}, I_{CC2}	Write

*Note: X means Don't Care

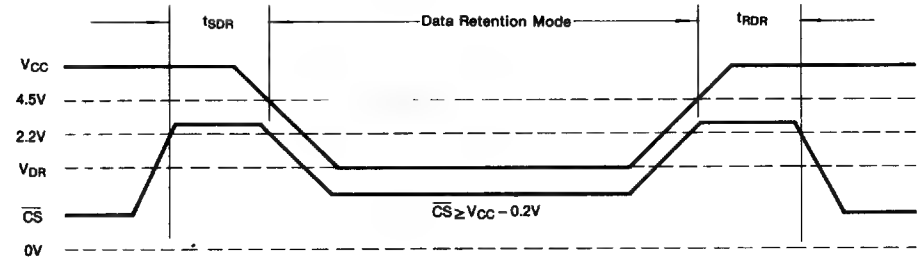
DATA RETENTION CHARACTERISTICS (Ta = 0 to 70°C)

(This characteristics is guaranteed only for L-version)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
V_{CC} for Data Retention	V_{DR}	$CS \geq V_{CC} - 0.2V$	2.0		5.5	V
Data Retention Current	I_{DR}	$V_{CC} = 3V$ $CS \geq V_{CC} - 0.2V$		1	50	μA
Data Retention Set-up Time	t_{SDR}	See Data Retention Waveforms (below)	0			nS
Recovery Time	t_{RDR}		t_{RC}*			nS

*t_{RC} = Read Cycle Time

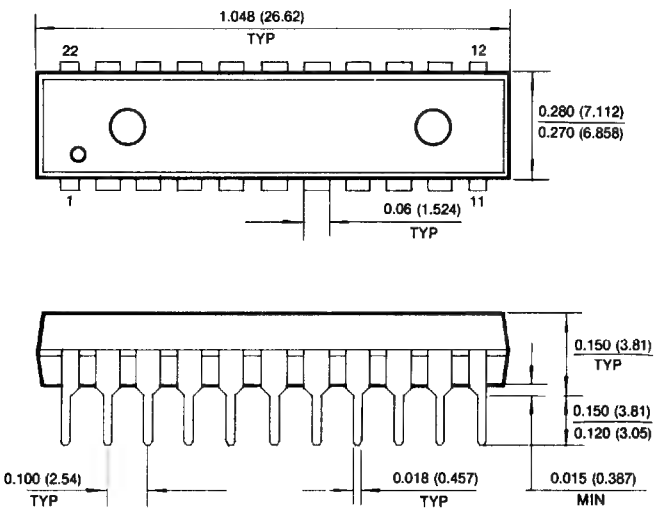
DATA RETENTION WAVEFORM



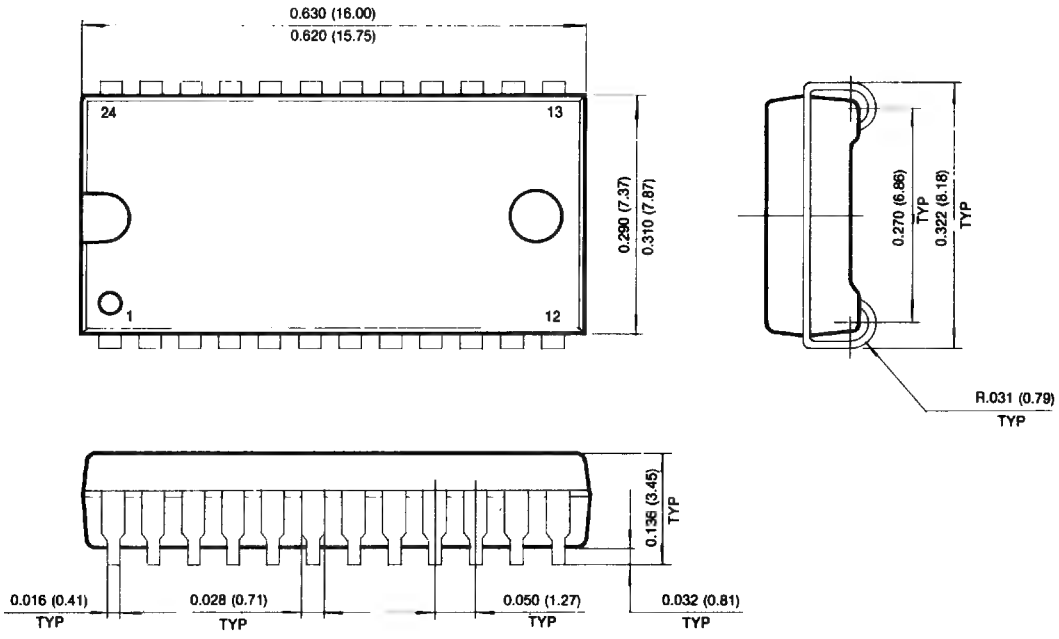
PACKAGE DIMENSIONS

Unit: Inches (millimeters)

22-PIN PLASTIC DUAL-IN-LINE PACKAGE



24-PIN PLASTIC SMALL OUT-LINE FORM PACKAGE



16K x 4 Bit Static RAM

FEATURE

- **Fast Access Time 25,35,45ns(max.)**
- **Low Power Dissipation**
  - **Standby (TTL) : 2 mA (max.)**
  - **(CMOS): 100 μA (max.)**
  - **Operating : 100 mA (max.)**
- **Single 5V ± 10% Power Supply**
- **TTL compatible inputs and output**
- **Full Static Operation**
  - **— No clock or refresh required**
- **Tri-state Output**
- **Low Data Retention Current: 50 μA (max.)**
- **Battery Back-up Operation**
  - **— 2V (min.) Data Retention**
- **Standard 22-pin DIP (300mil)**

GENERAL DESCRIPTION

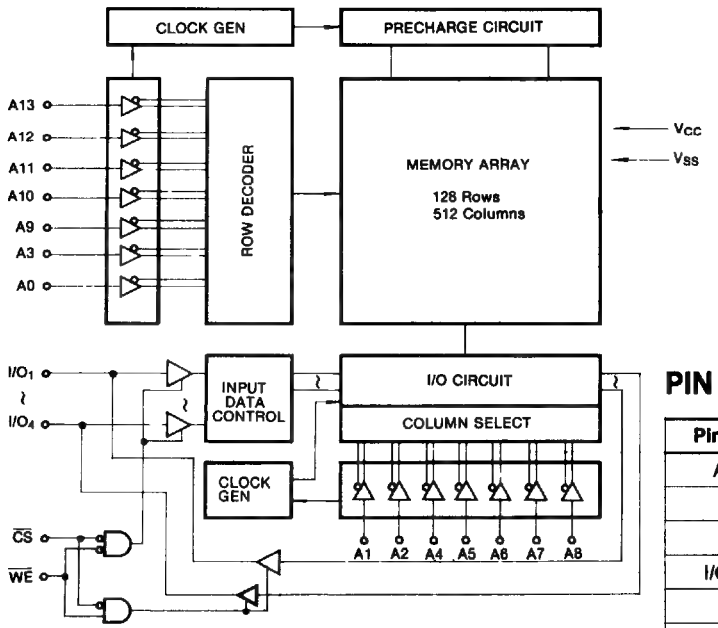
The KM6465P/LP is a 65,536-bit high-speed Static Random Access Memory organized as 16,384 words by 4 bit.

The device is fabricated using Samsung's advanced CMOS process.

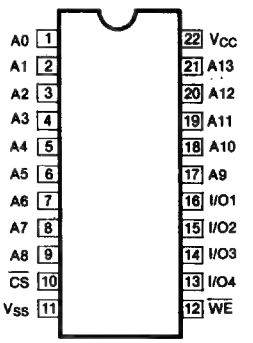
The KM6465P/LP has a chip enable input for the minimum current power down mode.

The KM6465P/LP has been designed for high speed applications. It is particularly well suited for the use in high speed and low power applications in which battery back-up for nonvolatility is required.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



PIN NAMES

Pin Name	Pin Function
A_0-A_{13}	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
I/O_1-I/O_4	Data Inputs/Outputs
V_{CC}	+5V Power Supply
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	$V_{in, out}$	−0.5 to 7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−0.5 to 7.0	V
Power Dissipation	P_d	1.0	W
Storage Temperature	T_{stg}	−55 to +125	°C
Operating Temperature	T_a	0 to 70	°C

*Note: Stresses grater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS (Ta = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.0		$V_{CC}+0.3$	V
Input Low Voltage	V_{IL}*	−0.5		0.8	V

* V_{IL}(min) = −3.0V for <20ns pulse

DC AND OPERATING CHARACTERISTICS

(Ta = 0 to 70°C, V_{CC} = 5V ± 10%, unless otherwise specified)

Parameter	Symbol	Test Condition	Ver	Min	Max	Unit
Input Leakage Current	I_{LI}	$V_{IN} = V_{SS}$ to V_{CC}			1	μA
Output Leakage Current	I_{LO}	$\overline{CS} = V_{IH}$ or $\overline{WE} = V_{IL}$ $V_{I/O} = V_{SS}$ to V_{CC}			1	μA
Operating Power Supply Current	I_{CC1}	$\overline{CS} = V_{IL}$, $V_{IN} = V_{IL}/V_{IH}$ I_{OUT} = 0mA			20	mA
Average Operating Current	I_{CC2}	Min Cycle, 100% Duty $\overline{CS} = V_{IL}$, I_{OUT} = 0mA			120	mA
Standby Power Supply Current	I_{SB}	$\overline{CS} = V_{IH}$			3	mA
	I_{SB1}	$\overline{CS} \geq V_{CC} - 0.2V$	P		2	mA
			LP		100	μA
Output Low Voltage	V_{OL}	I_{OL} = 8mA			0.4	V
Output High Voltage	V_{OH}	I_{OL} = −4mA		2.4		V

CAPACITANCE (f = 1MHz, Ta = 25°C)

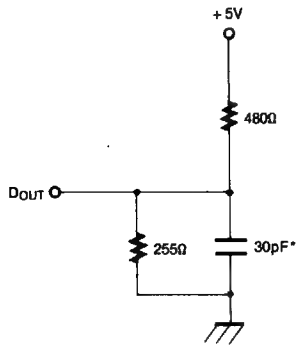
Parameter	Symbol	Test Conditions	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN} = 0V	—	7	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	—	7	pF

*Note: Capacitance is sampled and not 100% tested.

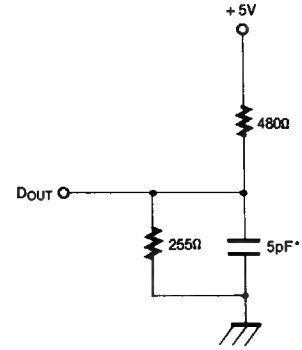
TEST CONDITIONS (Ta = 0 to 70°C, V_{CC} = 5V ± 10%, unless otherwise specified)

Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Time	5 ns
Input and Output Timing Reference Levels	1.5V
Output Load	See below

Output Load(a)



Output Load(b)
(for t_{HZ}, t_{LZ}, t_{WZ} & t_{OW})



*Including Scope and Jig Capacitance

READ CYCLE

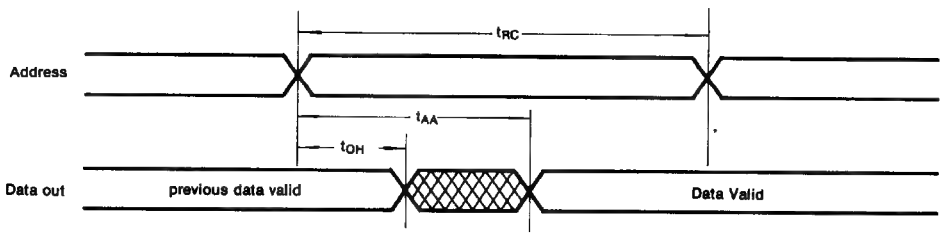
Parameter	Symbol	KM6465P-25 KM6465LP-25		KM6465P-35 KM6465LP-35		KM6465P-45 KM6465LP-45		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	25		35		45		ns
Address Access Time	t_{AA}		25		35		45	ns
Chip Select to Output	t_{ACS}		25		35		45	ns
Chip Enable to Low-Z Output	t_{LZ}	5		7		10		ns
Chip Disable to High-Z Output	t_{HZ}	0	10	0	12	0	15	ns
Output Hold from Address Change	t_{OH}	5		5		5		ns
Chip Selection to Power Up Time	t_{PU}	0		0		0		ns
Chip Desselection to Power Down Time	t_{PD}		25		35		45	ns

WRITE CYCLE

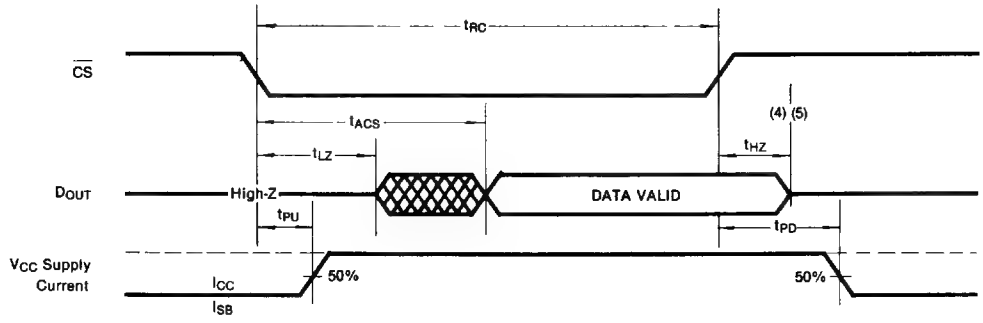
Parameter	Symbol	KM6465P-25 KM6465LP-25		KM6465P-35 KM6465LP-35		KM6465P-45 KM6465LP-45		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	20		30		40		ns
Chip Select to End of Write	t_{CW}	20		30		40		ns
Address Set-Up Time	t_{AS}	0		0		0		ns
Address Valid to End of Write	t_{AW}	20		30		40		ns
Write Pulse Width	t_{WP}	20		25		30		ns
Write Recovery Time	t_{WR}	0		0		0		ns
Write to Output High-Z	t_{WZ}	0	7	0	10	0	15	ns
Data to Write Time Overlap	t_{DW}	10		12		15		ns
Data Hold from Write Time	t_{DH}	0		0		0		ns
End Write to Output Low-Z	t_{OW}	5		7		10		ns

TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE (Address Controlled)



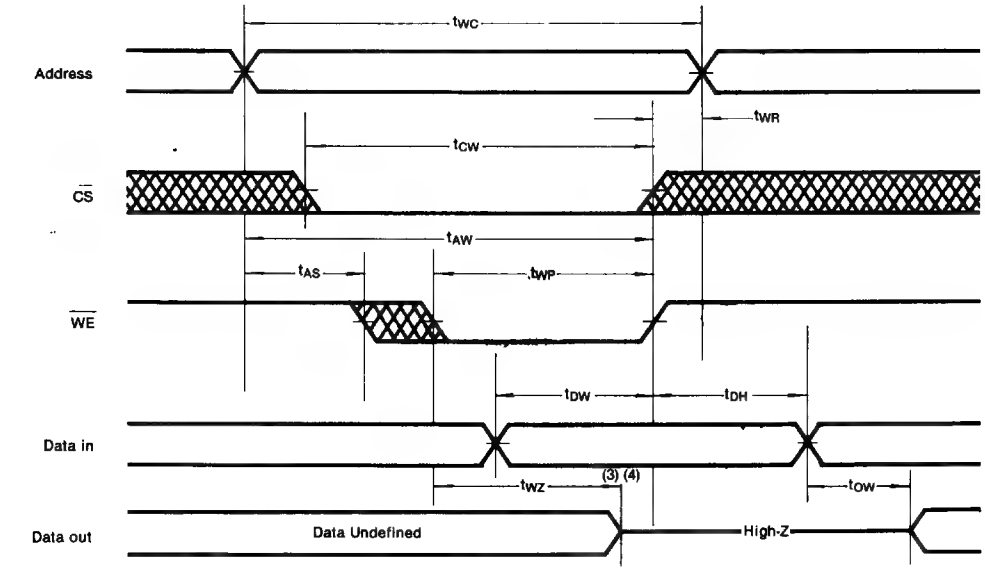
TIMING WAVEFORM OF READ CYCLE ($\overline{CS}$ Controlled)



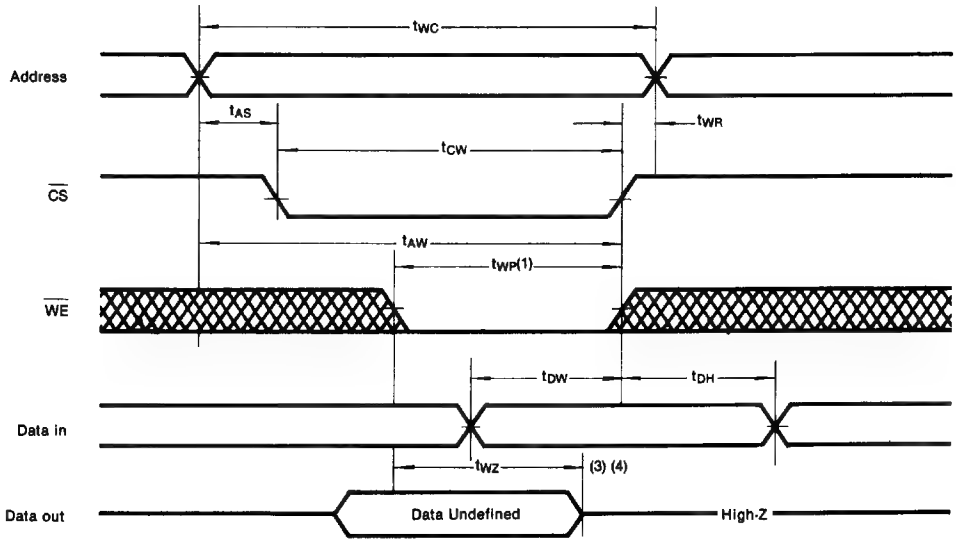
Note (READ CYCLE)

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. At any given temperature and voltage condition, t_{HZ}(max.) is less than t_{LZ}(min.) both for a given device and from device to device.
4. Transition is measured ±200mV from steady state voltage with Load(b).
5. This parameter is sampled and not 100% tested.
6. Device is continuosly selected with $\overline{CS} = V_{IL}$
7. Address valid prior to or coincident with $\overline{CS}$ transition low.

TIMING WAVEFORM OF WRITE CYCLE ($\overline{WE}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE ($\overline{CS}$ Controlled)



Note (WRITE CYCLE)

1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and low $\overline{WE}$.
2. All write cycle timing is referenced from the last valid address to the first transition address.
3. Transition is measured ±200mV from steady state voltage with Load(b).
4. This parameter is sampled and not 100% tested.
5. At any given temperature and voltage condition, t_{WZ}(max.) is less than t_{OW}(min.) both for a given device and from device to device.
6. $\overline{CS}$ or $\overline{WE}$ must be in high during address transition.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	I/O PIN	Supply Current	Mode
H	X	High-Z	I_{SB}, I_{SB1}	Not Select
L	H	D_{OUT}	I_{CC}	Read
L	L	D_{IN}	I_{CC}	Write

*Note: X means Don't Care

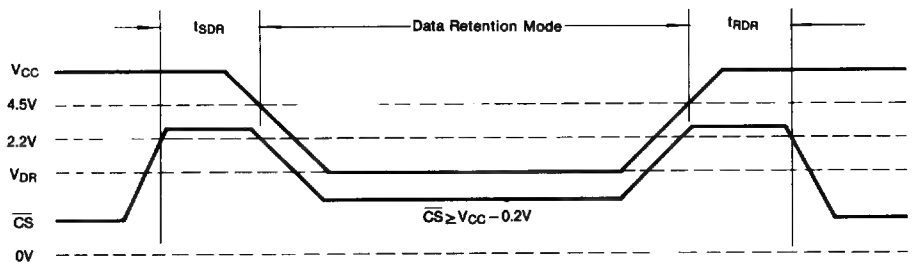
DATA RETENTION CHARACTERISTICS (Ta=0 to 70°C)

(This characteristics is guaranteed only for L-version)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geq V_{CC} - 0.2V$	2.0		5.5	V
Data Retention Current	I_{DR}	$V_{CC} = 3V$ $\overline{CS} \geq V_{CC} - 0.2V$		1	50	μA
Data Retention Set-up Time	t_{SDR}	See Data Retention Waveforms (below)	0		nS	
Recovery Time	t_{RDR}		t_{RC}*			nS

*t_{RC} = Read Cycle Time

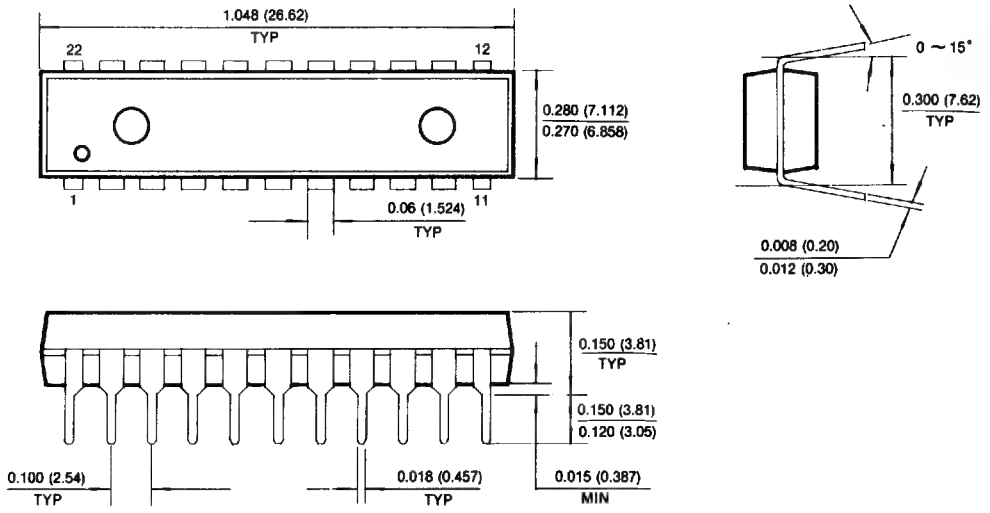
DATA RETENTION WAVEFORM



PACKAGE DIMENSIONS

Unit: Inches (millimeters)

22-PIN PLASTIC DUAL-IN-LINE PACKAGE



8K x 8 Bit Static RAM

FEATURE

- **Fast Access Time 35,45,55ns(max.)**
- **Low Power Dissipation**
  - **Standby (TTL) : 3 mA (max.)**
  - **(CMOS): 100 μA (max.)**
  - **Operating : 120 mA (max.)**
- **Single 5V ± 10% Power Supply**
- **TTL compatible inputs and output**
- **Full Static Operation**
  - **— No clock or refresh required**
- **Tri-state Output**
- **Low Data Retention Current: 50 μA (max.)**
- **Battery Back-up Operation**
  - **— 2V (min.) Data Retention**
- **Standard 28-pin DIP (300 mil)**

GENERAL DESCRIPTION

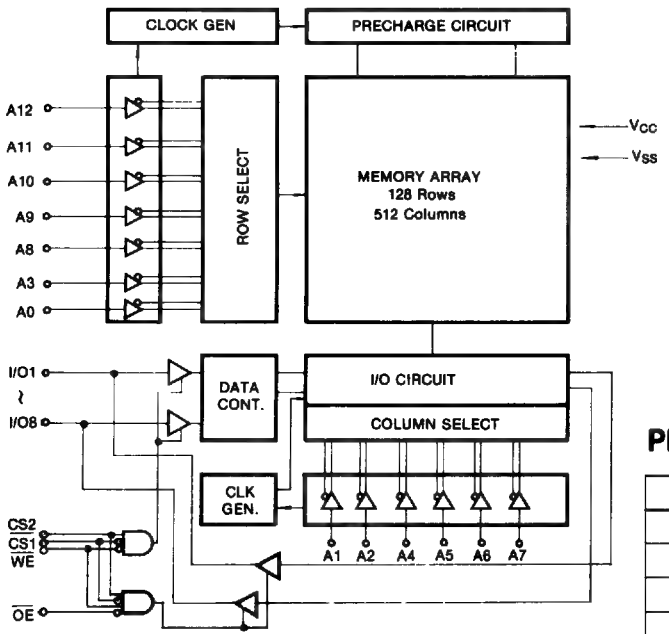
The KM6865P/LP is a 65,536-bit high-speed Static Random Access Memory organized as 8,192 words by 8 bit.

The device is fabricated using Samsung's advanced CMOS process.

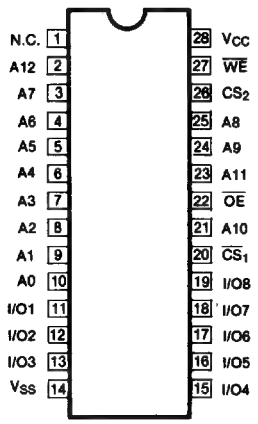
The KM6865P/LP has an output enable input for precise control of the data outputs. It also has a chip enable input for the minimum current power down mode.

The KM6865P/LP has been designed for high speed applications. It is particularly well suited for the use in high speed and low power applications in which battery back-up for nonvolatility is required.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



PIN NAMES

Pin Name	Pin Function
A_0-A_{12}	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS_1}$, CS_2	Chip Select
$\overline{OE}$	Output Enable
I/O_1-I/O_8	Data Inputs/Outputs
V_{CC}	+5V Power Supply
V_{SS}	Ground
N.C.	No Connection

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	$V_{in, out}$	−0.5 to 7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−0.5 to 7.0	V
Power Dissipation	P_d	1.0	W
Storage Temperature	T_{stg}	−55 to +125	°C
Operating Temperature	T_a	0 to 70	°C

*Note: Stresses grater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS (T_a = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2		V_{CC} + 0.3	V
Input Low Voltage	V_{IL}*	−0.5		0.8	V

* V_{IL}(min) = −3.0V for <20ns pulse

DC AND OPERATING CHARACTERISTICS

(T_a = 0 to 70°C, V_{CC} = 5V ± 10%, unless otherwise specified)

Parameter	Symbol	Test Condition	Ver	Min	Max	Unit
Input Leakage Current	I_{LI}	$V_{IN} = V_{SS}$ to V_{CC}		−1	2	μA
Output Leakage Current	I_{LO}	$\overline{CS1} = V_{IH}$ or CS2 = V_{IL} $\overline{WE} = V_{IL}$ $V_{I/O} = V_{SS}$ to V_{CC}		−1	2	μA
Average Operating Current	I_{CC}	Min Cycle, 100% Duty $\overline{CS1} = V_{IL}$, CS2 = V_{IH} I_{OUT} = 0mA			120	mA
Standby Power Supply Current	I_{SB}	$\overline{CS1} = V_{IH}$, CS2 = V_{IL}			3	mA
	I_{SB1}	$\overline{CS1} \geq V_{CC} - 0.2V$	P		2	mA
		CS2 < 0.2V	LP		100	μA
Output Low Voltage	V_{OL}	I_{OL} = 8mA			0.4	V
Output High Voltage	V_{OH}	I_{OL} = −4mA		2.4		V

CAPACITANCE (f = 1MHz, T_a = 25°C)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN} = 0V	—	7	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	—	7	pF

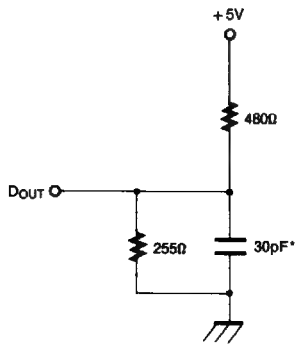
*Note: Capacitance is sampled and not 100% tested.

AC CHARACTERISTICS

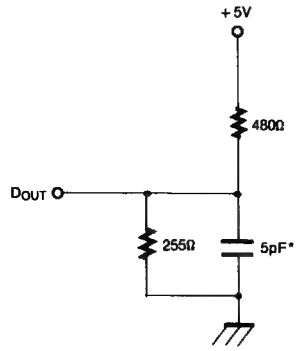
TEST CONDITIONS ($T_a = 0$ to 70°C, $V_{CC} = 5V \pm 10\%$, unless otherwise specified)

Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Time	5 ns
Input and Output Timing Reference Levels	1.5V
Output Load	See below

Output Load(a)



Output Load(b)
(for t_{HZ}, t_{LZ}, t_{WZ} & t_{OW})



*Including Scope and Jig Capacitance

READ CYCLE

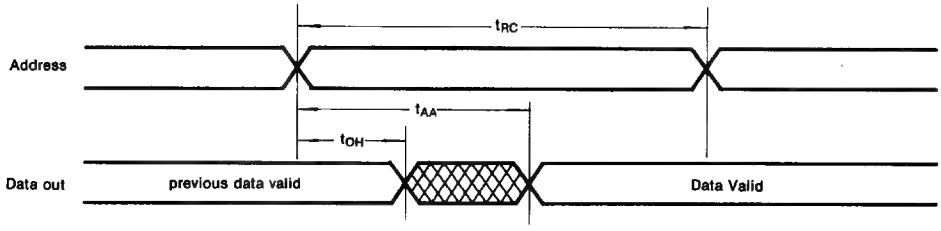
Parameter	Symbol	KM6865P-35 KM6865LP-35		KM6865P-45 KM6865LP-45		KM6865P-55 KM6865LP-55		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	35		45		55		ns
Address Access Time	t_{AA}		35		45		55	ns
Chip Select to Output	t_{ACS}		35		45		55	ns
Output Enable to Output	t_{OE}		15		20		25	ns
Output Enable to Low-Z	t_{OLZ}	5		5		5		ns
Chip Disable to High-Z Output	t_{HZ}	0	15	0	15	0	20	ns
Output Disable to High-Z	t_{OHZ}	0	15	0	20	0	25	ns
Output Hold from Address Change	t_{OH}	5		5		5		ns
Chip Selection to Power Up Time	t_{PU}	0		0		0		ns
Chip Desselection to Power Down Time	t_{PD}		25		35		45	ns

WRITE CYCLE

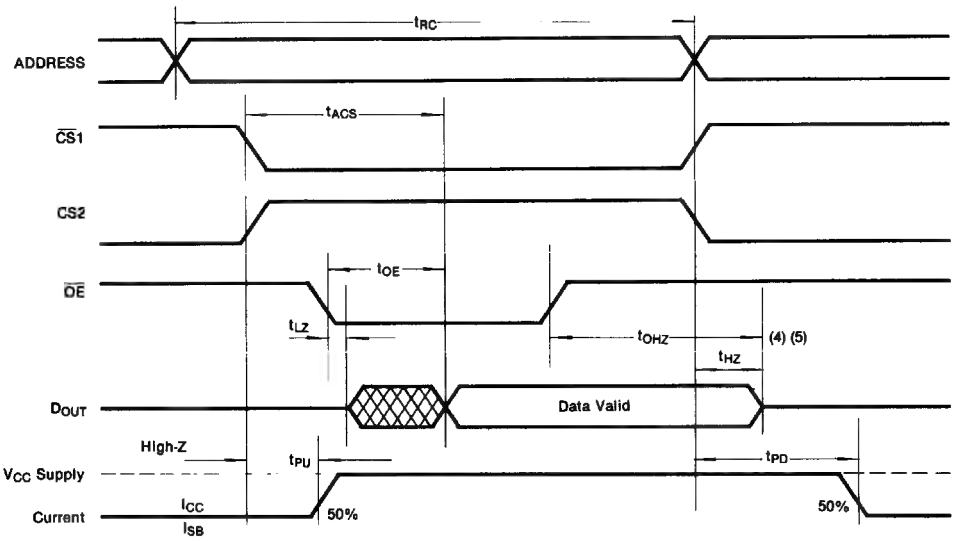
Parameter	Symbol	KM6865P-35 KM6865LP-35		KM6865P-45 KM6865LP-45		KM6865P-55 KM6865LP-55		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	30		40		40		ns
Chip Select to End of Write	t_{CW}	30		40		40		ns
Address Set-Up Time	t_{AS}	0		0		0		ns
Address Valid to End of Write	t_{AW}	30		40		40		ns
Write Pulse Width	t_{WP}	30		40		50		ns
Write Recovery Time	t_{WR}	0		0		0		ns
Write to Output High-Z	t_{WZ}	0	15	0	20	0	25	ns
Data to Write Time Overlap	t_{DW}	15		20		25		ns
Data Hold from Write Time	t_{DH}	0		0		0		ns
End Write to Output Low-Z	t_{OW}	5		5		5		ns

TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE NO: 1 (Note 1, 2, 6)



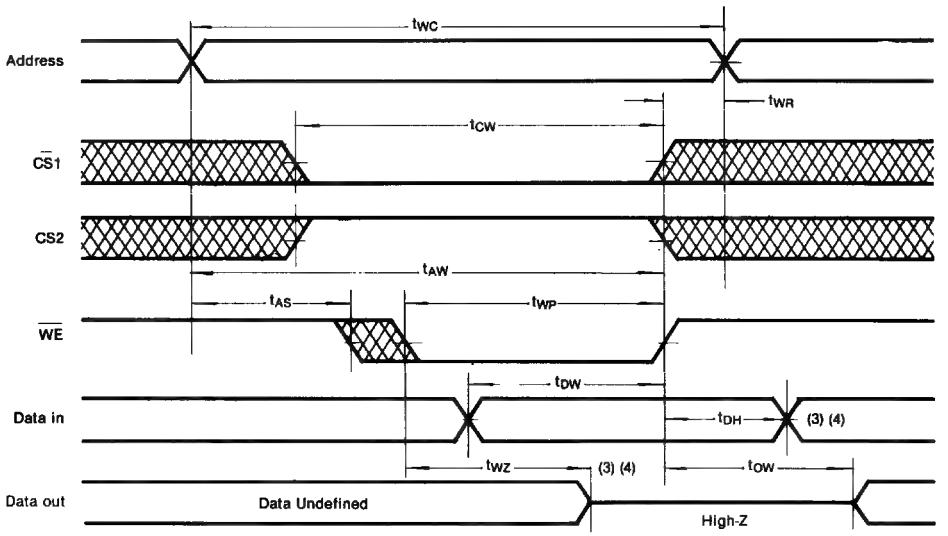
TIMING WAVEFORM OF READ CYCLE NO: 2 (Note 1, 3, 5, 7)



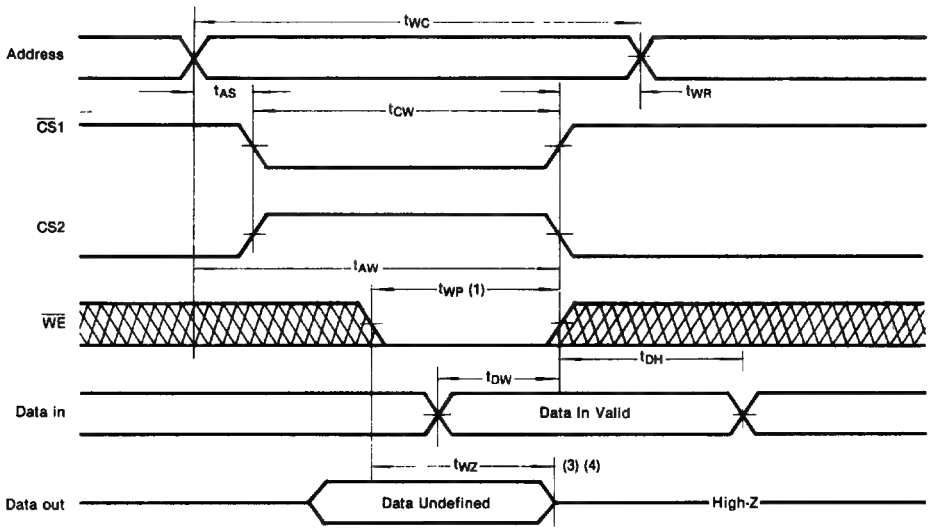
Note (READ CYCLE)

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. At any given temperature and voltage condition, t_{HZ}(max.) is less than t_{LZ}(min.) both for a given device and from device to device.
4. Transition is measured ±200mV from steady state voltage with Load(b).
5. This parameter is sampled and not 100% tested.
6. Device is continuosly selected with $\overline{CS1} = V_{IL}$, $CS2 = V_{IH}$
7. Address valid prior to coincident with $\overline{CS1}$ transition low.

TIMING WAVEFORM OF WRITE CYCLE ($\overline{WE}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE ($\overline{CS}$ Controlled)



Note (WRITE CYCLE)

1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}1$, a high CS2 and low $\overline{WE}$.
2. All write cycle timing is referenced from the last valid address to the first transition address.
3. Transition is measured ±200mV from steady state voltage with Load(b).
4. This parameter is sampled and not 100% tested.
5. At any given temperature and voltage condition, t_{WZ}(max.) is less than t_{OW}(min.) both for a given device and from device to device.
6. $\overline{CS}1$ or $\overline{WE}$ must be high or CS2 must be low during address transition.

FUNCTIONAL DESCRIPTION

$\overline{CS1}$	CS2	$\overline{WE}$	$\overline{OE}$	I/O PIN	Supply Current	Mode
H	X	X	X	High-Z	I_{SB}, I_{SB1}	Standby Mode
X	L	X	X	High-Z	I_{SB}, I_{SB1}	Standby Mode
L	H	H	H	High-Z	I_{CC}	Output Disable
L	H	H	L	D_{OUT}	I_{CC}	Read
L	H	L	X	D_{IN}	I_{CC}	Write

*Note: X means Don't Care

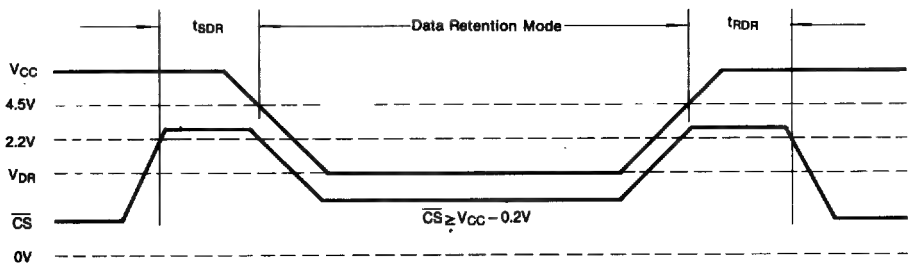
DATA RETENTION CHARACTERISTICS (Ta = 0 to 70°C)

(This characteristics is guaranteed only for L-version)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
V_{CC} for Data Retention	V_{DR}	$CS \geq V_{CC} - 0.2V$	2.0		5.5	V
Data Retention Current	I_{DR}	$V_{CC} = 3V$ $CS \geq V_{CC} - 0.2V$		1	50	μA
Data Retention Set-up Time	t_{SDR}	See Data Retention Waveforms (below)	0		nS	
Recovery Time	t_{RDR}		t_{RC}*			nS

*t_{RC} = Read Cycle Time

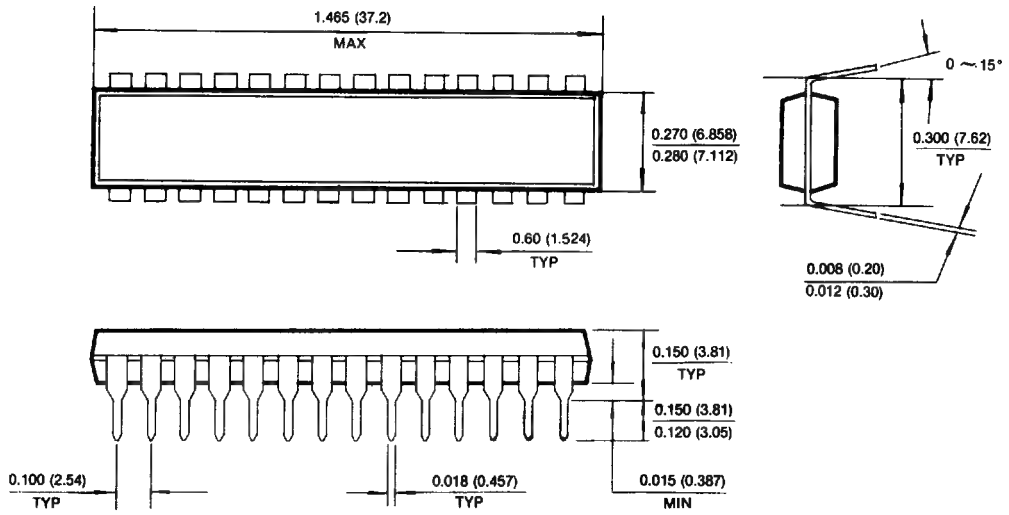
DATA RETENTION WAVEFORM



PACKAGE DIMENSIONS

28 LEAD PLASTIC DUAL IN LINE PACKAGE

Units: Inches (millimeters)



256K x 1 Bit Static RAM

FEATURES

- **Fast Access Time 25,35,45ns(max.)**
- **Low Power Dissipation**
  - **Standby (TTL) : 3 mA (max.)**
  - **(CMOS): 100 μA (max.)**
  - **Operating : 100 mA (max.)**
- **Single 5V ± 10% Power Supply**
- **TTL compatible Inputs and output**
- **Full Static Operation**
  - **— No clock or refresh required**
- **Tri-state Output**
- **Low Data Retention Current: 50 μA (max.)**
- **Battery Back-up Operation**
  - **— 2V (min.) Data Retention**
- **Standard 24-pin DIP (300mil) and 24-pin SOJ (300 mil)**

GENERAL DESCRIPTION

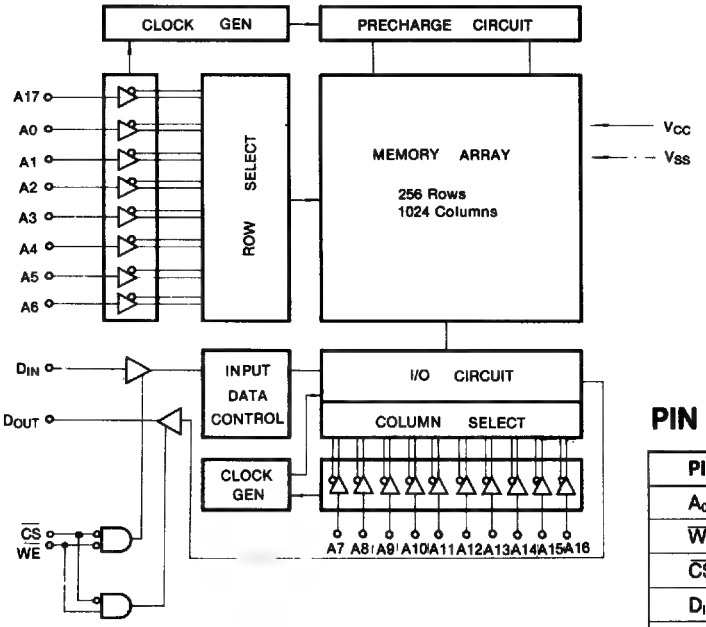
The KM61257 is a 262,144-bit high-speed Static Random Access Memory organized as 262,144 words by 1 bit.

The device is fabricated using Samsung's advanced CMOS process.

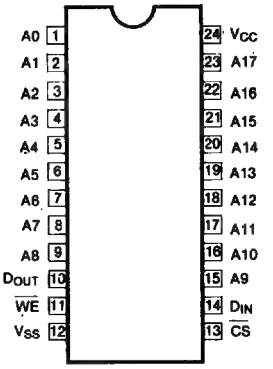
The KM61257 has a chip enable input for the minimum current power down mode.

The KM61257 has been designed for high speed applications. It is particularly well suited for the use in high speed and low power applications in which battery back-up for nonvolatility is required.

FUNCTION BLOCK DIAGRAM



PIN CONFIGURATION



PIN NAMES

Pin Name	Pin Function
A_0-A_{17}	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
D_{IN}	Data Input
D_{OUT}	Data Output
V_{CC}	Power (+5V)
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	$V_{in, out}$	−0.5 to 7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−0.5 to 7.0	V
Power Dissipation	P_d	1.0	W
Storage Temperature	T_{stg}	−55 to +125	°C
Operating Temperature	T_a	0 to 70	°C

*Note: Stresses grater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS (Ta = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2		$V_{CC}+0.5$	V
Input Low Voltage	V_{IL}*	−0.5		0.8	V

* $V_{IL}(min) = -3.0V$ for <20ns pulse

DC AND OPERATING CHARACTERISTICS

(Ta = 0 to 70°C, $V_{CC} = 5V \pm 10\%$, unless otherwise specified)

Parameter	Symbol	Test Condition	Ver	Min	Max	Unit
Input Leakage Current	I_{LI}	$V_{IN} = V_{SS}$ to V_{CC}			2	μA
Output Leakage Current	I_{LO}	$\overline{CS} = V_{IH}$ or $WE = V_{IL}$ $V_{I/O} = V_{SS}$ to V_{CC}			2	μA
Operating Power Supply Current	I_{CC1}	$\overline{CS} = V_{IL}$, $V_{IN} = V_{IL}/V_{IH}$ $I_{OUT} = 0mA$			20	mA
Average Operating Current	I_{CC2}	Min Cycle, 100% Duty $\overline{CS} = V_{IL}$, $I_{OUT} = 0mA$			100	mA
Standby Power Supply Current	I_{SB}	$\overline{CS} = V_{IH}$			3	mA
	I_{SB1}	$\overline{CS} \geq V_{CC} - 0.2V$			2	mA
			L		100	μA
Output Low Voltage	V_{OL}	$I_{OL} = 8mA$			0.4	V
Output High Voltage	V_{OH}	$I_{OL} = -4mA$		2.4		V

CAPACITANCE (f = 1MHz, Ta = 25°C)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Input Capacitance	C_{IN}	$V_{IN} = 0V$	—	7	pF
Input/Output Capacitance	C_{OUT}	$V_{OUT} = 0V$	—	7	pF

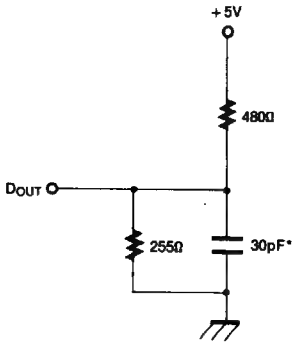
*Note: Capacitance is sampled and not 100% tested.

AC CHARACTERISTICS

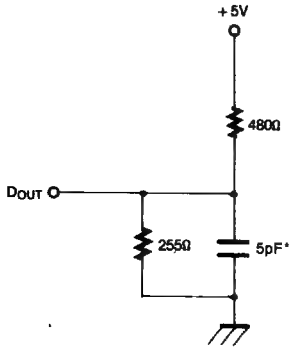
TEST CONDITIONS (Ta = 0 to 70°C, V_{CC} = 5V ± 10%, unless otherwise specified)

Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Time	5 ns
Input and Output Timing Reference Levels	1.5V
Output Load	See below

Output Load(a)



Output Load(b)
(for t_{HZ}, t_{LZ}, t_{WZ} & t_{OW})



*Including Scope and Jig Capacitance

READ CYCLE

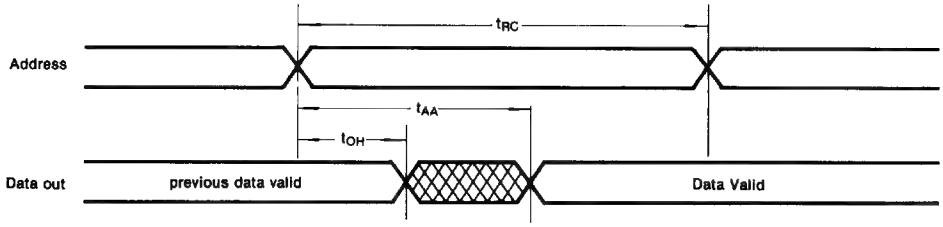
Parameter	Symbol	KM61257-25 KM61257L-25		KM61257-35 KM61257L-35		KM61257-45 KM61257L-45		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	25		35		45		ns
Address Access Time	t_{AA}		25		35		45	ns
Chip Select to Output	t_{ACS}		25		35		45	ns
Chip Enable to Low-Z Output	t_{LZ}	5		5		5		ns
Chip Disable to High-Z Output	t_{HZ}	0	15	0	15	0	20	ns
Output Hold from Address Change	t_{OH}	5		5		5		ns
Chip Selection to Power Up Time	t_{PU}	0		0		0		ns
Chip Desselection to Power Down Time	t_{PD}		25		35		45	ns

WRITE CYCLE

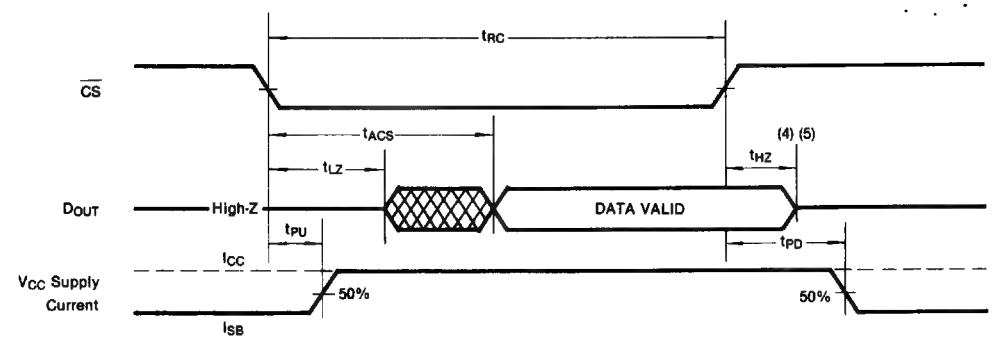
Parameter	Symbol	KM61257-25 KM61257L-25		KM61257-35 KM61257L-35		KM61257-45 KM61257L-45		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	25		30		40		ns
Chip Select to End of Write	t_{CW}	25		30		40		ns
Address Set-Up Time	t_{AS}	0		0		0		ns
Address Valid to End of Write	t_{AW}	25		30		40		ns
Write Pulse Width	t_{WP}	25		30		35		ns
Write Recovery Time	t_{WR}	0		0		0		ns
Write to Output High-Z	t_{WZ}	0	15	0	20	0	20	ns
Data to Write Time Overlap	t_{DW}	15		20		25		ns
Data Hold from Write Time	t_{DH}	0		0		0		ns
End Write to Output Low-Z	t_{OW}	5		5		5		ns

TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE (Address Controlled)



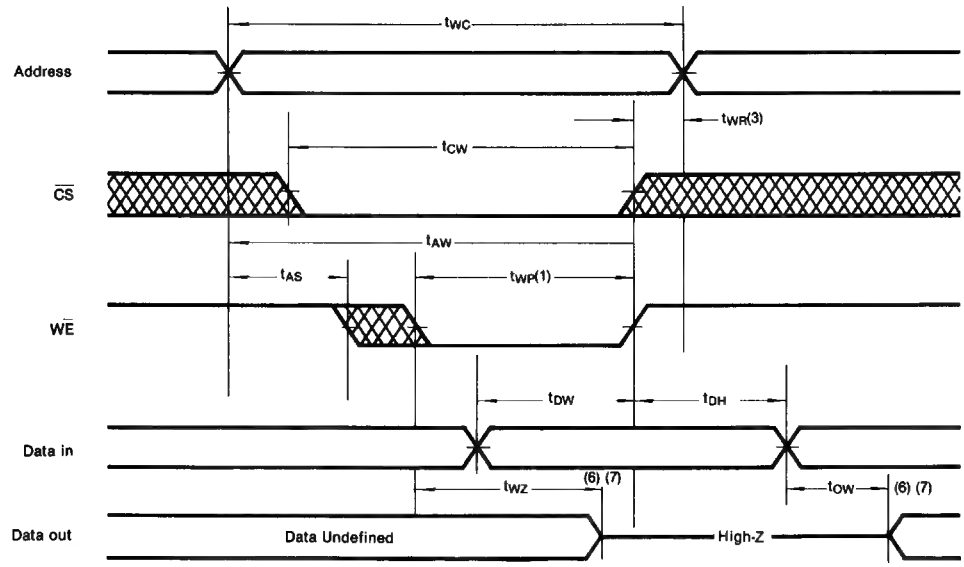
TIMING WAVEFORM OF READ CYCLE ($\overline{CS}$ Controlled)



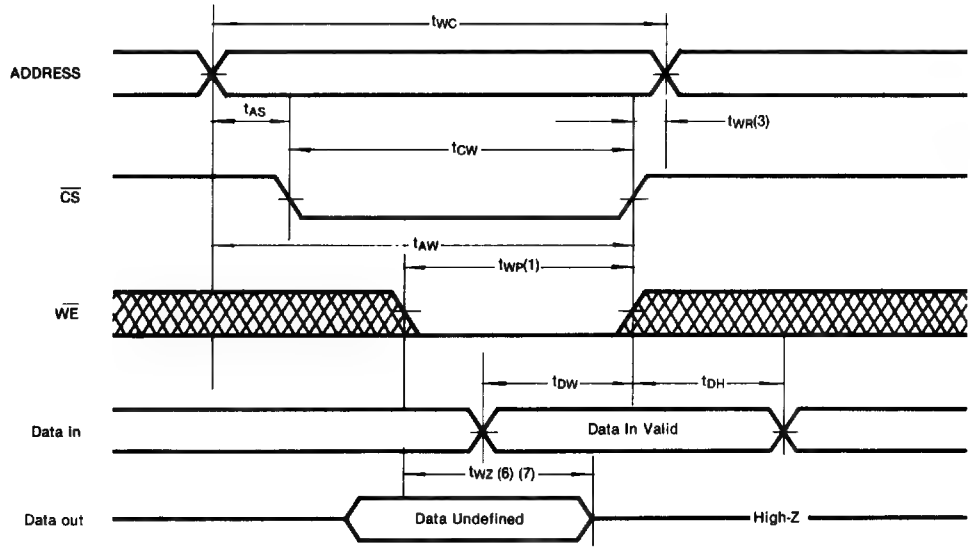
Note (READ CYCLE)

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. At any given temperature and voltage condition, t_{HZ}(max.) is less than t_{LZ}(min.) both for a given device and from device to device.
4. Transition is measured ±200mV from steady state voltage with Load(b).
5. This parameter is sampled and not 100% tested.
6. Device is continuosly selected with $\overline{CS} = V_{IL}$
7. Address valid prior to or coincident with $\overline{CS}$ transition low.

TIMING WAVEFORM OF WRITE CYCLE ($\overline{WE}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE ($\overline{CS}$ Controlled)



Note (WRITE CYCLE)

1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and low $\overline{WE}$.
2. All write cycle timing is referenced from the last valid address to the first transition address.
3. Transition is measured ±200mV from steady state voltage with Load(b).
4. This parameter is sampled and not 100% tested.
5. At any given temperature and voltage condition, t_{WZ}(max.) is less than t_{OW}(min.) both for a given device and from device to device.
6. $\overline{CS}$ or $\overline{WE}$ must be in high during address transition.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	D_{OUT} PIN	Supply Current	Mode
H	X	High-Z	I_{SB}, I_{SB1}	Not Select
L	H	D_{OUT}	I_{CC1}, I_{CC2}	Read
L	H	D_{IN}	I_{CC1}, I_{CC2}	Write

*Note: X means Don't Care

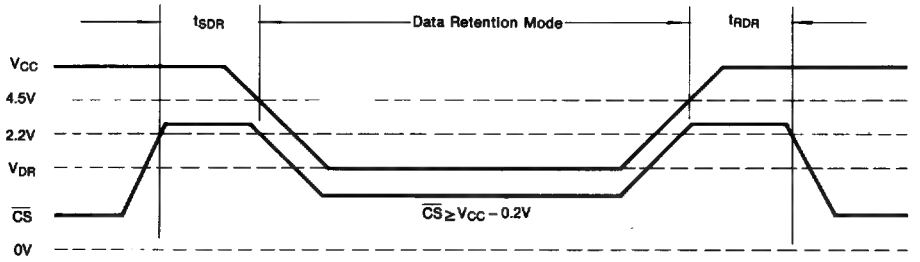
DATA RETENTION CHARACTERISTICS (Ta = 0 to 70°C)

(This characteristics is guaranteed only for L-version)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geq V_{CC} - 0.2V$	2.0		5.5	V
Data Retention Current	I_{DR}	$V_{CC} = 3V$ $\overline{CS} \geq V_{CC} - 0.2V$		1	50	μA
Data Retention Set-up Time	t_{SDR}	See Data Retention Waveforms (below)	0			nS
Recovery Time	t_{RDR}		t_{RC}*			nS

*t_{RC} = Read Cycle Time

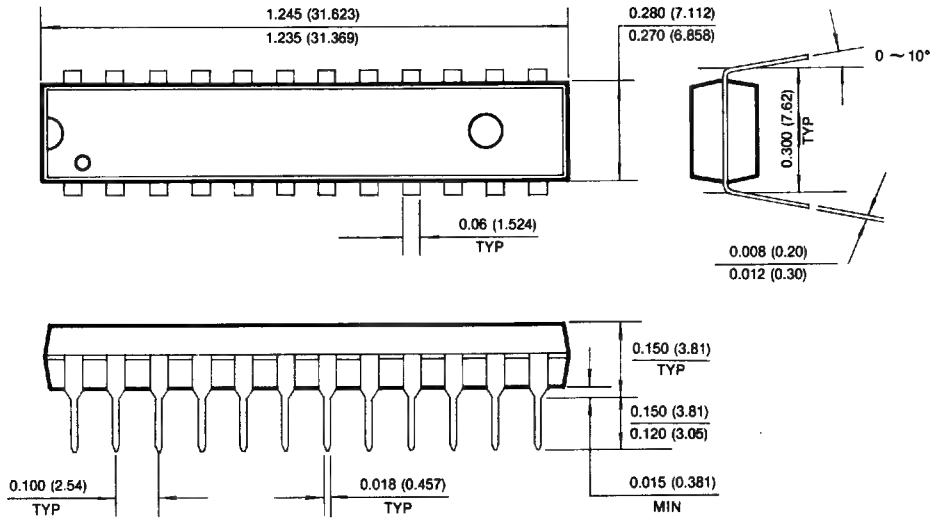
DATA RETENTION WAVEFORM



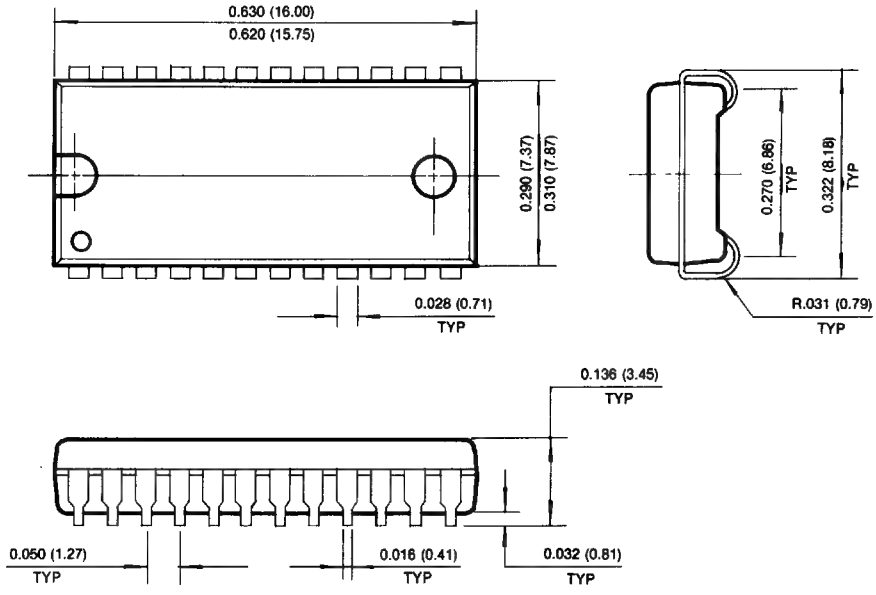
PACKAGE DIMENSIONS

24 LEAD PLASTIC DUAL IN LINE PACKAGE

Unit: Inches (millimeters)



24 PIN PLASTIC SMALL OUT LINE J FORM PACKAGE



64K × 4 Bit Static RAM

FEATURES

- **Fast Access Time 25,35,45ns(max.)**
- **Low Power Dissipation**
  - **Standby (TTL) : 3 mA (max.)**
  - **(CMOS): 100 μA (max.)**
  - **Operating : 120 mA (max.)**
- **Single 5V ± 10% Power Supply**
- **TTL compatible inputs and output**
- **Full Static Operation**
  - **— No clock or refresh required**
- **Tri-state Output**
- **Low Data Retention Current: 50 μA (max.)**
- **Battery Back-up Operation**
  - **— 2V (min.) Data Retention**
- **Standard 24-pin DIP (300mil) and 24-pin SOJ (300 mil)**

GENERAL DESCRIPTION

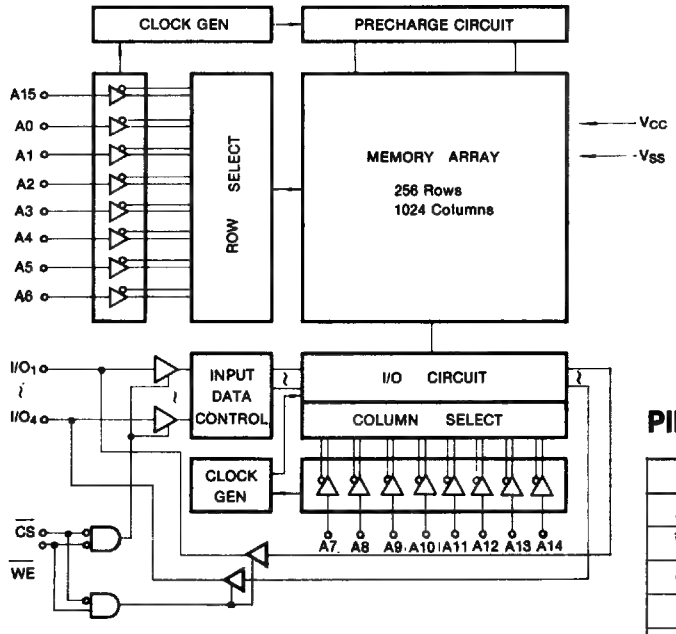
The KM64257 is a 262,144-bit high-speed Static Random Access Memory organized as 65,536 words by 4 bit.

The device is fabricated using Samsung's advanced CMOS process.

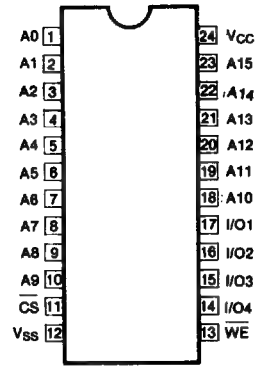
The KM64257 has a chip enable input for the minimum current power down mode.

The KM64257 has been designed for high speed applications. It is particularly well suited for the use in high speed and low power applications in which battery back-up for nonvolatility is required.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



PIN NAMES

Pin Name	Pin Function
A_0-A_{15}	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
I/O_1-I/O_4	Data Input/Outputs
V_{CC}	Power (+5V)
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	$V_{in, out}$	−0.5 to 7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−0.5 to 7.0	V
Power Dissipation	P_d	1.0	W
Storage Temperature	T_{stg}	−55 to +125	°C
Operating Temperature	T_a	0 to 70	°C

*Note: Stresses grater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS (Ta = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2		V_{CC} + 0.5	V
Input Low Voltage	V_{IL}*	−0.5		0.8	V

* V_{IL}(min) = −3.0V for <20ns pulse

DC AND OPERATING CHARACTERISTICS

(Ta = 0 to 70°C, V_{CC} = 5V ± 10%, unless otherwise specified)

Parameter	Symbol	Test Condition	Ver	Min	Max	Unit
Input Leakage Current	I_{LI}	$V_{IN} = V_{SS}$ to V_{CC}			2	μA
Output Leakage Current	I_{LO}	$\overline{CS} = V_{IH}$ or $\overline{WE} = V_{IL}$ $V_{I/O} = V_{SS}$ to V_{CC}			2	μA
Operating Power Supply Current	I_{CC1}	$\overline{CS} = V_{IL}$, $V_{IN} = V_{IL}/V_{IH}$ I_{OUT} = 0mA			20	mA
Average Operating Current	I_{CC2}	Min Cycle, 100% Duty $\overline{CS} = V_{IL}$, I_{OUT} = 0mA			120	mA
Standby Power Supply Current	I_{SB}	$\overline{CS} = V_{IH}$			3	mA
	I_{SB1}	$\overline{CS} \geq V_{CC} - 0.2V$			2	mA
			L		100	μA
Output Low Voltage	V_{OL}	I_{OL} = 8mA			0.4	V
Output High Voltage	V_{OH}	I_{OL} = −4mA		2.4		V

CAPACITANCE (f = 1MHz, Ta = 25°C)

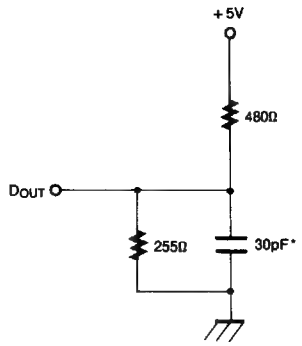
Parameter	Symbol	Test Conditions	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN} = 0V	—	7	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	—	7	pF

*Note: Capacitance is sampled and not 100% tested.

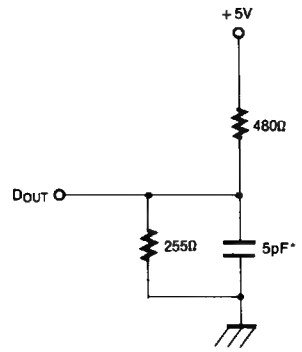
TEST CONDITIONS (Ta = 0 to 70°C, V_{CC} = 5V ± 10%, unless otherwise specified)

Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Time	5 ns
Input and Output Timing Reference Levels	1.5V
Output Load	See below

Output Load(a)



Output Load(b)
(for t_{HZ}, t_{LZ}, t_{WZ} & t_{OW})



*Including Scope and Jig Capacitance

READ CYCLE

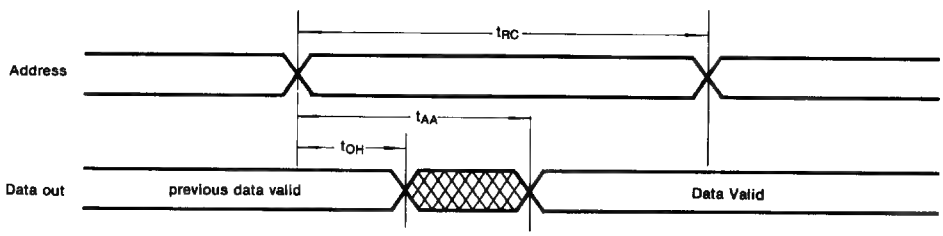
Parameter	Symbol	KM64257-25 KM64257L-25		KM64257-35 KM64257L-35		KM64257-45 KM64257L-45		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	25		35		45		ns
Address Access Time	t_{AA}		25		35		45	ns
Chip Select to Output	t_{ACS}		25		35		45	ns
Chip Enable to Low-Z Output	t_{LZ}	5		5		5		ns
Chip Disable to High-Z Output	t_{HZ}	0	15	0	15	0	20	ns
Output Hold from Address Change	t_{OH}	5		5		5		ns
Chip Selection to Power Up Time	t_{PU}	0		0		0		ns
Chip Desselection to Power Down Time	t_{PD}		20		30		30	ns

WRITE CYCLE

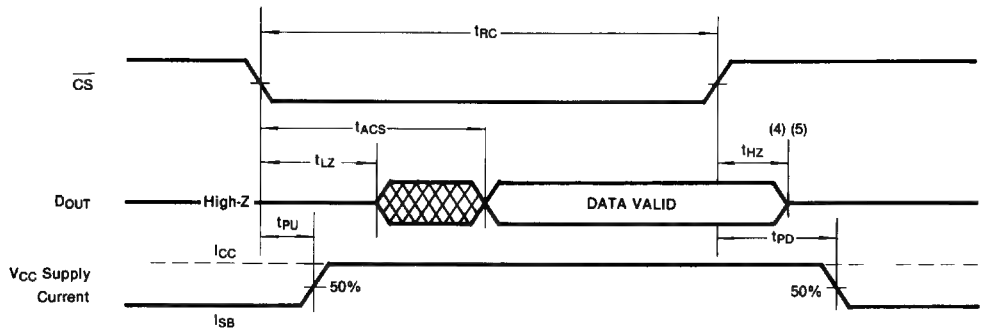
Parameter	Symbol	KM64257-25 KM64257L-25		KM64257-35 KM64257L-35		KM64257-45 KM64257L-45		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	25		30		40		ns
Chip Select to End of Write	t_{CW}	25		30		40		ns
Address Set-Up Time	t_{AS}	0		0		0		ns
Address Valid to End of Write	t_{AW}	25		30		40		ns
Write Pulse Width	t_{WP}	25		30		35		ns
Write Recovery Time	t_{WR}	0		0		0		ns
Write to Output High-Z	t_{WZ}	0	8	0	10	0	15	ns
Data to Write Time Overlap	t_{DW}	17		20		20		ns
Data Hold from Write Time	t_{DH}	0		0		0		ns
End Write to Output Low-Z	t_{OW}	5		5		5		ns

TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE (Address Controlled)



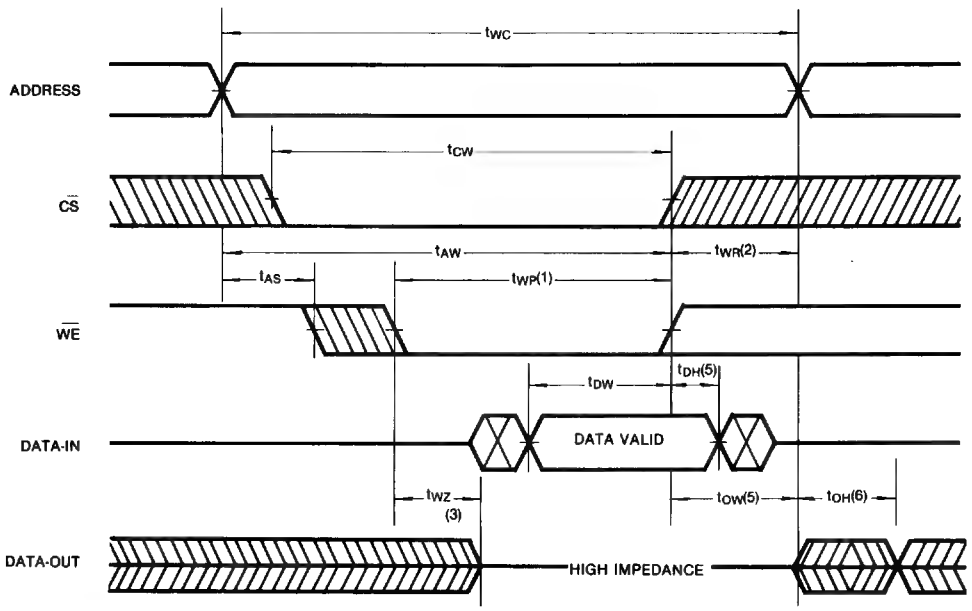
TIMING WAVEFORM OF READ CYCLE ($\overline{CS}$ Controlled)



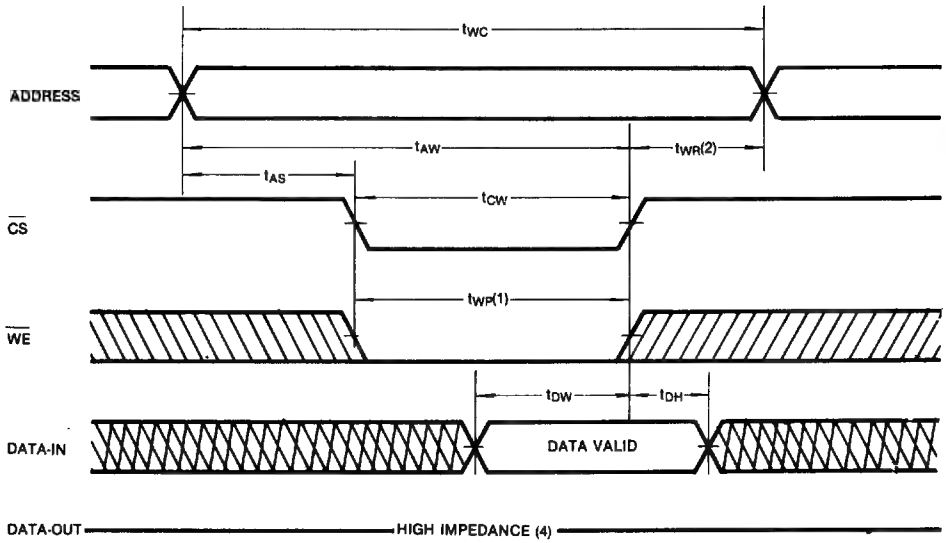
Note (READ CYCLE)

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. At any given temperature and voltage condition, t_{HZ}(max.) is less than t_{LZ}(min.) both for a given device and from device to device.
4. Transition is measured ±200mV from steady state voltage with Load(b).
5. This parameter is sampled and not 100% tested.
6. Device is continuosly selected with $\overline{CS} = V_{IL}$
7. Address valid prior to or coincident with $\overline{CS}$ transition low.

TIMING WAVEFORM OF WRITE CYCLE ($\overline{WE}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE ($\overline{CS}$ Controlled)



Note (WRITE CYCLE)

1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$. (t_{WP}).
2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
4. If the $\overline{CS}$ low transition occurs simuluaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, the output buffers remain in a high impedance state.
5. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then the data Input signals of opposite phase to the outputs must not be applied to them.
6. D_{OUT} is the same phase of write data of this write cycle, if t_{WR} is long enough.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	I/O PIN	Supply Current	Mode
H	X	High-Z	I_{SB}, I_{SB1}	Not Select
L	H	D_{OUT}	I_{CC1}, I_{CC2}	Read
L	L	D_{IN}	I_{CC1}, I_{CC2}	Write

*Note: X means Don't Care

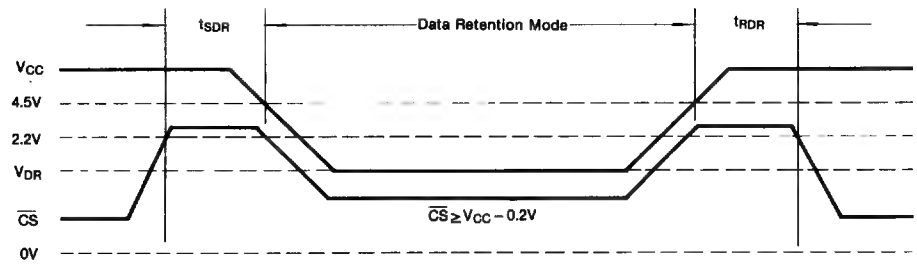
DATA RETENTION CHARACTERISTICS (Ta = 0 to 70°C)

(This characteristics is guaranteed only for L-version)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geq V_{CC} - 0.2V$	2.0		5.5	V
Data Retention Current	I_{DR}	$V_{CC} = 3V$ $\overline{CS} \geq V_{CC} - 0.2V$		1	50	μA
Data Retention Set-up Time	t_{SDR}	See Data Retention Waveforms (below)	0			nS
Recovery Time	t_{RDR}		t_{RC}*			nS

*t_{RC} = Read Cycle Time

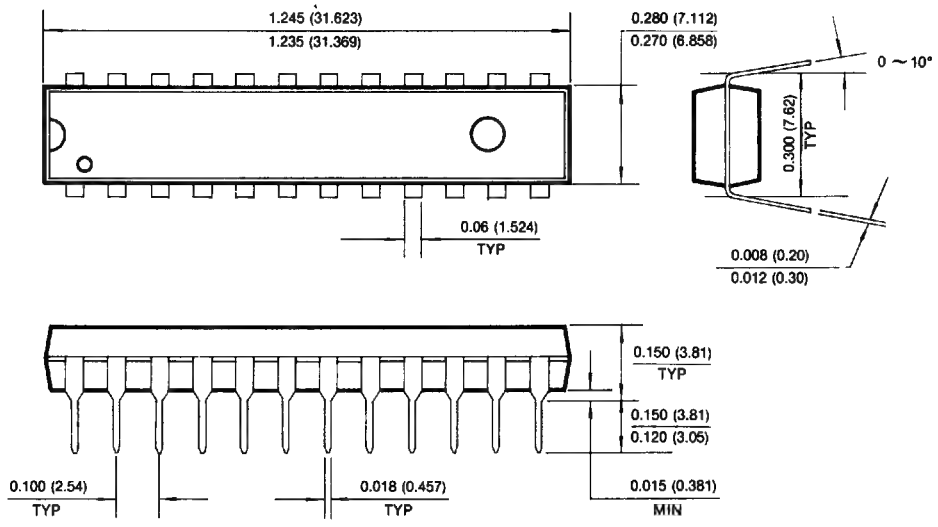
DATA RETENTION WAVEFORM



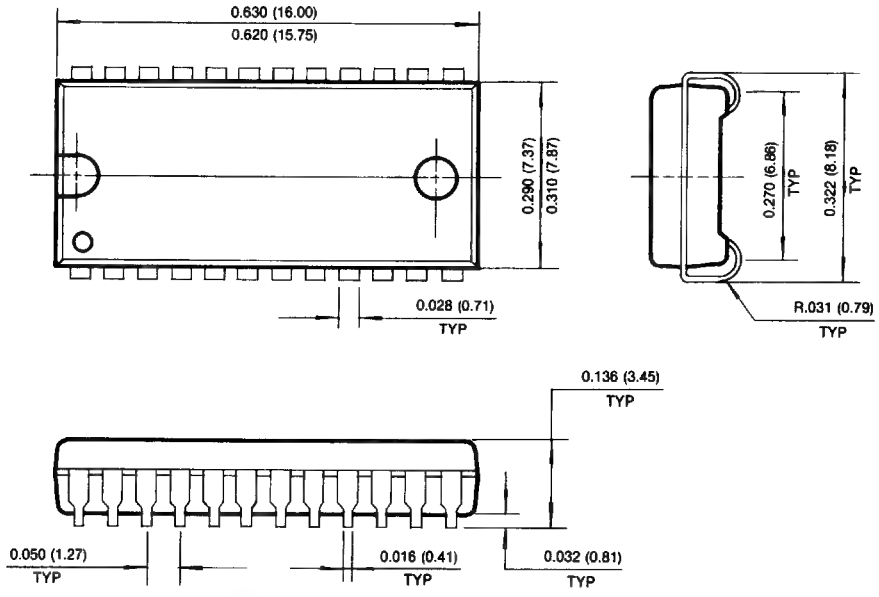
PACKAGE DIMENSIONS

24 LEAD PLASTIC DUAL IN LINE PACKAGE

Unit: Inches (millimeters)



24 PIN PLASTIC SMALL OUT LINE J FORM PACKAGE



32K × 8 Bit Static RAM

FEATURES

- **Fast Access Time 35,45,55ns(max.)**
- **Low Power Dissipation**
  - **Standby (TTL) : 3 mA (max.)**
  - **(CMOS): 100 μA (max.)**
  - **Operating : 120 mA (max.)**
- **Single 5V ± 10% Power Supply**
- **TTL compatible inputs and output**
- **Full Static Operation**
  - **— No clock or refresh required**
- **Tri-state Output**
- **Low Data Retention Current: 50 μA (max.)**
- **Battery Back-up Operation**
  - **— 2V (min.) Data Retention**
- **Standard 28-pin DIP (600mil)**

GENERAL DESCRIPTION

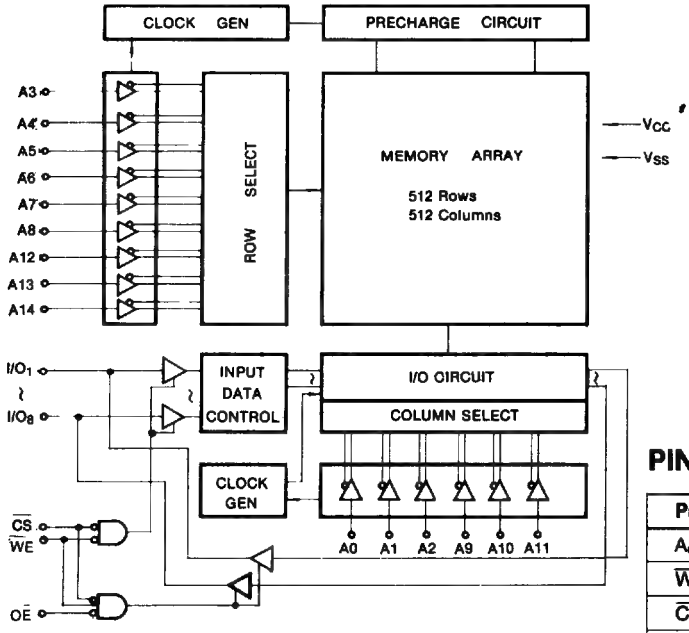
The KM68257 is a 262,144-bit high-speed Static Random Access Memory organized as 32,768 words by 8 bit.

The device is fabricated using Samsung's advanced CMOS process.

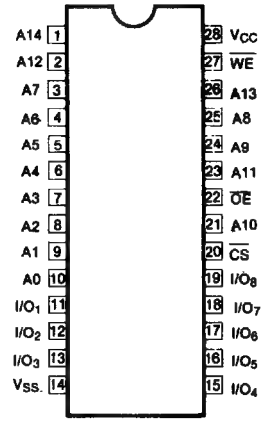
The KM68257 has an output enable input for precise control of the data outputs. It also has a chip enable input for the minimum current power down mode.

The KM68257 has been designed for high speed applications. It is particularly well suited for the use in high speed and low power applications in which battery back-up for nonvolatility is required.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



PIN NAMES

Pin Name	Pin Function
A_0-A_{14}	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Select
I/O_1-I/O_8	Data Input/Outputs
V_{CC}	Power (+5V)
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	$V_{in, out}$	−0.5 to 7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−0.5 to 7.0	V
Power Dissipation	P_d	1.0	W
Storage Temperature	T_{stg}	−55 to +125	°C
Operating Temperature	T_a	0 to 70	°C

*Note: Stresses grater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS (T_a = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2		V_{CC} + 0.3	V
Input Low Voltage	V_{IL}*	−0.5		0.8	V

* V_{IL}(min) = −3.0V for <20ns pulse

DC AND OPERATING CHARACTERISTICS

(T_a = 0 to 70°C, V_{CC} = 5V ± 10%, unless otherwise specified)

Parameter	Symbol	Test Condition	Ver	Min	Max	Unit
Input Leakage Current	I_{LI}	$V_{IN} = V_{SS}$ to V_{CC}		−2	2	μA
Output Leakage Current	I_{LO}	$\overline{CS} = V_{IH}$ or $\overline{WE} = V_{IL}$ $V_{I/O} = V_{SS}$ to V_{CC}		−2	2	μA
Operating Power Supply Current	I_{CC1}	$\overline{CS} = V_{IL}$, $V_{IN} = V_{IL}/V_{IH}$ I_{OUT} = 0mA			30	mA
Average Operating Current	I_{CC2}	Min Cycle, 100% Duty $\overline{CS} = V_{IL}$, I_{OUT} = 0mA			120	mA
Standby Power Supply Current	I_{SB}	$\overline{CS} = V_{IH}$			3	mA
	I_{SB1}	$\overline{CS} \geq V_{CC} - 0.2V$	P		1	mA
			LP		100	μA
Output Low Voltage	V_{OL}	I_{OL} = 8mA			0.4	V
Output High Voltage	V_{OH}	I_{OL} = −4mA		2.4		V

CAPACITANCE (f = 1MHz, T_a = 25°C)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN} = 0V	—	8	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	—	8	pF

*Note: Capacitance is sampled and not 100% tested.

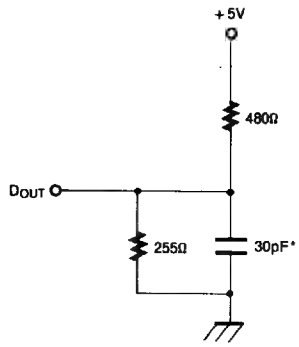
AC CHARACTERISTICS

(Ta = 0 to 70°C, V_{CC} = 5V ± 10%, unless otherwise specified)

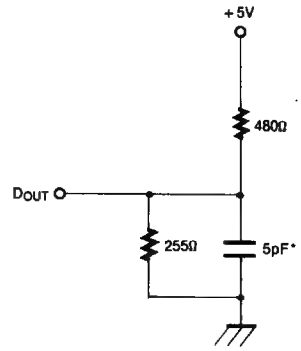
TEST CONDITIONS (Ta = 0 to 70°C, V_{CC} = 5V ± 10%, unless otherwise specified)

Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Time	5 ns
Input and Output Timing Reference Levels	1.5V
Output Load	See below

Output Load(a)



Output Load(b)
(for t_{HZ}, t_{LZ}, t_{WZ} & t_{OW})



*Including Scope and Jig Capacitance

READ CYCLE

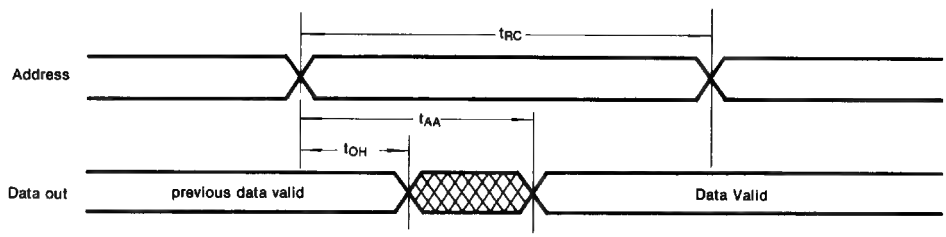
Parameter	Symbol	KM68257P-35 KM68257LP-35		KM68257P-45 KM68257LP-45		KM68257P-55 KM68257LP-55		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	35		45		55		ns
Address Access Time	t_{AA}		35		45		55	ns
Chip Select to Output	t_{ACS}		35		45		55	ns
Output Enable to Output	t_{OE}		15		20		25	ns
Output Enable to Low-Z Output	t_{OLZ}	0		0		0		ns
Chip Enable to Low-Z Output	t_{LZ}	5		10		10		ns
Output Disable to High-Z Output	t_{OHZ}	0	15	0	15	0	20	ns
Chip Disable to High-Z Output	t_{HZ}	0	15	0	15	0	20	ns
Output Hold from Address Change	t_{OH}	5		5		5		ns
Chip Selection to Power Up Time	t_{PU}	0		0		0		ns
Chip Deselection to Power Down Time	t_{PD}		30		35		40	ns

WRITE CYCLE

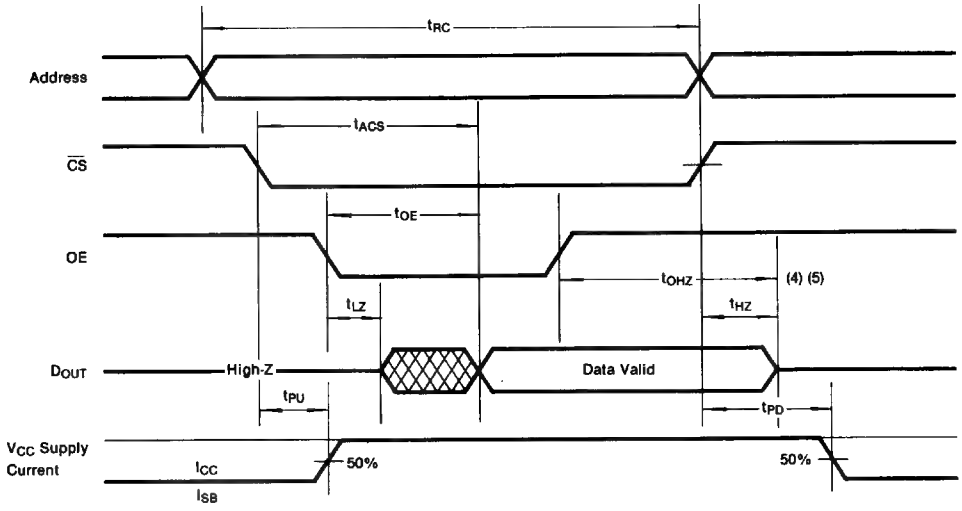
Parameter	Symbol	KM68257P-25 KM68257LP-25		KM68257P-35 KM68257LP-35		KM68257P-45 KM68257LP-45		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	35		45		55		ns
Chip Select to End of Write	t_{CW}	35		40		45		ns
Address Set-Up Time	t_{AS}	0		0		0		ns
Address Valid to End of Write	t_{AW}	30		35		40		ns
Write Pulse Width	t_{WP}	30		35		40		ns
Write Recovery Time	t_{WR}	0		0		0		ns
Write to Output High-Z	t_{WZ}	0	15	0	15	0	20	ns
Data to Write Time Overlap	t_{DW}	20		25		30		ns
Data Hold from Write Time	t_{DH}	0		0		0		ns
End Write to Output Low-Z	t_{OW}	5		5		5		ns

TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE NO: 1



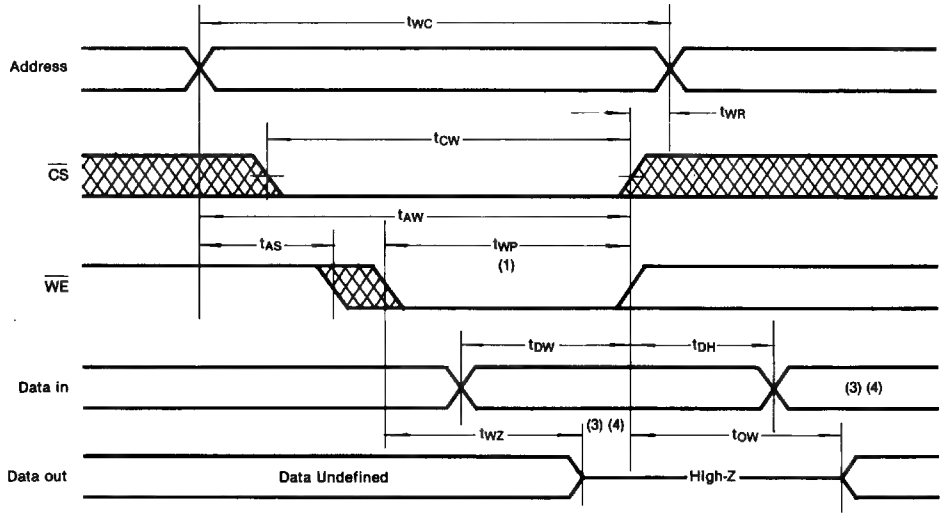
TIMING WAVEFORM OF READ CYCLE NO: 2



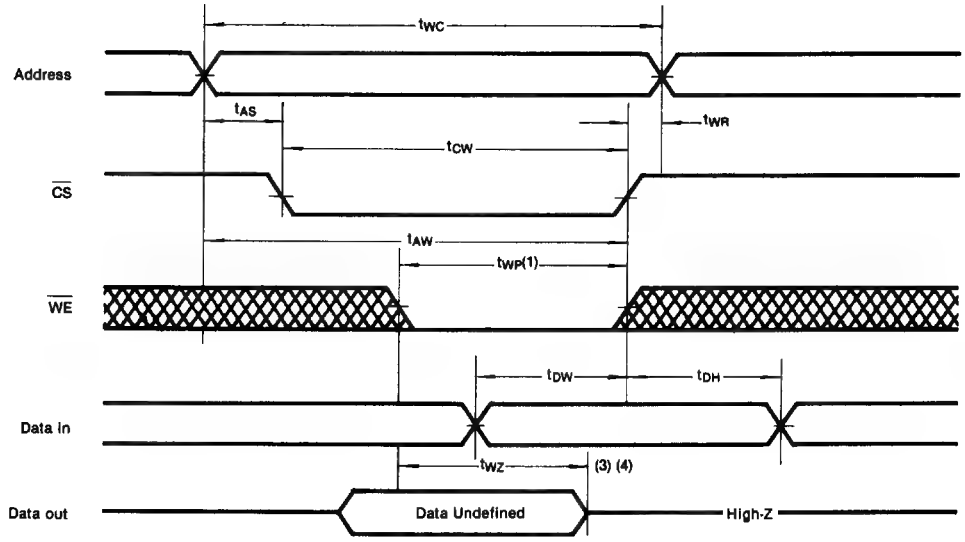
Note (READ CYCLE)

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. At any given temperature and voltage condition, t_{HZ}(max.) is less than t_{LZ}(min.) both for a given device and from device to device.
4. Transition is measured ±200mV from steady state voltage with Load(b).
5. This parameter is sampled and not 100% tested.
6. Device is continuosly selected with $\overline{CS} = V_{IL}$
7. Address valid prior to or coincident with $\overline{CS}$ transition low.

TIMING WAVEFORM OF WRITE CYCLE ($\overline{WE}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE ($\overline{WE}$ Controlled)



Note (WRITE CYCLE)

1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and low $\overline{WE}$.
2. All write cycle timing is referenced from the last valid address to the first transition address.
3. Transition is measured ±500mV from steady state voltage with Load(b).
4. This parameter is sampled and not 100% tested.
5. At any given temperature and voltage condition, t_{WZ}(max.) is less than t_{OW}(min.) both for a given device and from device to device.
6. $\overline{CS}$ or $\overline{WE}$ must be in high during address transition.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	I/O PIN	Supply Current	Mode
H	X	X	High-Z	I_{SB}, I_{SB1}	Standby Mode
L	H	H	High-Z	I_{CC1}, I_{CC2}	Output Disable
L	H	L	D_{OUT}	I_{CC1}, I_{CC2}	Read
L	L	L	D_{IN}	I_{CC1}, I_{CC2}	Write

*Note: X means Don't Care

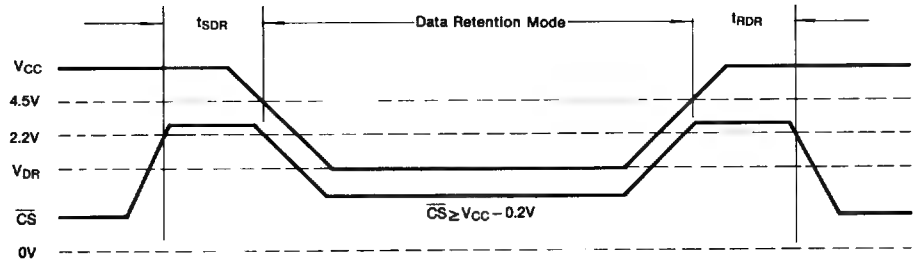
DATA RETENTION CHARACTERISTICS (Ta = 0 to 70°C)

(This characteristics is guaranteed only for L-version)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geq V_{CC} - 0.2V$	2.0		5.5	V
Data Retention Current	I_{DR}	$V_{CC} = 3V$ $\overline{CS} \geq V_{CC} - 0.2V$		1	50	μA
Data Retention Set-up Time	t_{SDR}	See Data Retention Waveforms (below)	0			nS
Recovery Time	t_{RDR}		t_{RC}*			nS

*t_{RC} = Read Cycle Time

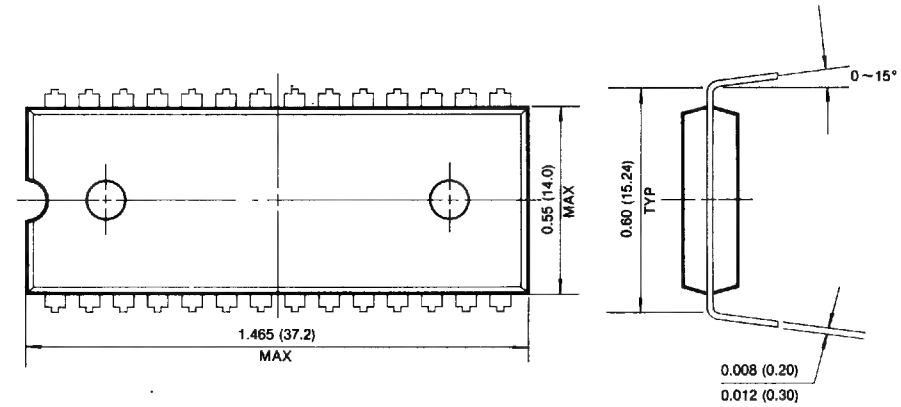
DATA RETENTION WAVEFORM

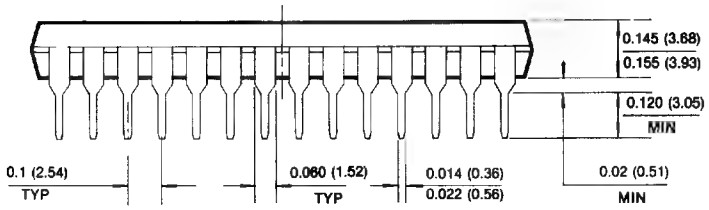


PACKAGE DIMENSIONS

28 LEAD PLASTIC DUAL IN LINE PACKAGE

Units: Inches (millimeters)





128K x 8 Bit Static RAM

FEATURES

- **Fast Access Time 70, 80, 100, 120ns (max.)**
- **Low Power Dissipation**
  - **Standby (TTL) : 3 mA (max.)**
  - **(CMOS): 100 μA (max.)**
  - **Operating : 100 mA (max.)**
- **Single 5V ± 10% Power Supply**
- **TTL compatible inputs and output**
- **Full Static Operation**
  - **— No clock or refresh required**
- **Tri-state Output**
- **Low Data Retention Current: 50 μA (max.)**
- **Battery Back-up Operation**
  - **— 2V (min.) Data Retention**
- **Standard 32-pin DIP (600mil) and 32-pin SOP (450mil)**

GENERAL DESCRIPTION

The KM681000/L is a 1,048,576-bit high-speed Static Random Access Memory organized as 131,072 words by 8 bit.

The device is fabricated using Samsung's advanced CMOS process.

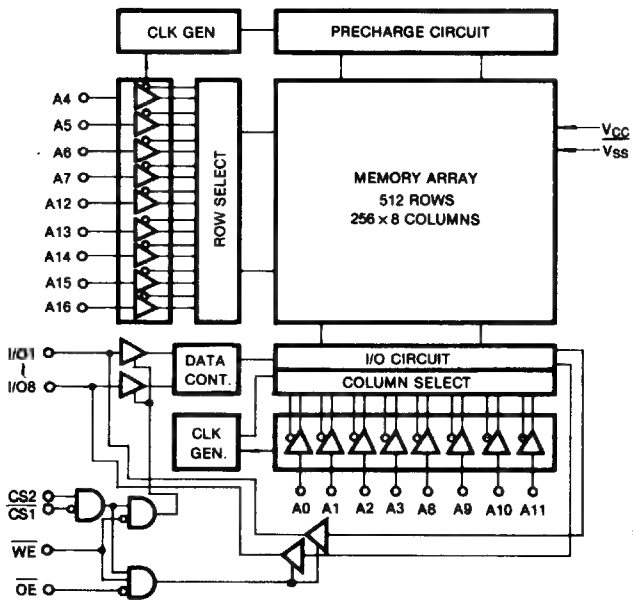
The KM681000/L has an output enable input for precise control of the data outputs.

It also has a chip enable inputs for the minimum current power down mode.

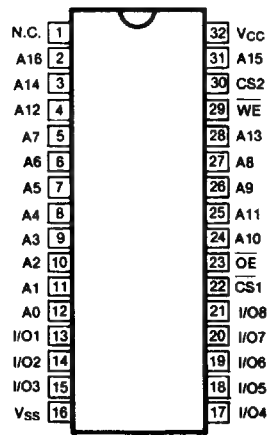
The KM681000/L has been designed for high speed and low power applications.

It is particularly well suited for battery back-up nonvolatile memory application.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



PIN NAMES

Pin Name	Pin Function
A_0-A_{16}	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS1}$, CS2	Chip Select
$\overline{OE}$	Output Enable
I/O_1-I/O_8	Data Inputs/Outputs
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

EEPROM DATA SHEETS 4

1. KM93C06
2. KM93C07
3. KM93C46
4. KM28C16/KM28C17
5. KM28C64/KM28C65
6. KM28C256

EEPROM

Capacity	Part Number	Organization	Speed (ns)	Technology	Write Cycle Time (ms)	Features	Packages	Remarks
256 bit	†KM93C06	16 × 16	250KHz	CMOS	10	Ext.-timed	8 DIP	Now
	†KM93C07	16 × 16	250KHz	CMOS	10	Self-timed	8 DIP	Now
1K bit	†KM93C46	64 × 16	250KHz	CMOS	10	Self-timed	8 DIP/8 SOIC	Now
	†KM93C46I	64 × 16	250KHz	CMOS	10	Industrial	8 DIP	Now
16K bit	KM28C16	2K × 8	150/200/250	CMOS	2	$\overline{D}$-P, 32 page mode	24 DIP/32 PLCC	Now
	†KM28C16I	2K × 8	150/200/250	CMOS	2	Industrial	24 DIP	Now
	KM28C17	2K × 8	150/200/250	CMOS	2	$\overline{D}$-P, R/$\overline{B}$	28 DIP/32 PLCC	Now
	†KM28C17I	2K × 8	150/200/250	CMOS	2	Industrial	28 DIP	Now
64K bit	KM28C64	8K × 8	200/250	CMOS	5	$\overline{D}$-P, 32 page mode	28 DIP/32 PLCC	Now
	†KM28C64I	8K × 8	200/250	CMOS	5	Industrial	28 DIP	Now
	KM28C65	8K × 8	200/250	CMOS	5	$\overline{D}$-P, R/$\overline{B}$	28 DIP/32 PLCC	Now
	†KM28C65I	8K × 8	200/250	CMOS	5	Industrial	28 DIP	Now
256K bit	†KM28C256	32K × 8	150/200/250	CMOS	5	$\overline{D}$-P, T-B, 64 page mode	28 DIP/32 PLCC	6, '89
	†KM28C256I	32K × 8	150/200/250	CMOS	5	Industrial	28 DIP	6, '89

* $\overline{D}$-P: $\overline{Data}$-Polling, R/$\overline{B}$: Ready/$\overline{Busy}$, T-B: Toggle Bit
† New Product

256-Bit Serial Electrically Erasable PROM

FEATURES

- **16 x 16 serial read/write memory**
- **High performance advanced CMOS technology**
  - **Reliable floating gate technology**
- **Single 5 Volt supply**
- **Low power dissipation**
  - **Standby current: 250μA (TTL)**
  - **Active current: 5 mA (TTL)**
- **TTL compatible**
- **Enhanced write protection**

GENERAL DESCRIPTION

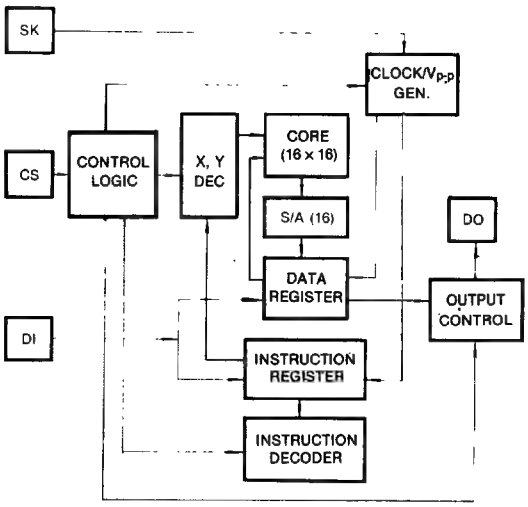
The KM93C06 is a CMOS 5V Only 256 bit non-volatile, sequential EEPROM. It is fabricated with the well defined floating gate CMOS technology using Folwer-Nordheim tunneling for erasing and programming.

The KM93C06 is organized as 16 registers of 16 bits each, which can be read/written serially by a microprocessor.

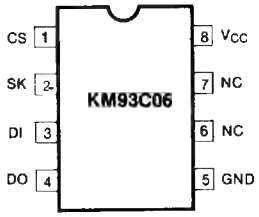
The KM93C06 is designed for applications up to 10,000 erase/write cycles per byte and over 10 years of data retention.

4

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



PIN NAMES

Pin Name	Pin Function
CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
N.C.	No Connection
V_{CC}	Power Supply
GND	Ground

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}	−0.3 to 7.0	V
Temperature Under Bias	T_{bias}	−10 to +85	°C
Storage Temperature	T_{stg}	−65 to +125	°C

*Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of the data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V
Input High Voltage, all inputs	V_{IH}	2.0	–	V_{CC} + 0.3	V
Input Low Voltage, all inputs	V_{IL}	−0.3	—	0.8	V

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Operating Voltage	V_{CC}		4.5	5.5	V
Operating Current (DC)	I_{CC1}	V_{CC} = 5.5V, CS = 2.0V, SK = 2.0V		1	mA
Operating Current (AC)	I_{CC2}	V_{CC} = 5.5V, f_{sk} = 250KHz		5	mA
Standby Current (TTL)	I_{SB1}	V_{CC} = 5.5V, CS = 0.8V		250	μA
Standby Current (CMOS)	I_{SB2}	V_{CC} = 5.5V, CS = 0V		100	μA
Input Voltage Levels	V_{IL} V_{IH}		−0.3 2.0	0.8 V_{CC} + 0.3	V V
Output Voltage Levels	V_{OL} V_{OH}	I_{OL} = 2.1mA I_{OH} = −400μA	 2.4	0.4	V V
Input Leakage Current	I_{LI}	V_{IN} = 5.5V		10	μA
Output Leakage Current	I_{LO}	V_{OUT} = 5.5V, CS = 0V		10	μA

INSTRUCTION SET FOR MODE SELECTION

Instruction	SB	OP Code	Address	Data	Comment
READ	1	10XX	A3A2A1A0	D_{OUT}	Read register A3A2A1A0
WRITE	1	01XX	A3A2A1A0	D15-D0	Write register A3A2A1A0
ERASE	1	11XX	A3A2A1A0	—	Erase register A3A2A1A0
EWEN	1	0011	xxxx	—	Erase/Write enable
EWDS	1	0000	xxxx	—	Erase/Write disable
ERAL	1	0010	xxxx	—	Erase all registers
WRAL	1	0001	xxxx	D15-D0	Write all registers

The KM93C06 provides 7 instructions as shown. Note that all the instructions start with a logic "1" start bit, and the next 8 bits carry the 4-bit OP code and the 4-bit address for 1 of 16, 16-bit register.

AC TEST CONDITIONS

Parameter	Value
Input Pulse Levels	0.45 to 2.4V
Input Rise and Fall Times	20 ns
Input and Output Timing Levels	0.8V and 2.0V
Output Load	1 TTL Gate and $C_L = 100pF$

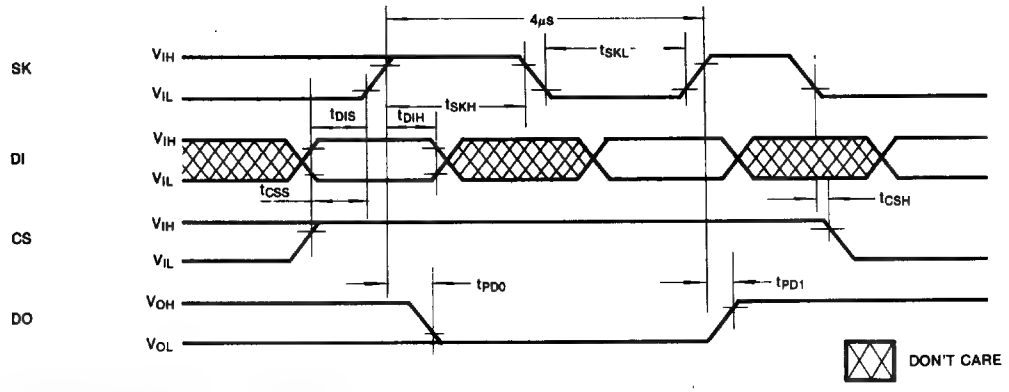
AC OPERATING CHARACTERISTICS ($T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise noted.)

Parameter	Symbol	Test Conditions	Min	Max	Unit
SK Frequency			0	250	KHz
SK High Time	t_{SKH}		1		μs
SK Low Time	t_{SKL}		1		μs
Chip Select Setup Time	t_{CSS}		0.2		μs
Chip Select Hold Time	t_{CSH}		0		μs
Data Setup Time	t_{DIS}		0.4		μs
Data Hold Time	t_{DIH}		0.4		μs
Output High Delay Time	t_{PD1}	$V_{OL} = 0.8V$, $V_{OH} = 2.0V$ $V_{IL} = 0.45V$, $V_{IH} = 2.4V$		2	μs
Output Low Delay Time	t_{PD0}			2	μs
Program Cycle Time	$t_{E/W}$		10	30	ms
Rising Edge of CS to Status Valid	t_{SV}			1	μs
Falling Edge of CS to D_{OUT} TRI-STATE	t_{0H}, t_{1H}			0.4	μA

Note 1: The SK frequency spec, specifies a minimum SK clock period of 4μs, therefore in a SK clock cycle $t_{SKH} + t_{SKL}$ must be greater than or equal to 4μs.
e.q., if $t_{SKL} = 1\mu s$ then the minimum $t_{SKH} = 3\mu s$ in order to meet the SK frequency specification.
Note 2: CS must be brought low for a minimum $1\mu s(t_{CS})$ between consecutive instruction cycles.

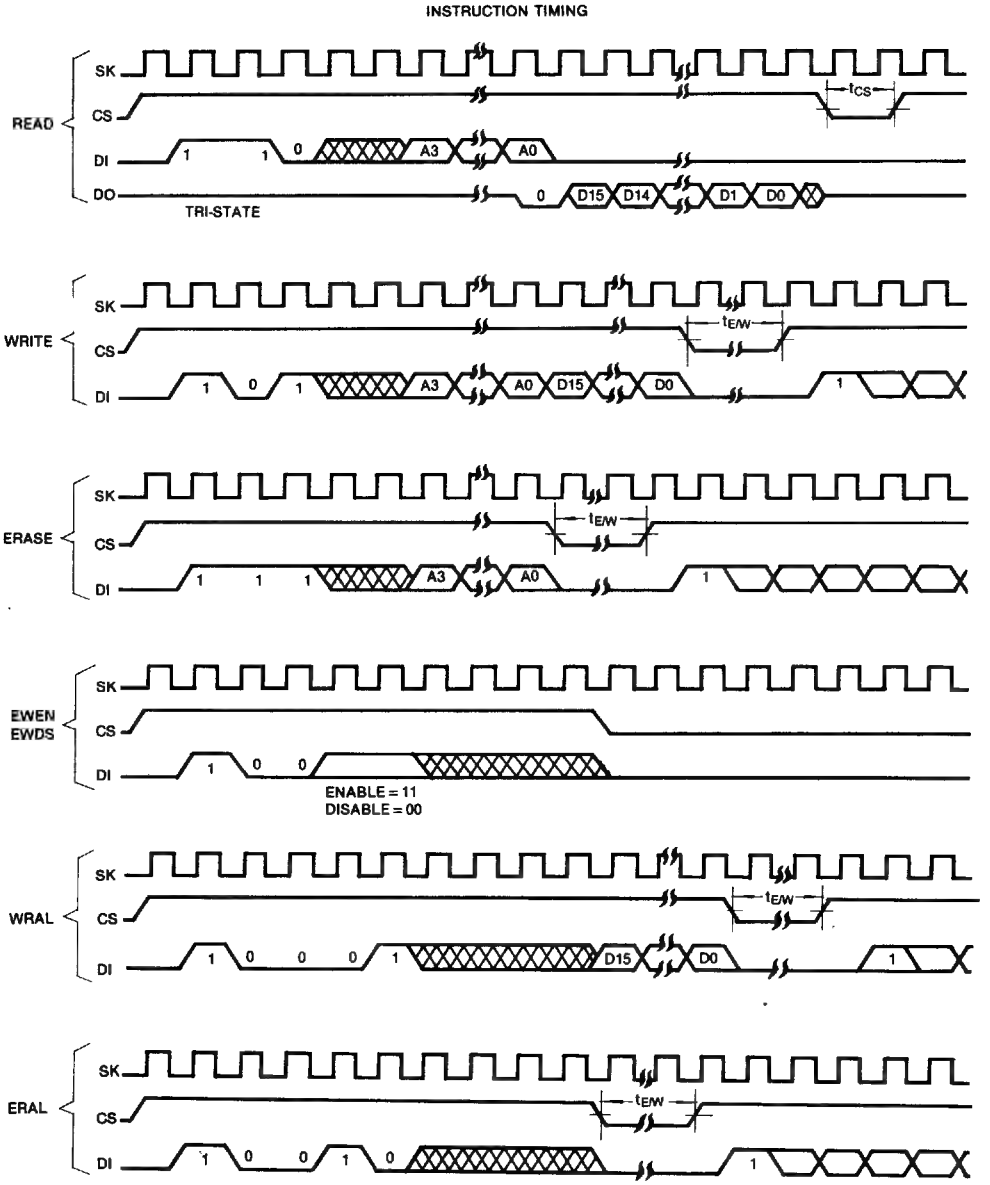
TIMING DIAGRAMS

SYNCHRONOUS DATA TIMING



TIMING DIAGRAMS (Continued)

INSTRUCTION TIMING



DEVICE OPERATION

The KM93C06 is 256 bit CMOS serial I/O EEPROM used with microcontrollers for nonvolatile memory applications. The on-chip programming voltage generator allows user to use a single 5V power supply. All the operation of the chip is proceeded by an instruction set, consisted of a start bit and four OP code bits, facilitating inherent protection against false write. The DO pin is in tri-state except for the read period to eliminate bus contention.

READ

After a read instruction and address set is received, low to high transition of the SK clock produces output data at DO pin. A dummy bit (logical "0") proceeds the 16 bit data output string.

EWEN / EWDS

The KM93C06 is at the erase/write disable (EWDS) state during power-up period to protect against accidental disturb. After the power up period, the erase/write operation must be proceeded by an erase/write enable (EWEN) operation. The erase/write enable (EWEN) mode is maintained until a erase/write disable (EWDS) operation is executed or V_{CC} is removed from the part. Execution of READ operation is independent of both EWEN and EWDS instructions.

ERASE

Before a write cycle, an erase cycle need to be operated to reset the EEPROM cells to the "erase" state. The chip starts an erase cycle by dropping CS low after an erase instruction and address set is input. The erase cycle is ended by raising CS input high after the program cycle time ($t_{E/W}$) is satisfied.

WRITE

The write operation is started by sequentially loading its instruction, address, and data set. After the last bit of data is input on the DI pin, CS must be brought low before the rising edge of the SK clock. This falling edge of CS initiates the write cycle. Like the erase operation, write cycle ended at the rising edge of CS input.

ERAL (chip erase)

Entire memory array is erased, i.e., logical "1" state, by this chip erase (ERAL) operation. The chip erase cycle is identical to the erase cycle except for different OP code.

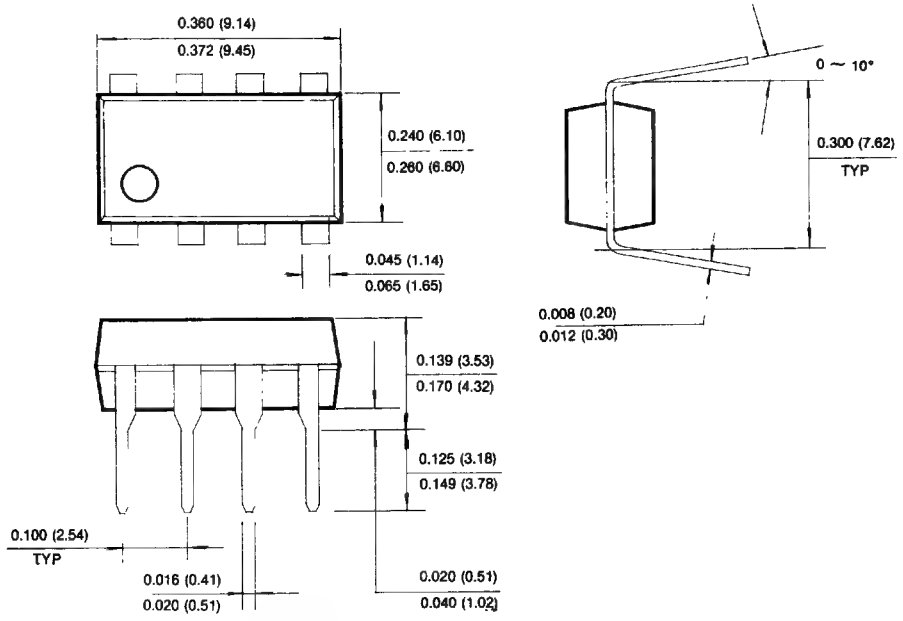
WRAL (chip write)

The entire array need to be erased before this chip write mode operation. Data given during this mode are written to all cells in the corresponding column simultaneously.

PACKAGE DIMENSIONS

8 PIN PLASTIC DUAL IN LINE PACKAGE

unit; inches (millimeters)



256-Bit Serial Electrically Erasable PROM

FEATURES

- **16 x 16 serial read/write memory**
- **High performance advanced CMOS technology**
  - **Reliable floating gate technology**
- **Single 5 Volt supply**
- **Low power dissipation**
  - **Standby current: 250μA (TTL)**
  - **Active current: 5 mA (TTL)**
- **TTL compatible**
- **Enhanced write protection**
- **Self-timed programming cycle**
- **Device status signal during programming**

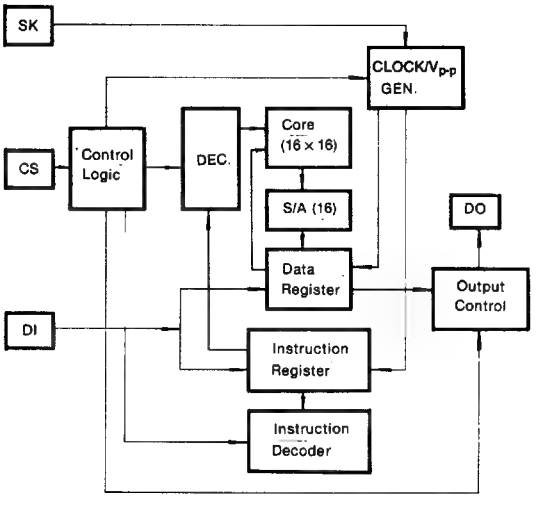
GENERAL DESCRIPTION

The KM93C07 is a CMOS 5V Only 256 bit non-volatile, sequential EEPROM. It is fabricated with the well defined floating-gate CMOS technology using Folwer-Nordheim tunneling for erasing and programming.

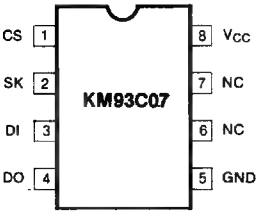
The KM93C07 is organized as 16 registers of 16 bits each, which can be read/written serially by a microprocessor. It operates in a self-timed mode with the DI pin indicating the R/$\overline{B}$ status of the device.

The KM93C07 is designed for applications up to 10,000 erase/write cycles per byte and over 10 years of data retention.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



PIN NAMES

Pin Name	Pin Function
CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
N.C.	No Connection
V_{CC}	Power Supply
GND	Ground

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}	−0.3 to 7.0	V
Temperature Under Bias	T_{bias}	−10 to +85	°C
Storage Temperature	T_{stg}	−65 to +125	°C

*Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of the data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V
Input High Voltage, all inputs	V_{IH}	2.0	–	V_{CC} + 0.3	V
Input Low Voltage, all inputs	V_{IL}	−0.3	—	0.8	V

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Operating Voltage	V_{CC}		4.5	5.5	V
Operating Current (DC)	I_{CC1}	V_{CC} = 5.5V, CS = 2.0V, SK = 2.0V		1	mA
Operating Current (AC)	I_{CC2}	V_{CC} = 5.5V, f_{sk} = 250KHz		5	mA
Standby Current (TTL)	I_{SB1}	V_{CC} = 5.5V, CS = 0.8V		250	μA
Standby Current (CMOS)	I_{SB2}	V_{CC} = 5.5V, CS = 0V		100	μA
Input Voltage Levels	V_{IL} V_{IH}		−0.3 2.0	0.8 V_{CC} + 0.3	V V
Output Voltage Levels	V_{OL} V_{OH}	I_{OL} = 2.1mA I_{OH} = −400μA	 2.4	0.4	V V
Input Leakage Current	I_{LI}	V_{IN} = 5.5V		10	μA
Output Leakage Current	I_{LO}	V_{OUT} = 5.5V, CS = 0V		10	μA

INSTRUCTION SET FOR MODE SELECTION

Instruction	SB	OP Code	Address	Data	Comment
READ	1	10XX	A3A2A1A0	D_{OUT}	Read register A3A2A1A0
WRITE	1	01XX	A3A2A1A0	D15-D0	Write register A3A2A1A0
ERASE	1	11XX	A3A2A1A0	—	Erase register A3A2A1A0
EWEN	1	0011	xxxx	—	Erase/Write enable
EWDS	1	0000	xxxx	—	Erase/Write disable
ERAL	1	0010	xxxx	—	Erase all registers
WRAL	1	0001	xxxx	D15-D0	Write all registers

The KM93C07 provides 7 instructions as shown. Note that all the instructions require the SB bit and the next 8 bits to carry the 4-bit OP code and the 4-bit address for 1 of 16, 16-bit registers.

AC TEST CONDITIONS

Parameter	Value
Input Pulse Levels	0.45 to 2.4V
Input Rise and Fall Times	20 ns
Input and Output Timing Levels	0.8V and 2.0V
Output Load	1 TTL Gate and $C_L = 100pF$

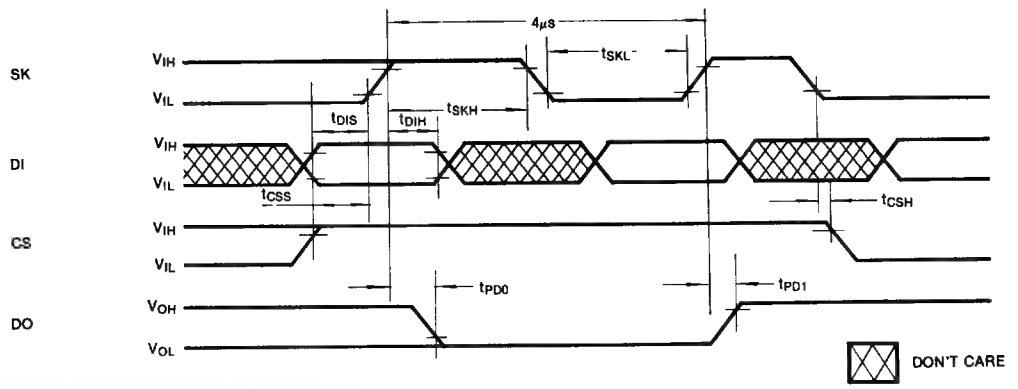
AC OPERATING CHARACTERISTICS ($T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise noted.)

Parameter	Symbol	Test Conditions	Min	Max	Unit
SK Frequency			0	250	KHz
SK High Time	t_{SKH}		1		μs
SK Low Time	t_{SKL}		1		μs
Chip Select Setup Time	t_{CSS}		0.2		μs
Chip Select Hold Time	t_{CSH}		0		μs
Data Setup Time	t_{DIS}		0.4		μs
Data Hold Time	t_{DIH}		0.4		μs
Output High Delay Time	t_{PD1}	$V_{OL} = 0.8V$, $V_{OH} = 2.0V$		2	μs
Output Low Delay Time	t_{PD0}	$V_{IL} = 0.45V$, $V_{IH} = 2.4V$		2	μs
Program Cycle Time	$t_{E/W}$			10	ms
Min CS Low Time	t_{CS}		1		μs
Rising Edge of CS to Status Valid	t_{SV}			1	μs
Falling Edge of CS to D_{OUT} TRI-STATE	t_{0H}, t_{1H}			0.4	μA

Note 1: The SK frequency spec, specifies a minimum SK clock period of 4μs, therefore in a SK clock cycle $t_{SKH} + t_{SKL}$ must be greater than or equal to 4μs.
e.q., if $t_{SKL} = 1\mu s$ then the minimum $t_{SKH} = 3\mu s$ in order to meet the SK frequency specification.
Note 2: CS must be brought low for a minimum 1μs(t_{CS}) between consecutive instruction cycles.

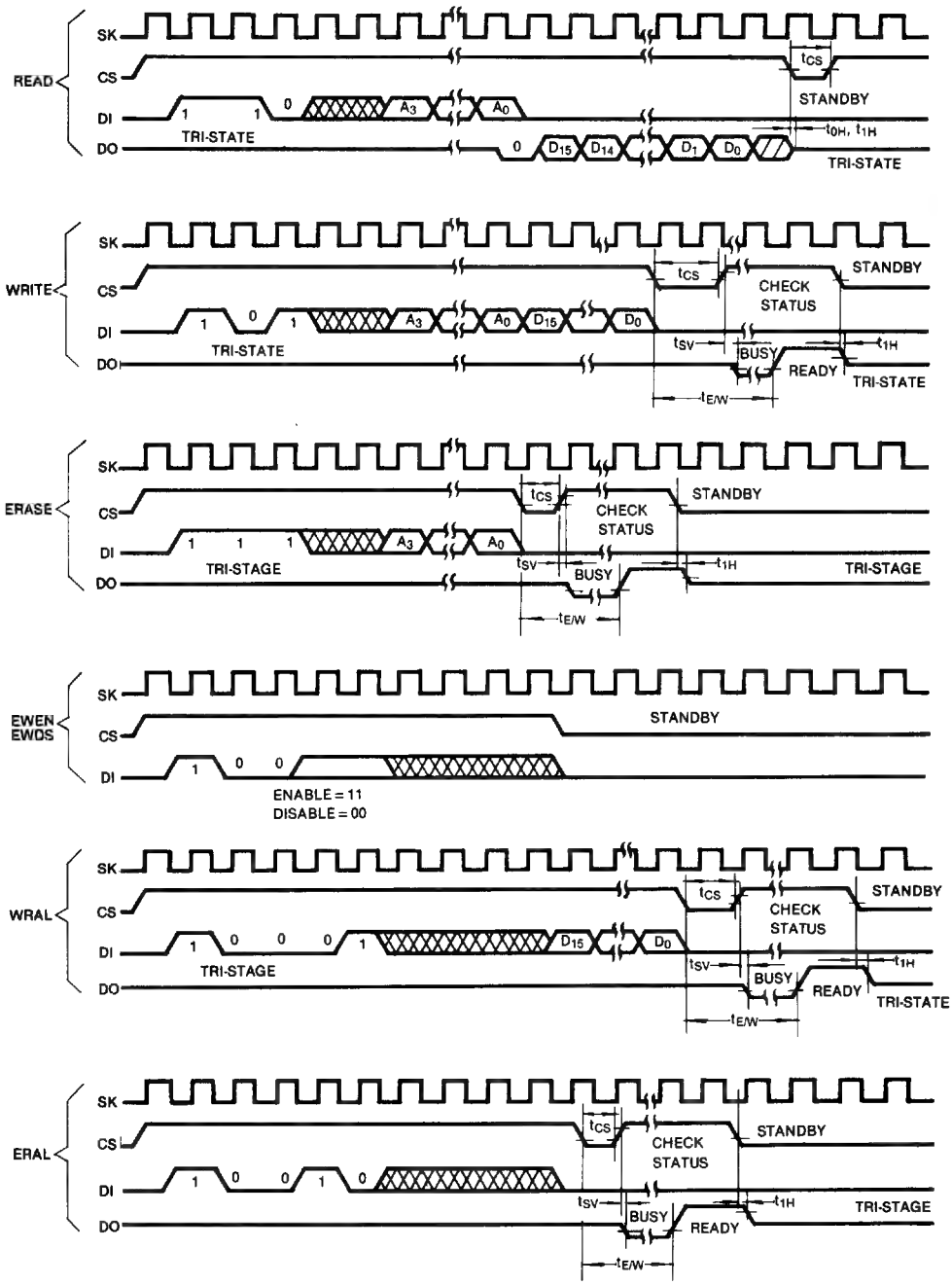
TIMING DIAGRAMS

SYNCHRONOUS DATA TIMING



TIMING DIAGRAMS (Continued)

INSTRUCTION TIMING



DEVICE OPERATION

The KM93C07 is 256 bit CMOS serial I/O EEPROM used with microcontrollers for nonvolatile memory applications. The on-chip programming voltage generator allows user to use a single 5V power supply. The erase and write cycle of the KM93C07 is self-timed with ready/$\overline{busy}$ status of the chip indicated at the DO pin. All the operations of the chip is proceeded by a four OP code bits, facilitating inherent protection against false write. The DO pin is tri-state except for the read period and the ready/$\overline{busy}$ indication period to eliminated bus contention.

READ

After a read instruction and address set is received, low to high transition of the SK clock produces output data at DO pin. A dummy bit (logical "0") proceeds the 16 bit data output string.

EWEN / EWDS

The KM93C07 is at the erase/write disable (EWDS) state during power-up period to protect against accidental disturb. After the power up period, the erase/write operation must be proceeded by an erase/write enable (EWEN) operation. The erase/write enable (EWEN) mode is maintained until a erase/write disable (EWDS) operation is executed or V_{CC} is removed from the part. Execution of READ operation is independent of both EWEN and EWDS instructions.

ERASE

Before a write cycle, an erase cycle need to be operated to reset the EEPROM cells to the "erase" state. The chip starts a self-timed erase cycle by dropping CS low after an erase instruction and address set is input. The chip's ready/$\overline{busy}$ status is indicated at the DO pin by bringing CS high during erase cycle.

WRITE

The write operation is started by sequentially loading its instruction, address, and data set. After the last bit of data is input on the DI pin, CS must be brought low before the rising edge of the SK clock. This falling edge of CS initiates the self-timed write cycle. Like the erase operation, write cycle has the ready/$\overline{busy}$ function.

ERAL (chip erase)

Entire memory array is erased, i.e., logical "1" state, by this chip erase (ERAL) operation. The chip erase cycle is identical to the erase cycle except for different OP code.

WRAL (chip write)

The entire array need to be erased before this chip write mode operation. Data given during this mode are written to all cells in the corresponding column simultaneously.

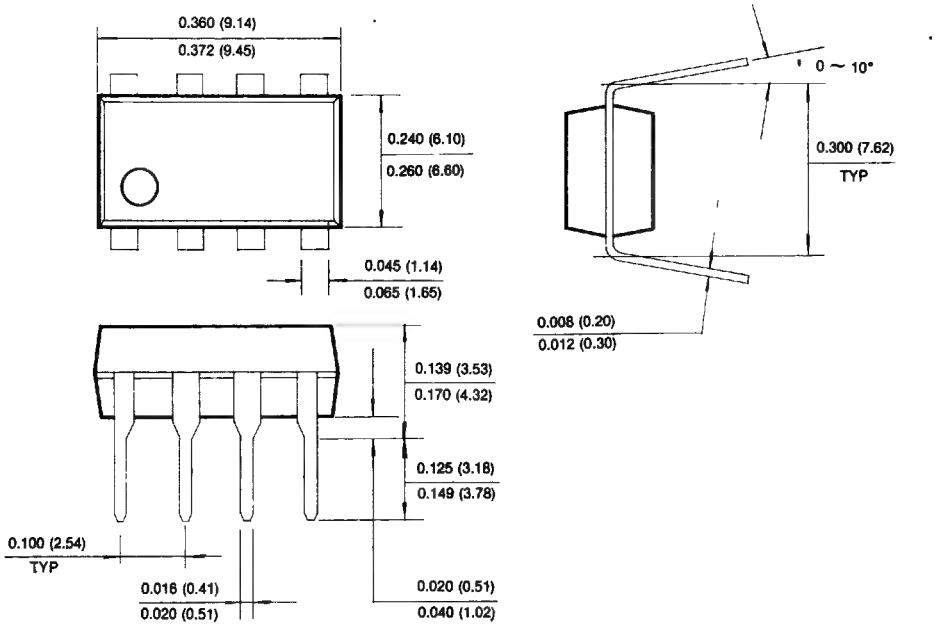
READY / $\overline{BUSY}$

The ready/busy status of KM93C07 during all the self-timed programming cycle (erase, write, chip erase, chip write) is indicated at DO pin. Bringing CS pin high, after the self-timed programming cycle is initiated, will produces logic '0' at DO pin if the chip is still programming and logic '1' if the programming cycle is completed.

PACKAGE DIMENSIONS

8 PIN PLASTIC DUAL IN LINE PACKAGE

unit; inches (millimeters)



4

1K Bit Serial Electrically Erasable PROM

FEATURES

- **Operating temperature range**
  - **— KM93C46: Commercial**
  - **— KM93C46I: Industrial**
- **Single 5 Volt supply**
- **High performance advanced CMOS technology**
  - **— Reliable floating gate technology**
- **64 x 16 serial read/write memory**
- **TTL compatible**
- **Low power dissipation**
  - **— Standby current: 250μA (TTL)**
  - **— Active current: 5 mA (TTL)**
- **Enhanced write protection**
- **Self-timed programming cycle**
- **Device status signal during programming**
- **10,000 Cycle Endurance**
- **Available in plastic DIP and SOP**

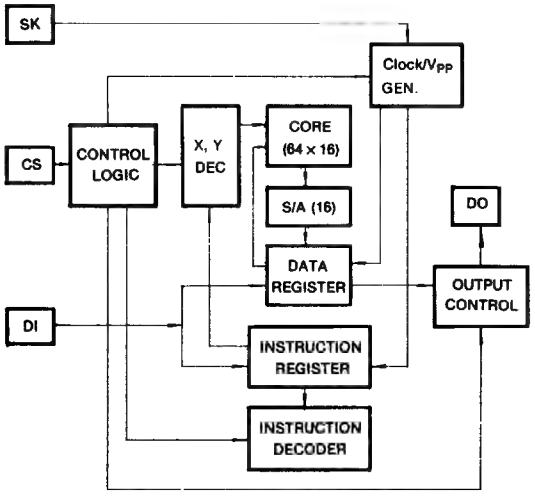
GENERAL DESCRIPTION

The KM93C46 is a CMOS 5V Only 1,024 bit non-volatile, sequential EEPROM. It is fabricated with the well defined floating gate CMOS technology using Folwer-Nordheim tunneling for erasing and programming.

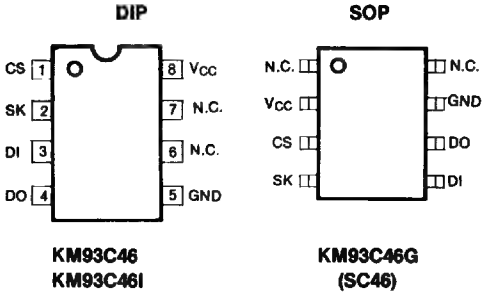
The KM93C46 is organized as 64 registers of 16 bits each, which can be read/written serially by a microprocessor. It operates in a self-timed mode with the DO pin indicating the READY/$\overline{\text{BUSY}}$ status of the device.

The KM93C46 is designed for applications up to 10,000 erase/write cycles per byte and over 10 years of data retention.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



KM93C46
KM93C46I

KM93C46G
(SC46)

PIN NAMES

Pin Name	Pin Function
CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
N.C.	No Connection
V_{CC}	Power Supply
GND	Ground

ABSOLUTE MAXIMUM RATINGS*

Parameter		Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}		V_{IN}	−0.3 to 7.0	V
Temperature Under Bias	Commercial	T_{bias}	−10 to +85	°C
	Industrial		−65 to +125	
Storage Temperature		T_{stg}	−65 to +125	°C

*Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of the data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

KM93C45 $T_A = 0$ to 70°C, Voltages referenced to V_{SS}
KM93C46I $T_A = -40$ to 85°C, Voltages referenced to V_{SS}

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V
Input High Voltage, all inputs	V_{IH}	2.0	—	$V_{CC}+0.3$	V
Input Low Voltage, all inputs	V_{IL}	−0.3	—	0.8	V

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Max	Unit
Operating Voltage	V_{CC}		4.5	5.5	V
Operating Current (DC)	I_{CC1}	$V_{CC}=5.5V$, CS = 2.0V, SK = 2.0V		1	mA
Operating Current (AC)	I_{CC2}	$V_{CC}=5.5V$, $f_{sk}=250KHz$		5	mA
Standby Current (TTL)	I_{SB1}	$V_{CC}=5.5V$, CS = 0.8V		250	μA
Standby Current (CMOS)	I_{SB2}	$V_{CC}=5.5V$, CS = 0V		100	μA
Input Voltage Levels	V_{IL} V_{IH}		−0.3 2.0	0.8 $V_{CC}+0.3$	V V
Output Voltage Levels	V_{OL} V_{OH}	$I_{OL}=2.1mA$ $I_{OH}=-400\mu A$	 2.4	0.4	V V
Input Leakage Current	I_{LI}	$V_{IN}=5.5V$		10	μA
Output Leakage Current	I_{LO}	$V_{OUT}=5.5V$, CS = 0V		10	μA

Note: Minimum V_{CC} for READ operation is 2.7V with minimum V_{OH} 1.5V

INSTRUCTION SET FOR MODE SELECTION

Instruction	SB	OP Code	Address	Data	Comment
READ	1	10	A5A4A3A2A1A0	D_{OUT}	Read register A5A4A3A2A1A0
WRITE	1	01	A5A4A3A2A1A0	D15-D0	Write register A5A4A3A2A1A0
ERASE	1	11	A5A4A3A2A1A0	—	Erase register A5A4A3A2A1A0
EWEN	1	00	11XXXX	—	Erase/Write enable
EWDS	1	00	00XXXX	—	Erase/Write disable
ERAL	1	00	10XXXX	—	Erase all registers
WRAL	1	00	01XXXX	D15-D0	Write all registers

The KM93C46 provides 7 instructions as shown. Note that all the instructions start with a logic "1" start bit, and the next 8 bits carry the 2-bit OP code and the 6-bit address for 1 of 64, 16-bit register.

AC TEST CONDITIONS

Parameter	Value
Input Pulse Levels	0.45 to 2.4V
Input Rise and Fall Times	20 ns
Input and Output Timing Levels	0.8V and 2.0V
Output Load	1 TTL Gate and $C_L = 100pF$

AC OPERATING CHARACTERISTICS

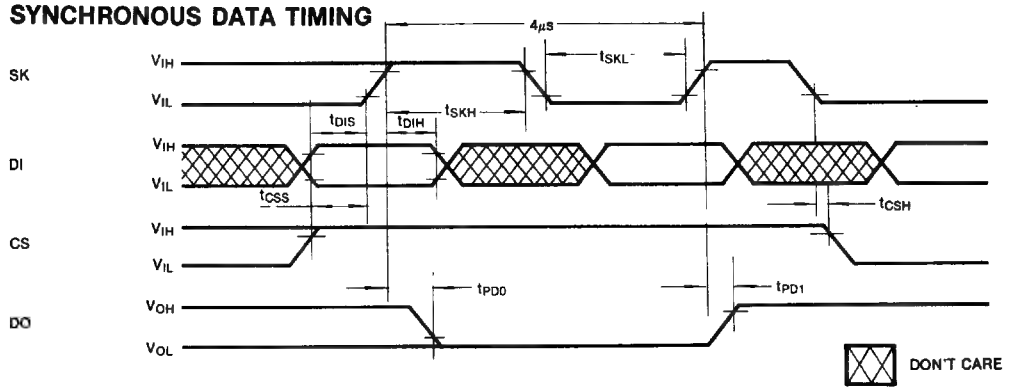
KM93C46 $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise noted.
KM93C46I $T_A = -40°C$ to $85°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise noted.

Parameter	Symbol	Test Conditions	Min	Max	Unit
SK Frequency			0	250	KHz
SK High Time	t_{SKH}		1		μs
SK Low Time	t_{SKL}		1		μs
Chip Select Setup Time	t_{CSS}		0.2		μs
Chip Select Hold Time	t_{CSH}		0		μs
Data Setup Time	t_{DIS}		0.4		μs
Data Hold Time	t_{DIH}		0.4		μs
Output High Delay Time	t_{PD1}	$V_{OL} = 0.8V$, $V_{OH} = 2.0V$		2	μs
Output Low Delay Time	t_{PD0}	$V_{IL} = 0.45V$, $V_{IH} = 2.4V$		2	μs
Self-Timed Program Cycle Time	$t_{E/W}$			10	ms
Min CS Low Time	t_{CS}		1		μs
Rising Edge of CS to Status Valid	t_{SV}			1	μs
Falling Edge of CS to D_{OUT} TRI-STATE	t_{0H}, t_{1H}			0.4	μA

Note 1: The SK frequency spec, specifies a minimum SK clock period of 4μs, therefore in a SK clock cycle $t_{SKH} + t_{SKL}$ must be greater than or equal to 4μs.
e.q., if $t_{SKL} = 1\mu s$ then the minimum $t_{SKH} = 3\mu s$ in order to meet the SK frequency specification.
Note 2: CS must be brought low for a minimum $1\mu s(t_{CS})$ between consecutive instruction cycles.

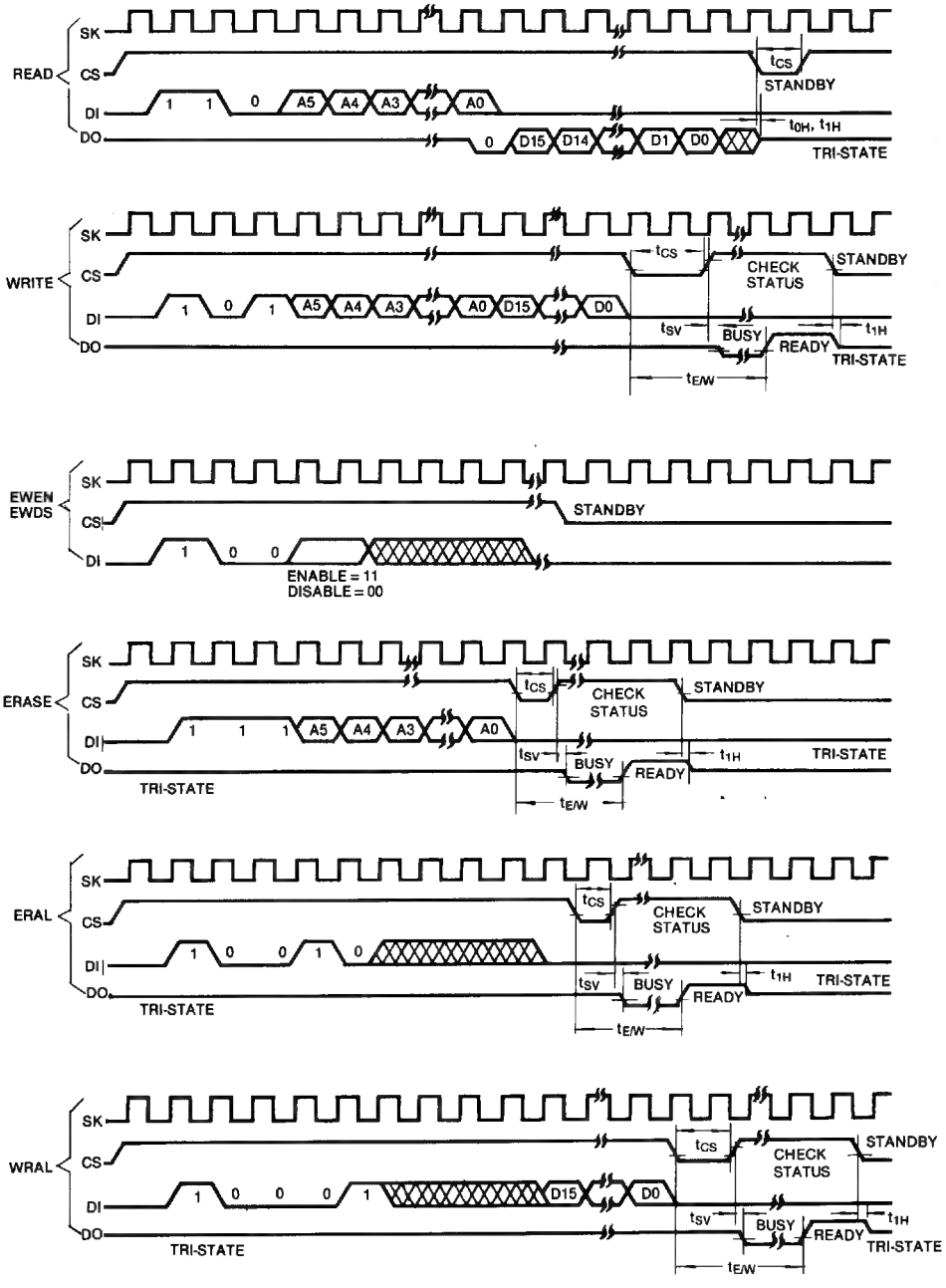
TIMING DIAGRAMS

SYNCHRONOUS DATA TIMING



TIMING DIAGRAMS (Continued)

INSTRUCTION TIMING



DEVICE OPERATION

The KM93C46 is a 1K bit CMOS serial I/O EEPROM used with microcontrollers for non-volatile memory applications. The on-chip programming voltage generator allows user to use a single 5V power supply. The erase and write cycle of the KM93C46 is self-timed with ready/$\overline{busy}$ status of the chip indicated at the DO pin. All the operations of the chip is proceeded by a two OP code bits, facilitating inherent protection against false write. The DO pin is in tri-state except for the read period and the ready/$\overline{busy}$ indication period to eliminate bus contention.

READ

After a read instruction and address set is received, low to high transition of the SK clock produces output data at DO pin. A dummy bit (logical "0") proceeds the 16 bit data output string.

EWEN / EWDS

The KM93C46 is at the erase/write disable (EWDS) state during power-up period to protect against accidental disturb. After the power up period, the erase/write operation must be proceeded by an erase/write enable (EWEN) operation. The erase/write enable (EWEN) mode is maintained until a erase/write disable (EWDS) operation is executed or V_{CC} is removed from the part. Execution of READ operation is independent of both EWEN and EWDS instructions.

ERASE

Before a write cycle, an erase cycle need to be operated to reset the EEPROM cells to the "erase" state. The chip starts the self-timed erase cycle by dropping CS low after an erase instruction and address set is input. The chip's ready/$\overline{busy}$ status is indicated at the DO pin by bringing CS high during erase cycle.

WRITE

The write operation is started by sequentially loading its instruction, address, and data set. After the last bit of data is input on the DI pin, CS must be brought low before the rising edge of the SK clock. This falling edge of CS initiates the self-timed write cycle. Like the erase operation, write cycle has the ready/$\overline{busy}$ function.

ERAL (chip erase)

Entire memory array is erased, i.e., logical "1" state, by this chip erase (ERAL) operation. The chip erase cycle is identical to the erase cycle except for different OP code.

WRAL (chip write)

The entire array need to be erased before this chip write mode operation. Data given during this mode are written to all cells in the corresponding column simultaneously.

READY / $\overline{BUSY}$

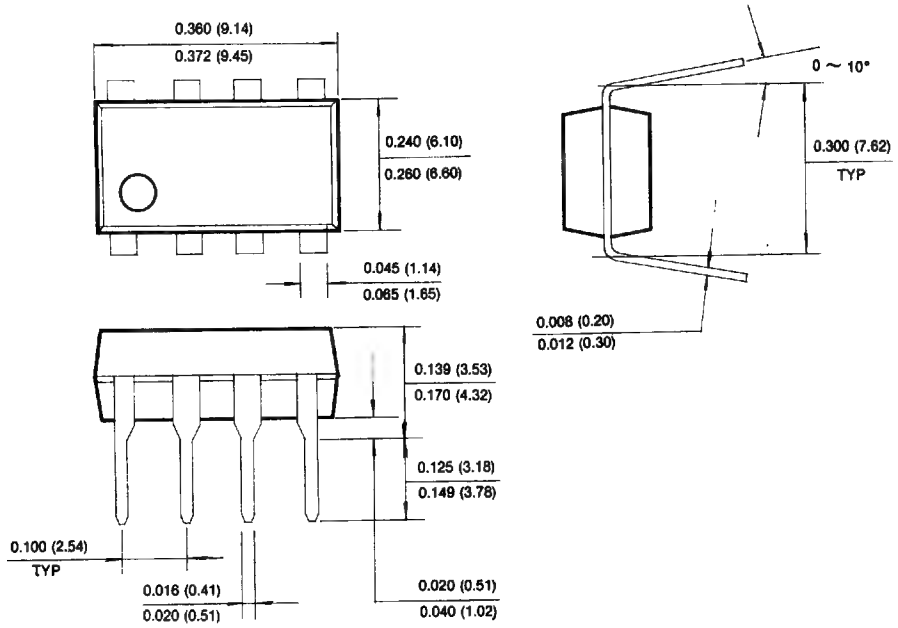
The ready/$\overline{busy}$ status of KM93C46 during all the self-timed programming cycle (erase, write, chip erase, chip write) is indicated at DO pin. Bringing CS pin high, after the self-timed programming cycle is initiated, will produces logic '0' at DO pin if the chip is still programming and logic '1' if the programming cycle is completed.

The KM93C46 has extended READ V_{CC} margin. READ operation is functional at V_{CC} 5.5-2.7V. AC/DC parameters at this V_{CC} range meet values given in this spec except for $V_{OH} = 1.5V$ at $V_{CC} = 2.7V$..

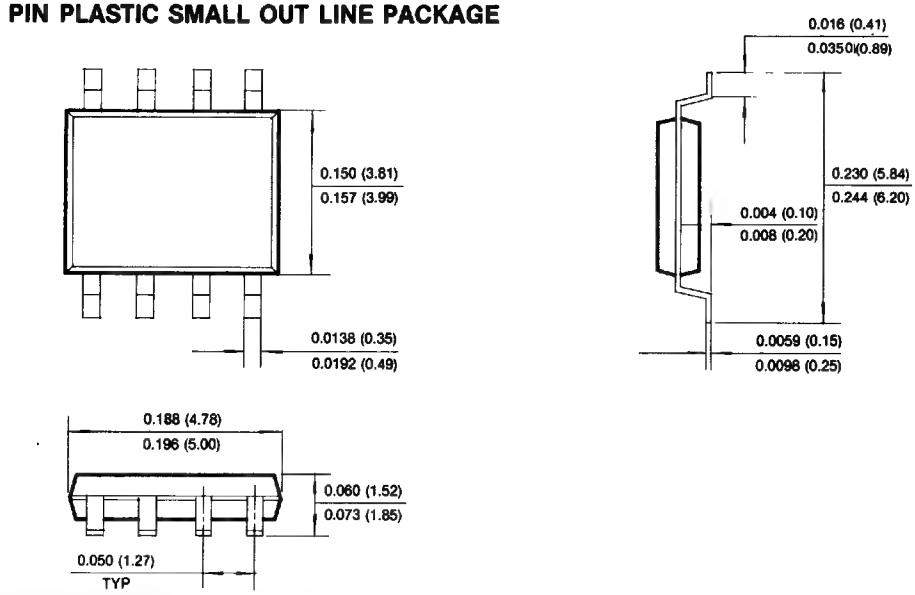
PACKAGE DIMENSIONS

8 PIN PLASTIC DUAL IN LINE PACKAGE

unit; inches (millimeters)



8 PIN PLASTIC SMALL OUT LINE PACKAGE



2K x 8 Bit CMOS Electrically Erasable PROM

FEATURES

- **Operating Temperature Range**
  - **— KM28C16/KM28C17: Commercial**
  - **— KM28C16I/KM28C17I: Industrial**
- **Simple Byte Write**
  - **— Single TTL Level Write Signal**
  - **— Latched Address and Data**
  - **— Automatic Write Timing**
  - **— Automatic Internal Erase-Before-Write**
  - **— Ready/$\overline{\text{Busy}}$ Output Pin (KM28C17)**
  - **— $\overline{\text{Data}}$-Polling and Verification**
- **32-byte page Write 2ms max**
  - **— Effective 62.5μs/byte write**
- **Enhanced Write Protection**
- **Single 5 volt Supply**
- **Fast Access Time: 150ns**
- **Power: 100μA—Standby (max)**
  30mA—Operating (max)
- **Two Line Control-Eliminates Bus Contention**
- **10,000 Cycle Endurance**
- **JEDEC Byte-wide Memory Pinput**

GENERAL DESCRIPTION

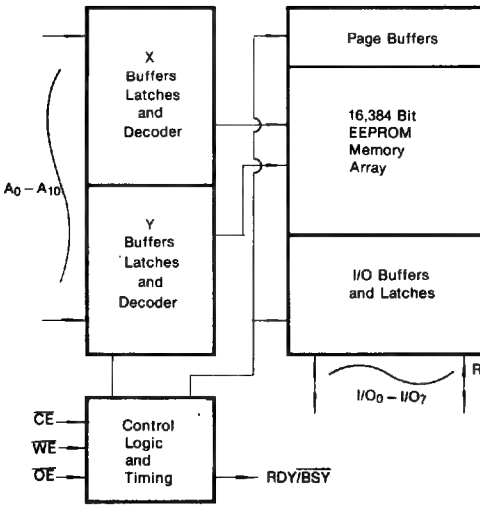
The KM28C16/C17 is a 2,048 x 8 bit Electrically Erasable Programmable Read Only Memory. Its data can be modified using simple TTL level signals and a single 5 volt power supply.

Writing data into the KM28C16/C17 is very simple. The internally self-timed writing cycle latches both address and data to provide a free system bus during the 2ms (max) write period. A 32-byte page write enables an entire chip written in 128ms.

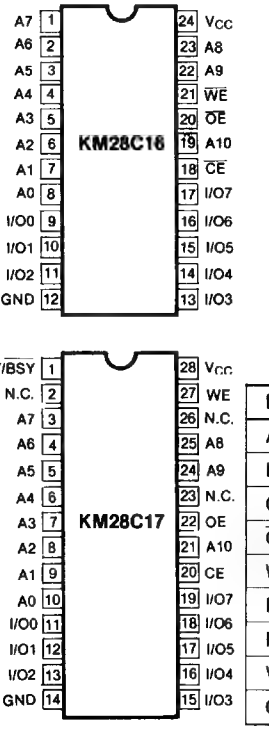
The KM28C16/C17 features $\overline{\text{Data}}$-polling, which enables the EEPROM to signal the processor that a write operation is complete without requiring the use of any external hardware. The KM28C17 features Read/$\overline{\text{Busy}}$ which is a hardware scheme to signal the status of the write operation and is especially useful in interrupt driven systems.

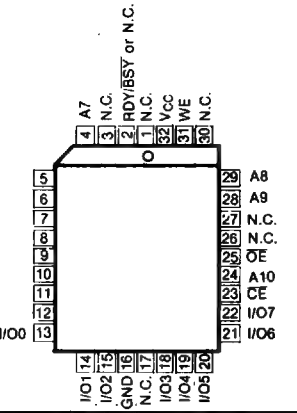
The KM28C16/C17 is fabricated with the well defined floating-gate CMOS technology using Fowler-Nordheim tunneling for erasing and programming.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION





Pin Name	Pin Function
A_0-A_{10}	Address Inputs
I/O_0-I/O_7	Data Inputs/Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
WE	Write Enable
RDY/$\overline{BSY}$	Ready/$\overline{Busy}$ Output
N.C.	No Connection
V_{CC}	+5V
GND	Ground

ELECTRICAL CHARACTERISTICS

Parameter		Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}		V_{IN}	−0.3 to 7.0	V
Temperature Under Bias	Commercial	T_{bias}	−10 to +85	°C
	Industrial		−65 to +125	°C
Storage Temperature		T_{stg}	−65 to +125	°C
Short Circuit Output Current		I_{OS}	5	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

4

RECOMMENDED OPERATING CONDITIONS

KM28C16/C17: Voltage reference to V_{SS}, $T_A = 0°C$ to $+70°C$
KM28C16I/C17I: Voltage reference to V_{SS}, $T_A = -40°C$ to $+85°C$

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V
Input High Voltage, all Inputs	V_{IH}	2.0	—	$V_{CC}+0.3$	V
Input Low Voltage, all Inputs	V_{IL}	−0.3	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Operating Current	I_{CC}	$\overline{CE} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$ All I/O's = OPEN All Addresses* (note 1)	—	30	mA
Standby Current (TTL)	I_{SB1}	$\overline{CE} = V_{IH}$ All I/O's = OPEN		1	mA
Standby Current (CMOS)	I_{SB2}	$\overline{CE} = V_{CC} - 0.2$ All I/O's = OPEN	—	100	μA
Input Leakage Current	I_{LI}	$V_{IN} = 0$ to 5.5V	—	10	μA
Output Leakage Current	I_{LO}	$V_{OUT} = 0$ to 5.5V	—	10	μA
Output High Voltage Level	V_{OH}	$I_{OH} = -400\mu A$	2.4	—	V
Output Low Voltage Level	V_{OL}	$I_{OL} = 2.1mA$	—	0.4	V
Write Inhibit V_{CC} Level	V_{WI}		3.8	—	V

* Note 1. All addresses toggling from V_{IL} to V_{IH} at 6.7MHz

CAPACITANCE ($T_A = 25°C$, $V_{CC} = 5V$, $f = 1.0$ MHz)

Parameter	Symbol	Conditions	Min	Max	Unit
Input/Output Capacitance	$C_{I/O}$	$V_{I/O} = 0V$	—	8	pF
Input Capacitance	C_{IN}	$V_{IN} = 0V$	—	8	pF

Note: Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O	Power
L	L	H	Read	D_{OUT}	Active
L	H	L	Write	D_{IN}	Active
L	L	H	$\overline{DATA}$-Polling	$I/O_7 = \overline{D_7}$	Active
H	X	X	Standby & Write Inhibit	High-Z	Standby
X	L	X	Write Inhibit	—	—
X	X	H	Write Inhibit	—	—

AC CHARACTERISTICS

KM28C16/C17: $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise noted.
KM28C16I/C17I: $T_A = -40°C$ to $+85°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise noted.

TEST CONDITIONS

Parameter	Value
Input Pulse Levels	0.45 to 2.4V
Input Rise and Fall Times	20 ns
Input and Output Timing Levels	0.8V and 2.0V
Output Load	1 TTL Gate and $C_L = 100pF$

READ CYCLE

Parameter	Symbol	KM28C16-15 KM28C16I-15 KM28C17-15 KM28C17I-15		KM28C16-20 KM28C16I-20 KM28C17-20 KM28C17I-20		KM28C16-25 KM28C16I-25 KM28C17-25 KM28C17I-25		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	150		200		250		ns
Chip Enable Access Time	t_{CE}		150		200		250	ns
Address Access Time	t_{AA}		150		200		250	ns
Output Enable Access Time	t_{OE}		60		80		100	ns
Output or Chip Disable to Output High-Z	t_{DF}	5	50	5	70	5	90	ns
Output Hold from Address Change, Chip Disable, or Output Disable Whichever Occurs First	t_{OH}	10		10		10		ns

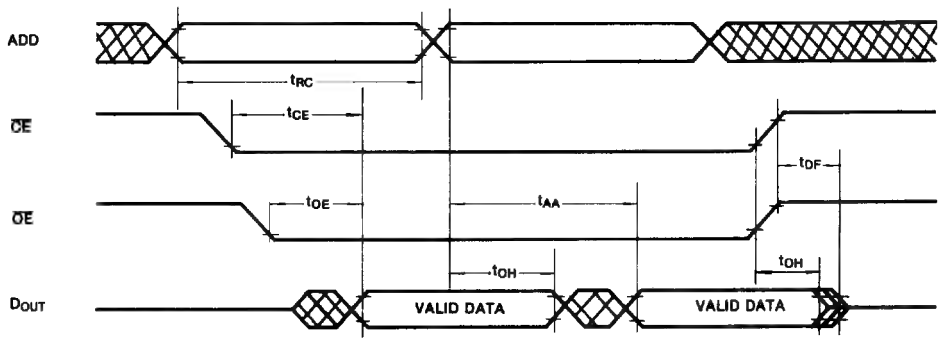
WRITE CYCLE

Parameter	Symbol	Min	Max	Unit
Write Cycle Time	t_{WC}	2		ms
Address Set-Up Time	t_{AS}	0		ns
Address Hold Time	t_{AH}	80		ns
Write Set-Up Time	t_{CS}	0		ns
Write Hold Time	t_{CH}	0		ns
$\overline{CE}$ Pulse Width	t_{CW}	100		ns
Output Enable Set-Up Time	t_{OES}	10		ns
Output Enable Hold Time	t_{OEH}	10		ns
$\overline{WE}$ Pulse Width	t_{WP}	100		ns
Data Set-Up Time	t_{DS}	50		ns
Data Hold Time	t_{DH}	10		ns
Time to Device Busy	t_{DB}		100	ns
Busy to Write Recovery Time	t_{BWR}	50		ns
Byte Load Cycle Time	t_{BLC}	0.2	100	μs
Last Byte Loaded to Data Polling	t_{LP}	1		μs

Note: The timer for t_{BLC} is reset at a falling edge of $\overline{WE}$ and starts at a rising edge of $\overline{WE}$.

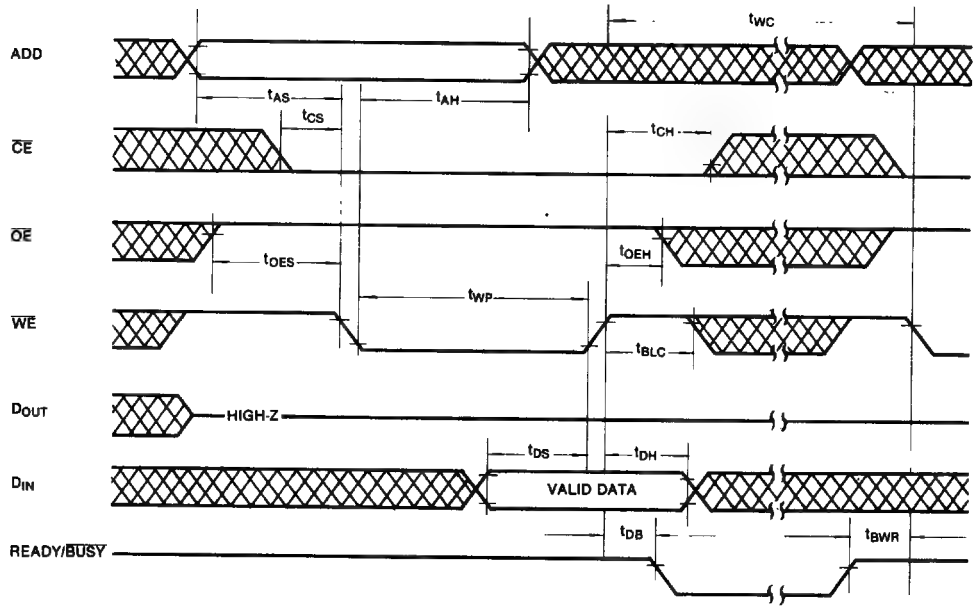
TIMING DIAGRAMS

READ CYCLE $\overline{WE} = V_{IH}$

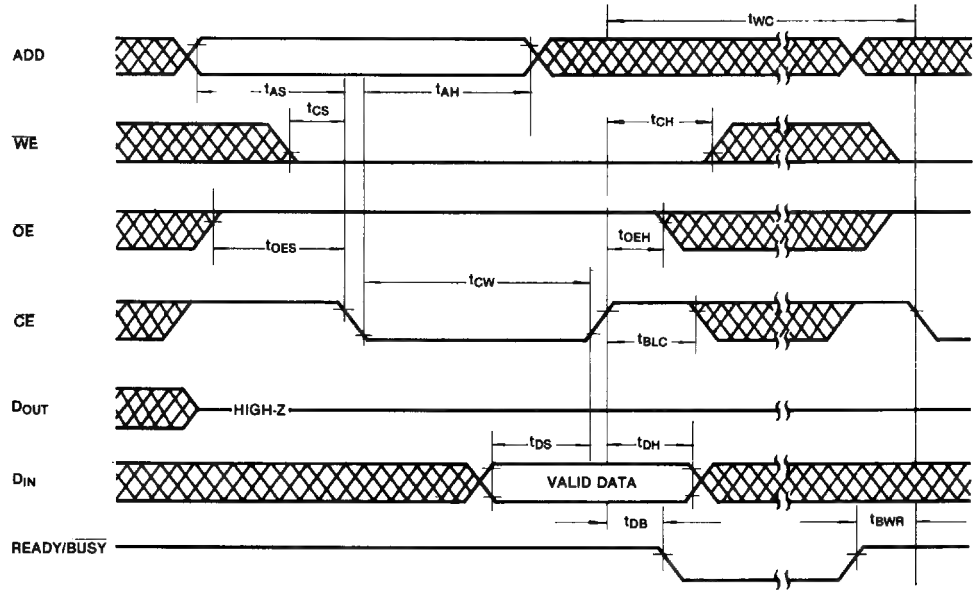


TIMING DIAGRAMS (Continued)

$\overline{WE}$ CONTROLLED WRITE CYCLE

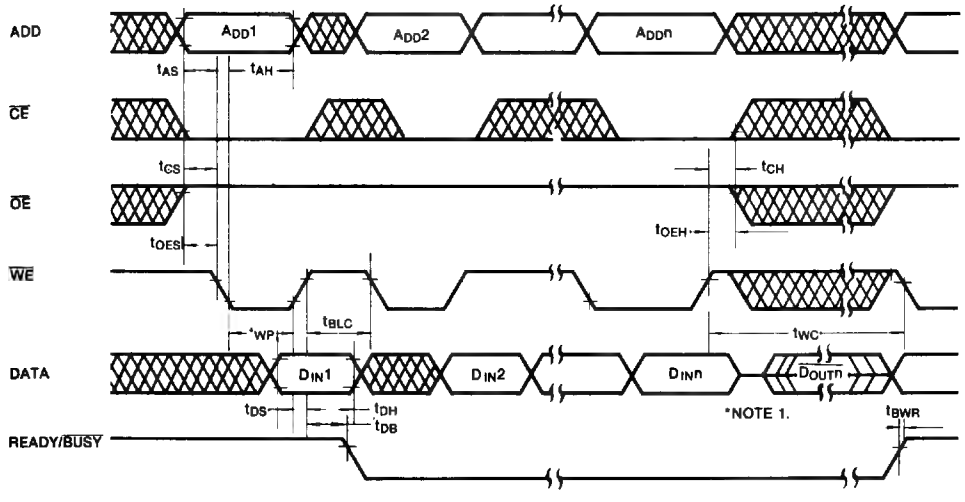


$\overline{CE}$ CONTROLLED WRITE

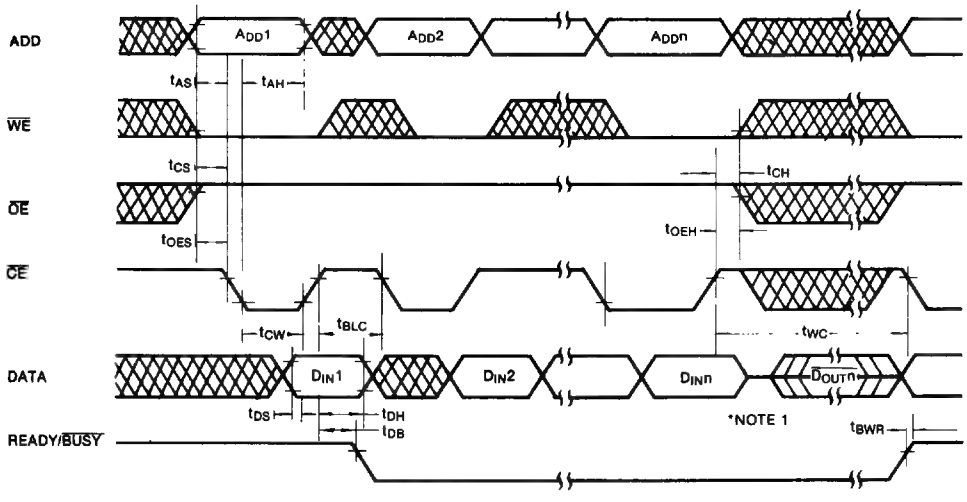


TIMING DIAGRAMS (Continued)

PAGE MODE WRITE ($\overline{WE}$ CONTROLLED WRITE CYCLE)



PAGE MODE WRITE ($\overline{CE}$ CONTROLLED WRITE CYCLE)



*NOTE: I/O_7 Outputs $\overline{D_{INn}}$ when the chip is read. I/O_0-I/O_6 have tristate.

DEVICE OPERATION

READ

Reading data from the KM28C16/C17 is similar to reading data from a SRAM. A read cycle occurs when $\overline{WE}$ is high and $\overline{CE}$ and $\overline{OE}$ are low. If either $\overline{CE}$ or $\overline{OE}$ goes high the read cycle is terminated. This two line control eliminates bus contention in a system environment. The Data I/O pins are in the high impedance state whenever $\overline{OE}$ or $\overline{CE}$ is high.

WRITE

Writing data into the KM28C16/C17 is easy. Only a single 5V supply and TTL level signals are required. The on-chip data latches, address latches, high voltage generator, and fully self-timed control logic make writing as easy as writing to a SRAM.

**** BYTE WRITE MODE ****

The byte write mode of the KM28C16/C17 is only a part of the page write mode. A single byte data loading followed by a t_{BLC} time-out and by a nonvolatile write cycle will complete a byte mode write. In this mode, the write is exactly identical to that of the KM28C16/C17.

**** PAGE WRITE MODE ****

The KM28C16/C17 allows up to 32 byte to be written in a single page write cycle. A page write cycle consists of a data loading period, in which from 1 to 32 byte data are loaded into the KM28C16/C17 internal registers and a nonvolatile write period, in which the loaded data in the registers are written to the EEPROM cells of the selected page.

Data are loaded into the KM28C16/C17 by sequentially pulsing $\overline{WE}$ with $\overline{CE}$ low and $\overline{OE}$ high. On each $\overline{WE}$, address is latched on the falling edge of the $\overline{WE}$ and data is latched on the rising edge of the $\overline{WE}$. The data can be loaded in any "Y" address order and can be renewed in a data loading period.

Since the timer for the data loading period (t_{BLC}) is reset at the falling edge of $\overline{WE}$ and starts at every rising edge of $\overline{WE}$, the only requirement on $\overline{WE}$ to continue the data loading is that the interval between $\overline{WE}$ pulses does not exceed the maximum t_{BLC} (100μs). If $\overline{OE}$ goes Low during the data loading period, further attempt to load the data will be ignored because the external $\overline{WE}$ signal is blocked by $\overline{OE}$ signal internally. Consequently, the t_{BLC} timer is not reset by the external $\overline{WE}$ pulse if $\overline{OE}$ is low.

The page address for the nonvolatile write is the "X" address (A_5-A_{10}) latched on the last $\overline{WE}$. The nonvolatile write period consists of an erase cycle and a program cycle. During the erase cycle, the existing data of the locations being addressed are erased. The new data latched at the register are written into the location during the program cycle. Note that only the addressed location in a page are rewritten during a page write cycle.

The KM28C16/C17 also supports $\overline{CE}$ controlled write cycle. That means $\overline{CE}$ can be used to latch address and data as well as $\overline{WE}$.

STANDBY

Power consumption is reduced to less than 100μA by deselecting the device with a high input on $\overline{CE}$. Whenever $\overline{CE}$ is high, the device is in the standby mode and I/O_0-I/O_7 are in the high impedance state, regardless of the state of $\overline{OE}$ or $\overline{WE}$.

DATA PROTECTION

Features have been designed into the KM28C16/C17 that prevent unwanted write cycles during power supply transitions and system noise periods.

The KM28C16/C17 has a protection feature against $\overline{WE}$ noises: a $\overline{WE}$ noise the width shorter than 20ns (typ.) will not start any unwanted write cycle.
Write cycles are also inhibited when V_{CC} is less than V_{WI} = 3.8 volts, the Write Inhibits V_{CC} level.
During power-up, the KM28C17 automatically prevents any write operation for a period of 2ms (typ.) after V_{CC} reaches the V_{WI} level. This will provide the system with sufficient time to bring $\overline{WE}$ and $\overline{CE}$ to a high level before a write can occur. Read cycles can be executed during this initialization period. Holding either $\overline{OE}$ low or $\overline{WE}$ high or $\overline{CE}$ high during power-on and power-off will inhibit inadvertent writes.

$\overline{DATA}$ POLLING

The KM28C16/C17 features $\overline{DATA}$-Polling at I/O_7 to detect the completion of a write cycle using a simple read and compare operation. Such a scheme does not require any external hardware. Reading the device at any time during a write operation will produce, at I/O_7, an inverted value of last data loaded into the EEPROM (I/O_0-I/O_6 are at the high impedance state). True data will be produced at all I/O's once the write cycle has been completed.

DEVICE OPERATION

READY/$\overline{BUSY}$

The KM28C17 has a Ready/$\overline{Busy}$ output on pin 1 that indicates when the write cycle is complete. The pin is normally high except when a write cycle is in progress, in which case the pin is low.

The Ready/$\overline{Busy}$ output is configured as open-drain driver there-by allowing two or more Ready/$\overline{Busy}$ output to be OR-tied. This pin requires an appropriate pull-up resistor for proper operation. The pull-up resistor value maybe calculated as follows.

$$RP = \frac{V_{CC}(max) - V_{OL}(max)}{I_{OL} + I_L} = \frac{5.1V}{2.1mA + I_L}$$

where I_L is the sum of the input currents of all devices tied to the Ready/$\overline{Busy}$ pin.

ENDURANCE AND DATA RETENTION

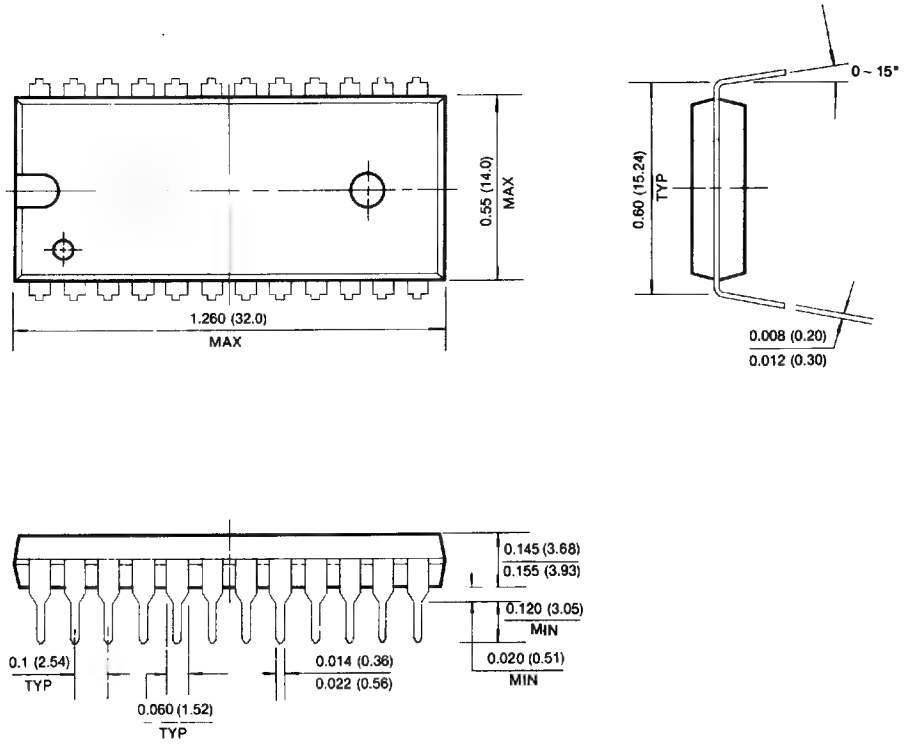
KM28C16/C17 is designed for applications requiring up to 10,000 write cycles per EEPROM byte and ten years of data retention. This means that each byte may be reliably written 10,000 times without degrading device operation and that the data in the byte will remain valid after its last write operation for ten years with or without power applied.

4

PACKAGE DIMENSIONS

24 LEAD PLASTIC DUAL IN LINE PACKAGE

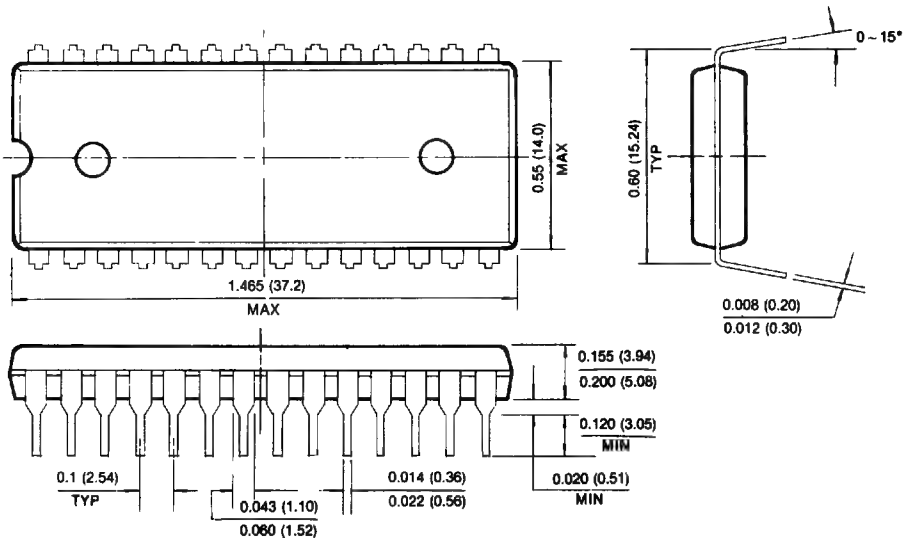
Units: Inches (millimeters)



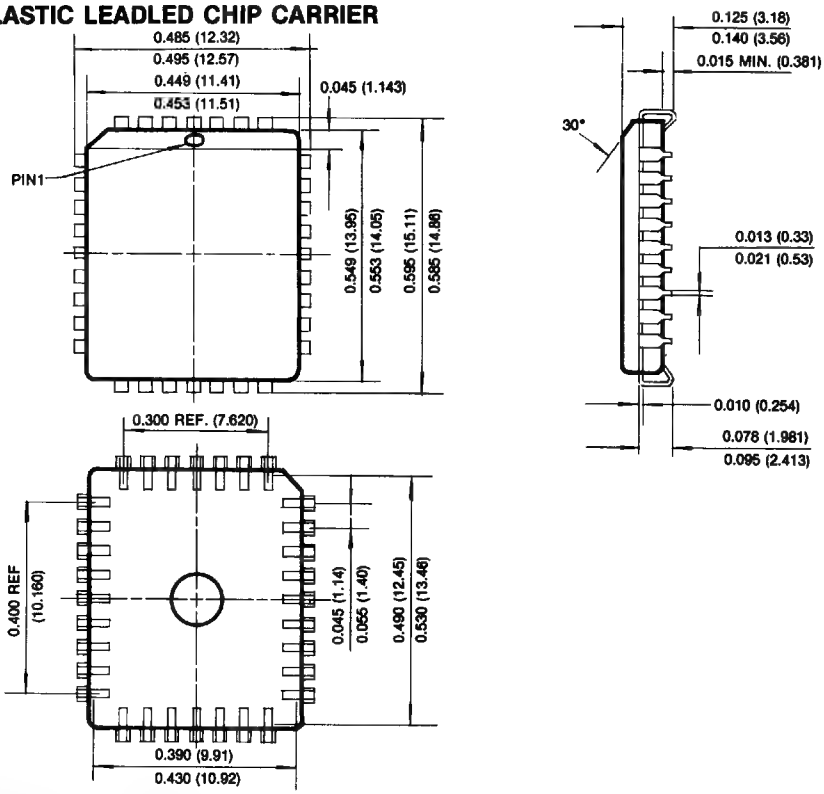
PACKAGE DIMENSIONS

28 LEAD PLASTIC DUAL IN LINE PACKAGE

Units: Inches (millimeters)



32 PIN PLASTIC LEADLED CHIP CARRIER



8K x 8 Bit CMOS Electrically Erasable PROM

FEATURES

- **Operating Temperature Range**
  - **KM28C64/KM28C65: Commercial**
  - **KM28C64I/KM28C65I: Industrial**
- **Simple Byte Write**
  - **Single TTL Level Write Signal**
  - **Latched Address and Data**
  - **Automatic Write Timing**
  - **Automatic Internal Erase-Before-Write**
  - **Ready/$\overline{\text{Busy}}$ Output Pin (KM28C65)**
  - **$\overline{\text{Data}}$ Polling and Verification**
- **32-byte page Write 5ms (max.)**
  - **Effective 150μs/byte write**
- **Enhanced Write Protection**
- **Single 5 volt Supply**
- **Fast Access Time: 200ns**
- **Power: 100μA—Standby (max)**
  30mA—Operating (max)
- **Two Line Control-Eliminates Bus Contention**
- **10,000 Cycle Endurance**
- **JEDEC Byte-wide Memory Pinput**

GENERAL DESCRIPTION

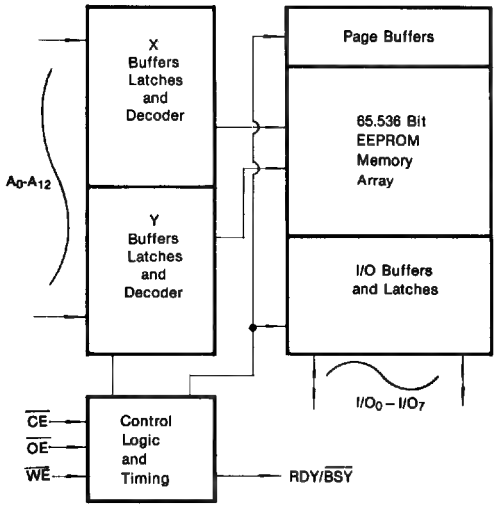
The KM28C64/C65 is a 8,192 x 8 bit Electrically Erasable Programmable Read Only Memory. Its data can be modified using simple TTL level signals and a single 5 volt power supply.

Writing data into the KM28C64/C65 is very simple. The internally self-timed writing cycle latches both address and data to provide a free system bus during the 5ms (max) write period. A 32-byte page write enables an entire chip written in 1.3 second.

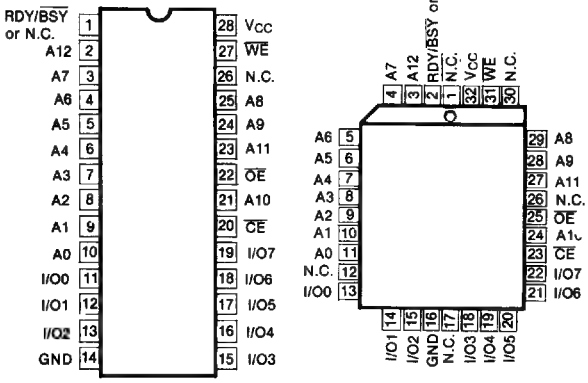
The KM28C64/C65 features $\overline{\text{Data}}$-polling, which enables the EEPROM to signal the processor that a write operation is complete without requiring the use of any external hardware. The KM28C65 features Read/$\overline{\text{Busy}}$ which is a hardware scheme to signal the status of the write operation and is especially useful in interrupt driven systems.

The KM28C64/C65 is fabricated with the well defined floating-gate CMOS technology using Fowler-Nordheim tunneling for erasing and programming.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Pin Name	Pin Function
A_0-A_{12}	Address Inputs
I/O_0-I/O_7	Data Inputs/Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
RDY/$\overline{BSY}$	Ready/$\overline{Busy}$ Output
N.C.	No Connection
V_{CC}	+5V
GND	Ground

ELECTRICAL CHARACTERISTICS

Parameter		Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}		V_{IN}	−0.3 to 7.0	V
Temperature Under Bias	Commercial	T_{bias}	−10 to +85	°C
	Industrial		−65 to +125	°C
Storage Temperature		T_{stg}	−65 to +125	°C
Short Circuit Output Current		I_{OS}	5	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

KM28C64/C65: Voltage reference to V_{SS}, $T_A = 0°C$ to $+70°C$
KM28C64I/C65I: Voltage reference to V_{SS}, $T_A = -40°C$ to $+85°C$

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V
Input High Voltage, all Inputs	V_{IH}	2.0	—	$V_{CC}+0.3$	V
Input Low Voltage, all Inputs	V_{IL}	−0.3	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Operating Current	I_{CC}	$\overline{CE} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$ all I/O's = open all addresses* (NOTE 1)	—	30	mA
Standby Current (TTL)	I_{SB1}	$\overline{CE} = V_{IH}$ all I/O's = open		1	mA
Standby Current (CMOS)	I_{SB2}	$\overline{CE} = V_{CC} - 0.2$ all I/O's = open	—	100	μA
Input Leakage Current	I_{LI}	$V_{IN} = 0$ to 5.5V	—	10	μA
Output Leakage Current	I_{LO}	$V_{OUT} = 0$ to 5.5V	—	10	μA
Output High Voltage Level	V_{OH}	$I_{OH} = -400\mu A$	2.4	—	V
Output Low Voltage Level	V_{OL}	$I_{OL} = 2.1mA$	—	0.4	V
Write Inhibit V_{CC} Level	V_{WI}		3.8	—	V

* Note 1. All addresses toggling from V_{IL} to V_{IH} at 5MHz

CAPACITANCE ($T_A = 25°C$, $V_{CC} = 5V$, f = 1.0 MHz)

Parameter	Symbol	Conditions	Min	Max	Unit
Input/Output Capacitance	$C_{I/O}$	$V_{I/O} = 0V$	—	8	pF
Input Capacitance	C_{IN}	$V_{IN} = 0V$	—	8	pF

Note: Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O	Power
L	L	H	Read	D_{OUT}	Active
L	H	L	Write	D_{IN}	Active
L	L	H	$\overline{DATA}$-Polling	$I/O_7 = \overline{D_7}$	Active
H	X	X	Standby & Write Inhibit	High-Z	Standby
X	L	X	Write Inhibit	—	—
X	X	H	Write Inhibit	—	—

AC CHARACTERISTICS

KM28C64/C65: $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise noted.
KM28C64I/C65I: $T_A = -40°C$ to $+85°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise noted.

TEST CONDITIONS

Parameter	Value
Input Pulse Levels	0.45 to 2.4V
Input Rise and Fall Times	20 ns
Input and Output Timing Levels	0.8V and 2.0V
Output Load	1 TTL Gate and $C_L = 100pF$

READ CYCLE

Parameter	Symbol	KM28C64-20 KM28C64I-20 KM28C65-20 KM28C65I-20		KM28C64-25 KM28C64I-25 KM28C65-25 KM28C65I-25		Unit
		Min	Max	Min	Max	
Read Cycle Time	t_{RC}	200		250		ns
Chip Enable Access Time	t_{CE}		200		250	ns
Address Access Time	t_{AA}		200		250	ns
Output Enable Access Time	t_{OE}		80		100	ns
Output or Chip Disable to Output High-Z	t_{DF}	5	70	5	90	ns
Output Hold from Address Change, Chip Disable, or Output Disable Whichever Occurs First	t_{OH}	10		10		ns

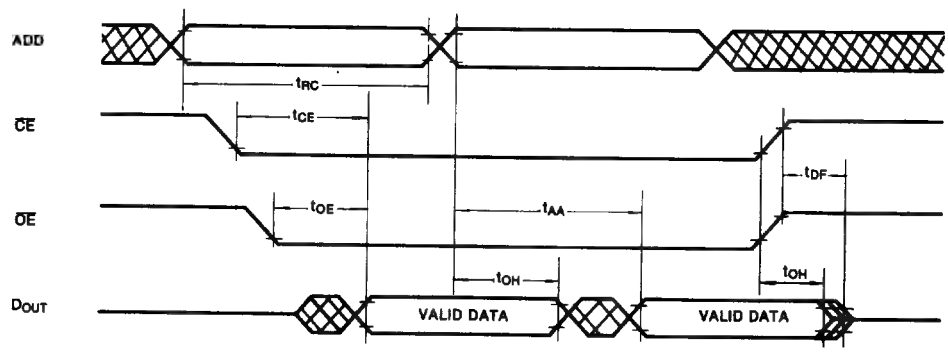
WRITE CYCLE

Parameter	Symbol	Min	Max	Unit
Write Cycle Time	t_{WC}	5		ms
Address Set-Up Time	t_{AS}	0		ns
Address Hold Time	t_{AH}	80		ns
Write Set-Up Time	t_{CS}	0		ns
Write Hold Time	t_{CH}	0		ns
$\overline{CE}$ Pulse Width	t_{CW}	100		ns
Output Enable Set-Up Time	t_{OES}	10		ns
Output Enable Hold Time	t_{OEH}	10		ns
$\overline{WE}$ Pulse Width	t_{WP}	100		ns
Data Set-Up Time	t_{DS}	50		ns
Data Hold Time	t_{DH}	10		ns
Time to Device Busy	t_{DB}		100	ns
Busy to Write Recovery Time	t_{BWR}	50		ns
Byte Load Cycle Time	t_{BLC}	0.2	30	μs
Last Byte Loaded to $\overline{Data}$ Polling	t_{LP}	1		μs

Note: The timer for t_{BLC} is reset at a falling edge of $\overline{WE}$ and starts at a rising edge of $\overline{WE}$.

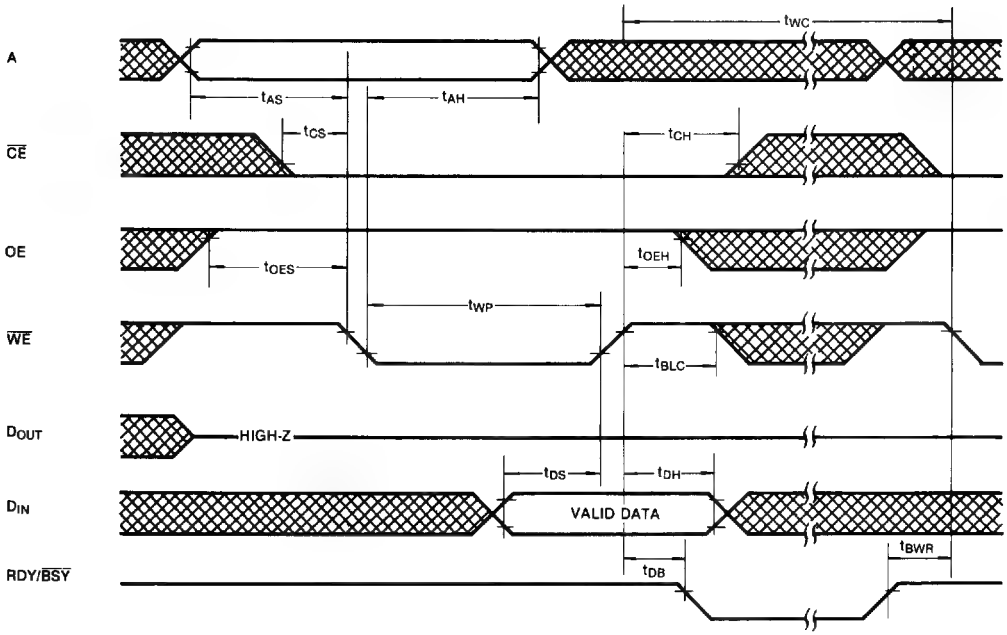
TIMING DIAGRAMS

READ CYCLE $\overline{WE} = V_{IH}$

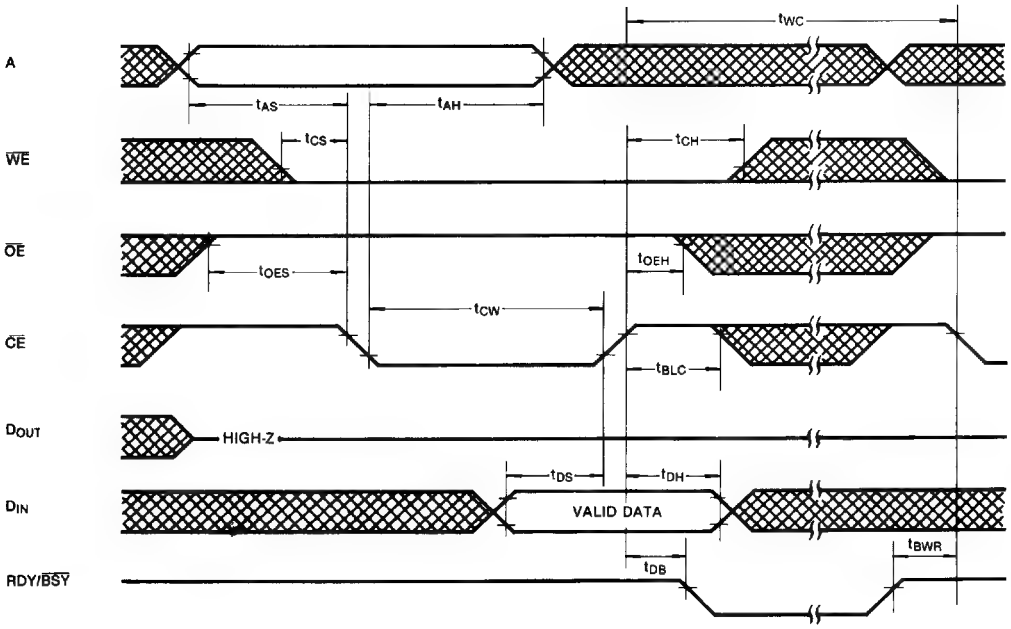


TIMING DIAGRAMS (Continued)

$\overline{WE}$ CONTROLLED WRITE CYCLE

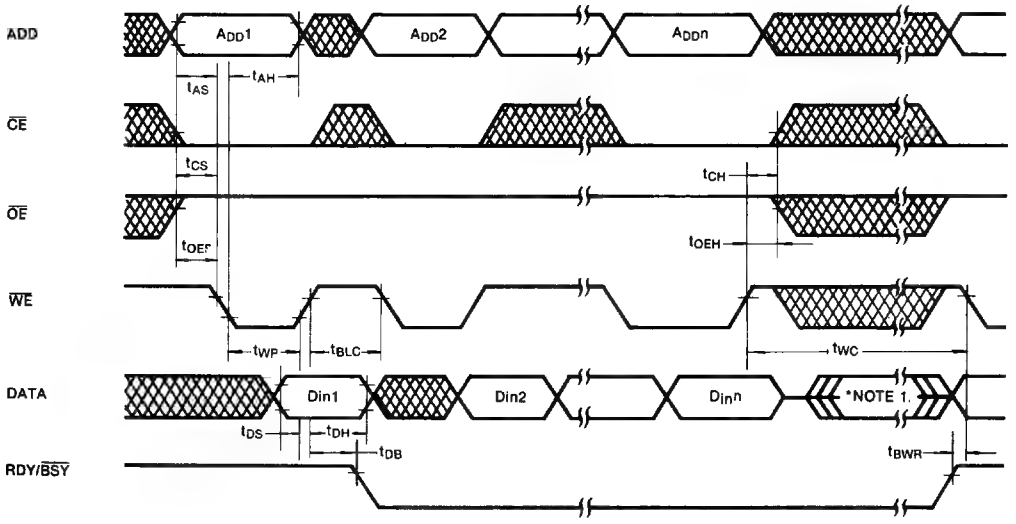


$\overline{CE}$ CONTROLLED WRITE CYCLE

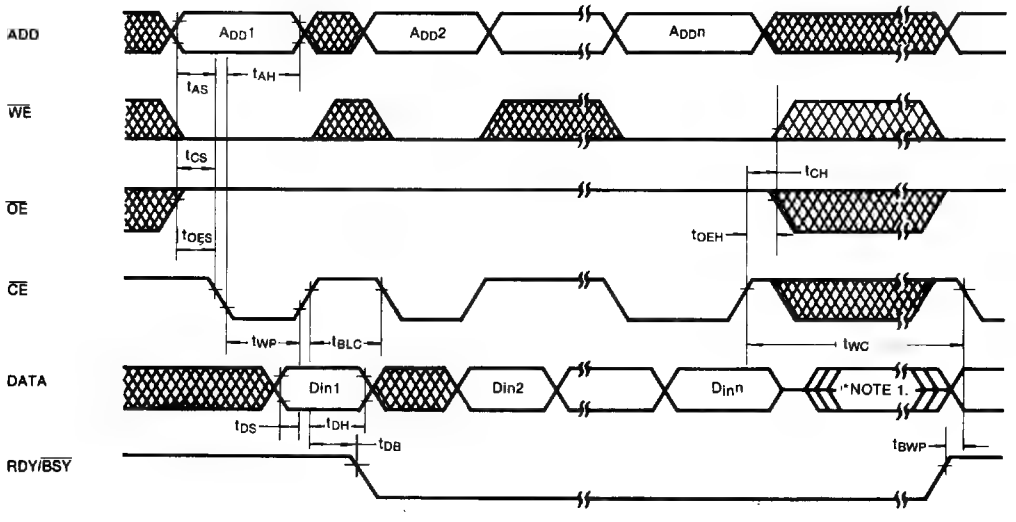


TIMING DIAGRAMS (Continued)

PAGE MODE WRITE ($\overline{WE}$ CONTROLLED WRITE CYCLE)



PAGE MODE WRITE ($\overline{CE}$ CONTROLLED WRITE CYCLE)



*NOTE 1. I/O_7 Outputs $D_{IN}n$ when the chip is read.
I/O_0-I/O_6 have tristate.

DEVICE OPERATION

READ

Reading data from the KM28C64/C65 is similar to reading data from a SRAM. A read cycle occurs when $\overline{WE}$ is high and $\overline{CE}$ and $\overline{OE}$ are low. If either $\overline{CE}$ or $\overline{OE}$ goes high the read cycle is terminated. This two line control eliminates bus contention in a system environment. The Data I/O pins are in the high impedance state whenever $\overline{OE}$ or $\overline{CE}$ is high.

WRITE

Writing data into the KM28C64/C65 is easy. Only a single 5V supply and TTL level signals are required. The on-chip data latches, address latches, high voltage generator, and fully self-timed control logic make writing as easy as writing to a SRAM.

**** BYTE WRITE MODE ****

The byte write mode of the KM28C64/C65 is only a part of the page write mode. A single byte data loading followed by a t_{BLC} time-out and by a nonvolatile write cycle will complete a byte mode written. In this mode, the write is exactly identical to that of the KM2864A/65A.

**** PAGE WRITE MODE ****

The KM28C64/C65 allows up to 32 byte to be written in a single page write cycle. A page write cycle consists of a data loading period, in which from 1 to 32 byte data are loaded into the KM28C64/C65 internal registers and a nonvolatile write period, in which the loaded data in the registers are written to the EEPROM cells of the selected page.

Data are loaded into the KM28C64/C65 by sequentially pulsing $\overline{WE}$ with $\overline{CE}$ low and $\overline{OE}$ high. On each $\overline{WE}$, address is latched on the falling edge of the $\overline{WE}$ and data is latched on the rising edge of the $\overline{WE}$. The data can be loaded in any "Y" address order and can be renewed in a data loading period.

Since the timer for the data loading period (t_{BLC}) is reset at the falling edge of $\overline{WE}$ and starts at every rising edge of $\overline{WE}$, the only requirement on $\overline{WE}$ to continue the data loading is that the interval between $\overline{WE}$ pulses does not exceed the maximum t_{BLC} (30μs). If $\overline{OE}$ goes Low during the data loading period, further attempt to load the data will be ignored because the external $\overline{WE}$ signal is blocked by $\overline{OE}$ signal internally. Consequently, the t_{BLC} timer is not reset by the external $\overline{WE}$ pulse if $\overline{OE}$ is low.

The page address for the nonvolatile write is the "X" address (A_5-A_{12}) latched on the last $\overline{WE}$. The nonvolatile write period consists of an erase cycle and a program cycle. During the erase cycle, the existing data of the locations being addressed are erased. The new data latched at the register are written into the locations during the program cycle. Note that only the addressed location in a page are rewritten during a page write cycle.

The KM28C64/C65 also supports $\overline{CE}$ controlled write cycle. That means $\overline{CE}$ can be used to latch address and data as well as $\overline{WE}$.

STANDBY

Power consumption is reduced to less than 100μA by deselecting the device with a high input on $\overline{CE}$. Whenever $\overline{CE}$ is high, the device is in the standby mode and I/O_0-I/O_7 are in the high impedance state, regardless of the state of $\overline{OE}$ or $\overline{WE}$.

DATA PROTECTION

Features have been designed into the KM28C64/C65 that prevent unwanted write cycles during power supply transitions and system noise periods.

The KM28C64/C65 has a protection feature against $\overline{WE}$ noises: a $\overline{WE}$ noise the width shorter than 20ns (typ.) will not start any unwanted write cycle.
Write cycles are also inhibited when V_{CC} is less than $V_{WI} = 3.8$ volts, the Write Inhibits V_{CC} level.
During power-up, the KM28C64/C65 automatically prevents any write operation for a period of 5ms (typ.) after V_{CC} reaches the V_{WI} level. This will provide the system with sufficient time to bring $\overline{WE}$ and $\overline{CE}$ to a high level before a write can occur. Read cycles can be executed during this initialization period. Holding either $\overline{OE}$ low or $\overline{WE}$ high or CE high during power-on and power-off will inhibit inadvertent writes.

$\overline{DATA}$ POLLING

The KM28C64/C65 features $\overline{DATA}$-Polling at I/O_7 to detect the completion of a write cycle using a simple read and compare operation. Such a scheme does not require any external hardware. Reading the device at any time during a write operation will produce, at I/O_7, an inverted value of last data loaded into the EEPROM (I/O_0-I/O_6 are at the high impedance state). True data will be produced at all I/O's once the write cycle has been completed.

DEVICE OPERATION (Continued)

READY/$\overline{BUSY}$

The KM28C65 has a Ready/$\overline{Busy}$ output on pin 1 that indicates when the write cycle is complete. The pin is normally high except when a write cycle is in progress, in which case the pin is low.

The Ready/$\overline{Busy}$ output is configured as open-drain driver there-by allowing two or more Ready/$\overline{Busy}$ output to be OR-tied. This pin requires an appropriate pull-up resistor for proper operation. The pull-up resistor value maybe calculated as follows.

$$RP = \frac{V_{CC}(max) - V_{OL}(max)}{I_{OL} + I_L} = \frac{5.1V}{2.1mA + I_L}$$

where I_L is the sum of the input currents of all devices tied to the Ready/$\overline{Busy}$ pin.

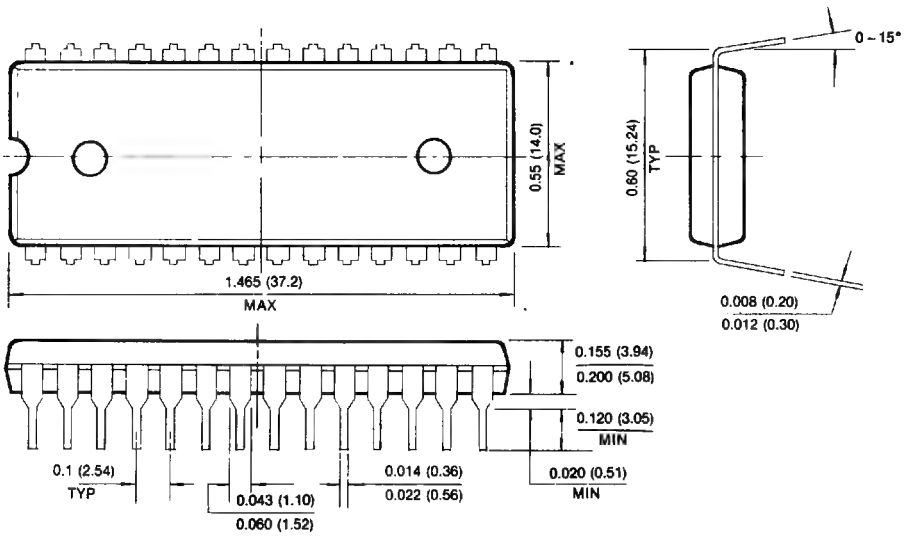
ENDURANCE AND DATA RETENTION

KM28C64/C65 is designed for applications requiring up to 10,000 write cycles per EEPROM byte and ten years of data retention. This means that each byte may be reliably written 10,000 times without degrading device operation and that the data in the byte will remain valid after its last write operation for ten years with or without power applied.

PACKAGE DIMENSIONS

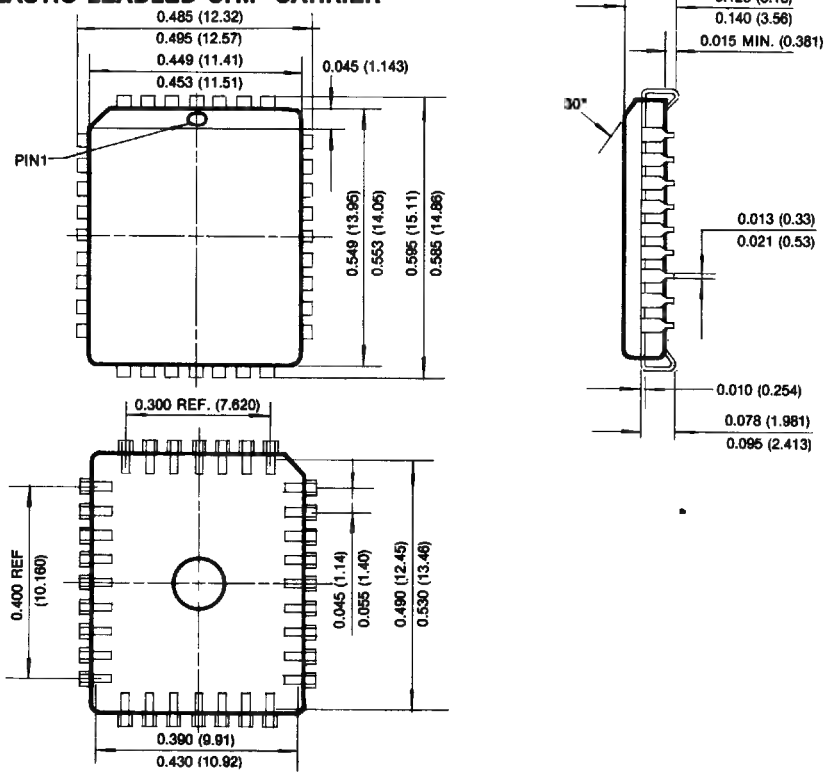
28 LEAD PLASTIC DUAL IN LINE PACKAGE

Units: Inches (millimeters)



PACKAGE DIMENSIONS (Continued)

32 PIN PLASTIC LEADLED CHIP CARRIER



4

32K×8 Bit CMOS Electrically Erasable PROM

FEATURES

- **Operating Temperature Range**
  - **— KM28C256: Commercial**
  - **— KM28C256I: Industrial**
- **Simple Byte Write**
  - **— Single TTL Level Write Signal**
  - **— Latched Address and Data**
  - **— Automatic Write Timing**
  - **— Automatic Internal Erase-Before-Write**
- **64-byte page Write 5ms (max.)**
- **Data Polling and Toggle bit**
- **Single 5 volt Supply**
- **Fast Access Time: 150ns**
- **Power: 100μA—Standby (max)**
  60mA—Operating (max)
- **Hardware and Software Data Protection**
- **Reliable CMOS Floating—Gate Technology**
  - **— Endurance: 100,000 or 10,000 cycles**
  - **— Data Retention: 10 years**

GENERAL DESCRIPTION

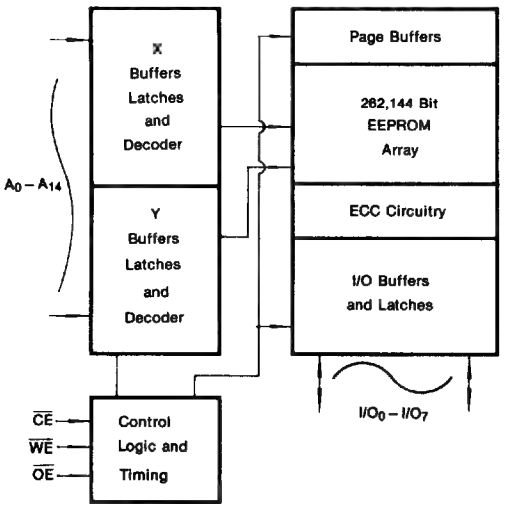
The KM28C256 is a 32,768×8 bit Electrically Erasable Programmable Read Only Memory. It is fabricated with the floating-gate CMOS technology using Fowler-Nordheim tunneling for erasing and programming.

Writing data into the KM28C256 is very simple. The internally self-timed writing cycle latches both address and data to provide a free system bus during the 5ms (max) write period. A 64-byte page write enables an entire chip written in 2.5 second.

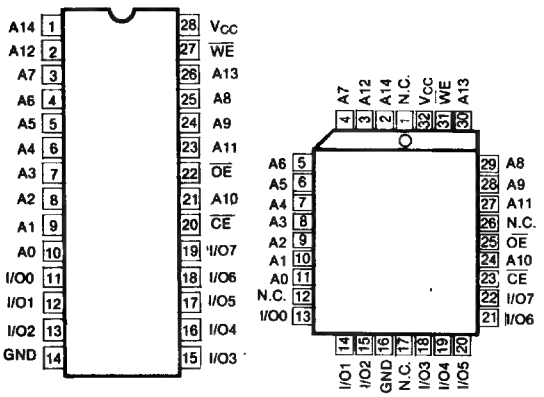
The KM28C256 is also features $\overline{\text{data}}$ polling and toggle bit scheme that signal the processor the completion of a write cycle without requiring use of any external hardware.

The KM28C256 is designed for applications up to 100,000 write cycles per byte. Its on-chip ECC renders the chip endure over 100,000 write cycles without failure.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Pin Name	Pin Function
A_0-A_{14}	Address Inputs
I/O_0-I/O_7	Data Inputs/Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
N.C.	No Connection
V_{CC}	+5V
GND	Ground

ABSOLUTE MAXIMUM RATINGS*

Parameter		Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}		V_{IN}	−0.3 to 7.0	V
Temperature Under Bias	Commercial	T_{bias}	−10 to +85	°C
	Industrial		−65 to +125	°C
Storage Temperature		T_{stg}	−65 to +125	°C
Short Circuit Output Current		I_{OS}	5	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

KM28C256: Voltage reference to V_{SS}, $T_A = 0°C$ to $+70°C$
KM28C256I: Voltage reference to V_{SS}, $T_A = -40°C$ to $+85°C$

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V
Input High Voltage, all Inputs	V_{IH}	2.0	—	$V_{CC}+0.3$	V
Input Low Voltage, all Inputs	V_{IL}	−0.3	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Operating Current	I_{CC}	$\overline{CE} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$ all I/O's = open all addresses* (NOTE 1)	—	60	mA
Standby Current (TTL)	I_{SB1}	$\overline{CE} = V_{IH}$ all I/O's = open	—	1	mA
Standby Current (CMOS)	I_{SB2}	$\overline{CE} = V_{CC} - 0.2$ all I/O's = open	—	100	μA
Input Leakage Current	I_{LI}	$V_{IN} = 0$ to 5.5V	—	1	μA
Output Leakage Current	I_{LO}	$V_{OUT} = 0$ to 5.5V	—	1	μA
Output High Voltage Level	V_{OH}	$I_{OH} = -400\mu A$	2.4	—	V
Output Low Voltage Level	V_{OL}	$I_{OL} = 2.1mA$	—	0.4	V
Write Inhibit V_{CC} Level	V_{WI}		3.8	—	V

* Note 1. All addresses toggling from V_{IL} to V_{IH} at 6.7MHz

CAPACITANCE ($T_A = 25°C$, $V_{CC} = 5V$, f = 1.0 MHz)

Parameter	Symbol	Conditions	Min	Max	Unit
Input/Output Capacitance	$C_{I/O}$	$V_{I/O} = 0V$	—	6	pF
Input Capacitance	C_{IN}	$V_{IN} = 0V$	—	6	pF

Note: Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O	Power
L	L	H	Read	D_{OUT}	Active
L	H	L	Write	D_{IN}	Active
L	L	H	$\overline{DATA}$-Polling	$I/O_7 = \overline{D}_7$	Active
H	X	X	Standby & Write Inhibit	High-Z	Standby
L	L	H	Toggle Bit	I/O_6	Active
X	L	X	Write Inhibit	—	—
X	X	H	Write Inhibit	—	—

AC CHARACTERISTICS

KM28C256: $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise noted.
KM28C256I: $T_A = -40°C$ to $+85°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise noted.

TEST CONDITIONS

Parameter	Value
Input Pulse Levels	0.45 to 2.4V
Input Rise and Fall Times	20 ns
Input and Output Timing Levels	0.8V and 2.0V
Output Load	1 TTL Gate and $C_L = 100pF$

READ CYCLE

Parameter	Symbol	KM28C256-15 KM28C256I-15		KM28C256-20 KM28C256I-20		KM28C256-25 KM28C256I-25		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	150		200		250		ns
Chip Enable Access Time	t_{CE}		150		200		250	ns
Address Access Time	t_{AA}		150		200		250	ns
Output Enable Access Time	t_{OE}		80		100		120	ns
Output or Chip Disable to Output High-Z	t_{DF}	5	50	5	60	5	70	ns
Output Hold from Address Change, Chip Disable, or Output Disable Whichever Occurs First	t_{OH}	0		0		0		ns

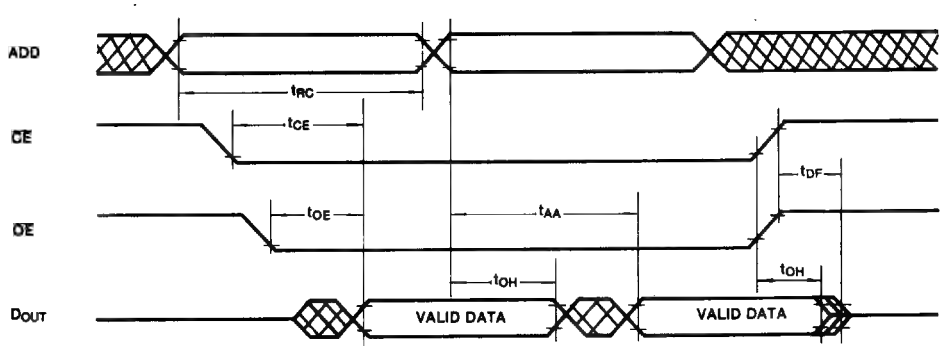
WRITE CYCLE

Parameter	Symbol	Min	Max	Unit
Write Cycle Time	t_{WC}	5		ms
Address Set-Up Time	t_{AS}	0		ns
Address Hold Time	t_{AH}	80		ns
Write Set-Up Time	t_{CS}	0		ns
Write Hold Time	t_{CH}	0		ns
$\overline{CE}$ Pulse Width	t_{CW}	100		ns
Output Enable Set-Up Time	t_{OES}	10		ns
Output Enable Hold Time	t_{OEH}	10		ns
$\overline{WE}$ Pulse Width	t_{WP}	100		ns
Data Set-Up Time	t_{DS}	50		ns
Data Hold Time	t_{DH}	0		ns
Byte Load Cycle Time	t_{BLC}	0.2	150	μs
Last Byte Loaded to Data Polling	t_{LP}	1		μs

Note: The timer for t_{BLC} is reset at a falling edge of $\overline{WE}$ and starts at a rising edge of $\overline{WE}$.

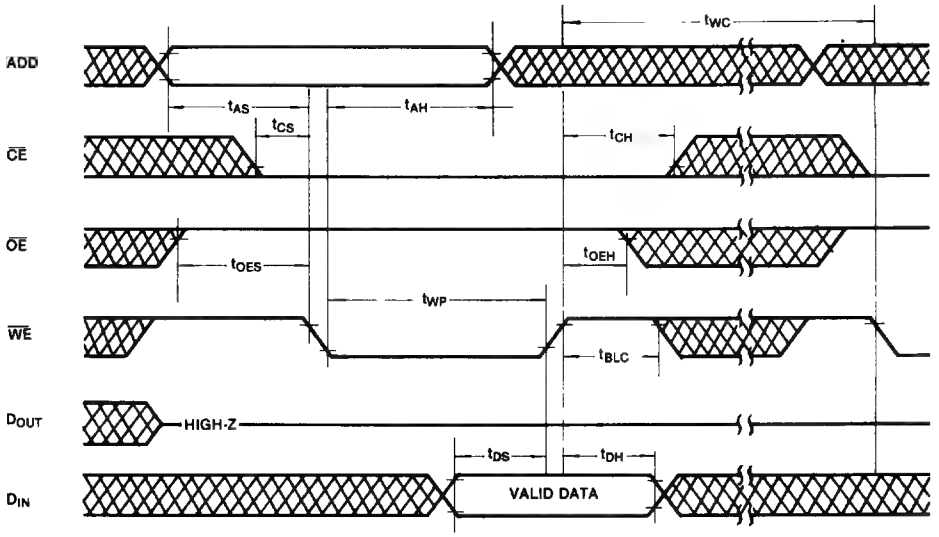
TIMING DIAGRAMS

READ CYCLE WE = V_{IH}

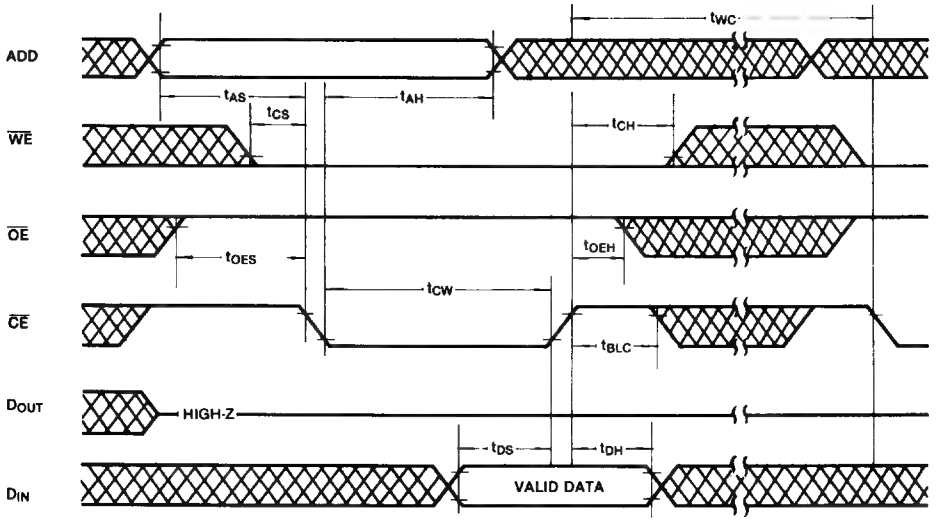


TIMING DIAGRAMS (Continued)

$\overline{WE}$ CONTROLLED WRITE CYCLE

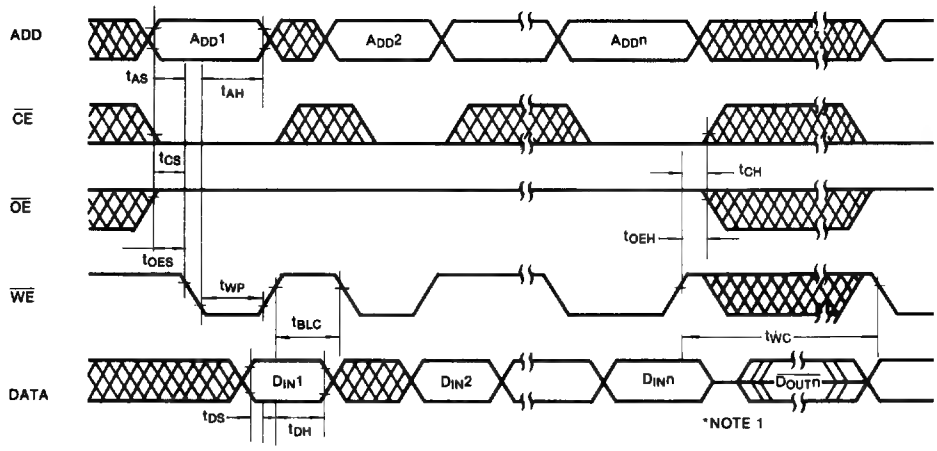


$\overline{CE}$ CONTROLLED WRITE CYCLE

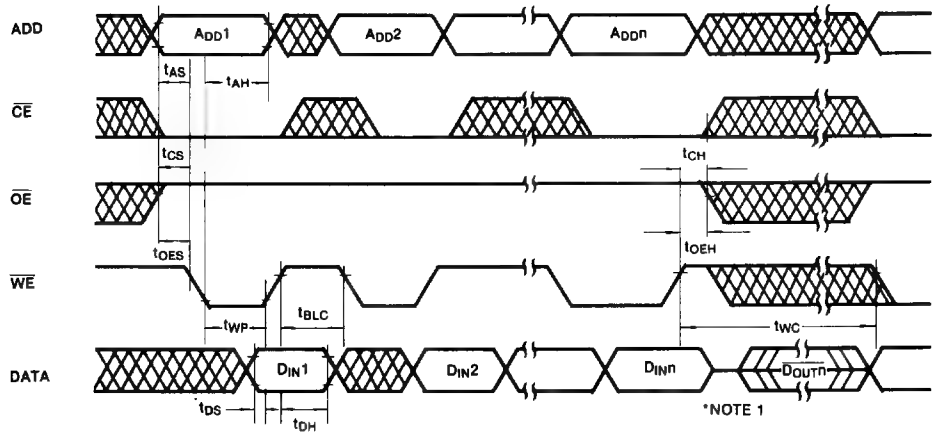


TIMING DIAGRAMS (Continued)

PAGE MODE WRITE ($\overline{WE}$ CONTROLLED WRITE CYCLE)



PAGE MODE WRITE ($\overline{CE}$ CONTROLLED WRITE CYCLE)



*NOTE 1. I/O_7 Outputs $\overline{D_{INn}}$ when the chip is read.
I/O_0-I/O_6 have tristate.

DEVICE OPERATION

READ

Reading data from the KM28C256 is similar to reading data from a SRAM. A read cycle occurs when $\overline{WE}$ is high and $\overline{CE}$ and $\overline{OE}$ are low. If either $\overline{CE}$ or $\overline{OE}$ goes high a read cycle is terminated. This two line control eliminates bus contention in a system environment. The Data I/O pins are in the high impedance state whenever $\overline{OE}$ or $\overline{CE}$ is high.

STANDBY

Current consumption is reduced to less than 100μA by deselecting the device with a high input on $\overline{CE}$. Whenever $\overline{CE}$ is high, the device is in the standby mode and I/O_0-I/O_7 are in the high impedance state, regardless of the state of $\overline{OE}$ or $\overline{WE}$.

WRITE

Writing data into the KM28C256 is easy. Only a single 5V supply and TTL level signals are required. The on-chip data latches, address latches, high voltage generator, and fully self-timed control logic make writing as easy as writing to a SRAM.

**** BYTE WRITE MODE ****

The byte write mode of the KM28C256 is only a part of the page write mode. A single byte data loading followed by a t_{BLC} time-out and by a nonvolatile write cycle will complete a byte mode write.

**** PAGE WRITE MODE ****

The KM28C256 allows up to 64 byte to be written in a single page write cycle. A page write cycle consists of a data loading period, in which from 1 to 64 byte data are loaded into the KM28C256 internal registers and a nonvolatile write period, in which the loaded data in the registers is written to the EEPROM cells of the selected page.

Data are loaded into the KM28C256 by sequentially pulsing $\overline{WE}$ with $\overline{CE}$ low and $\overline{OE}$ high. On each $\overline{WE}$, address is latched on the falling edge of the $\overline{WE}$ and data is latched on the rising edge of the $\overline{WE}$. The data can be loaded in any "Y" address order and can be renewed in a data loading period.

Since the timer for the data loading period (t_{BLC}) is reset at the falling edge of $\overline{WE}$ and starts at every rising edge of $\overline{WE}$, the only requirement on $\overline{WE}$ to continue the data loading is that the interval between $\overline{WE}$ pulses does not exceed the maximum t_{BLC} (150μs). If $\overline{OE}$ goes Low during the data loading period, further attempt to load the data will be ignored because the external $\overline{WE}$ signal is blocked by $\overline{OE}$ signal internally. Consequently, the t_{BLC} timer is not reset by the external $\overline{WE}$ pulse if $\overline{OE}$ is low.

The nonvolatile write starts if $\overline{WE}$ stay high for at least t_{BLC} maximum (150ns) after the last $\overline{WE}$ low to high transition. The page address for the nonvolatile write is the "X" address (A_6-A_{14}) latched on the last $\overline{WE}$. The nonvolatile write period consists of an erase cycle and a program cycle. During the erase cycle, the existing data of the locations being addressed during the loading period are erased. The new data latched at the register are written into the locations during the program cycle. Note that only the addressed location in a page are rewritten during a page write cycle.

The KM28C256 also supports $\overline{CE}$ controlled write cycle. That means $\overline{CE}$ can be used to latch address and data as well as $\overline{WE}$.

DATA PROTECTION

Features have been designed into the KM28C256 that prevent unwanted write cycles during power supply transitions and system noise periods.

The KM28C256 has a protection feature against $\overline{WE}$ noises a $\overline{WE}$ noise the width of which shorter than 20ns (typ.) will not start any unwanted write cycle. Write cycles are also inhibited when V_{CC} is less than V_{WI}, the write inhibit V_{CC} level. During power-up, the KM28C256 automatically prevents any write operation for a period of 5ms (max.) after V_{CC} reaches the V_{WI} level. This will protect the chip from a false write during power up transient. Read cycles can be executed during this initialization period. Holding either $\overline{OE}$ low or $\overline{WE}$ high or $\overline{CE}$ high during power-on and power-off will inhibit inadvertent writes.

**** SOFTWARE DATA PROTECTION ****

The KM28C256 has the JEDEC standard software data protection scheme for enhanced protection of stored data.

The scheme does not affect normal write operation if it is not enabled through a SDP enable software algorithm. The protection mode can be enabled by excuting a short SDP enable software algorithm, followed by a write operation, either a single byte write or page write operation. Once the protection mode is enabled, the KM28C256 will not write any data if the SDP enable software algorithm is not proceded. The data protection function can be disabled by excuting a SDP disable software algorithm. All the data and address timings for the SDP enable and disable are identical to those of a page write cycle.

**** Programmable Write Inhibit V_{CC} Level ****

Although V_{WI} is set at 3.8V initially, the write inhibit level is electrically programmable in the range of 3V to 4.5V. The nonvolatile V_{WI} adjustment uses Samsung's 4-cell EE Fuse and is reprogrammable.

DEVICE OPERATION

$\overline{\text{DATA}}$ POLLING

The KM28C256 features $\overline{\text{DATA}}$-Polling at I/O_7 to detect the completion of a write cycle using a simple read and compare operation. Such a scheme does not require any external hardware. During the write period, any attempt to read the EEPROM will produce, at I/O_7, an inverted data of the last data loaded in to the EEPROM. True data will be produced at all I/O's, once the write cycle has been completed.

**** TOGGLE BIT ****

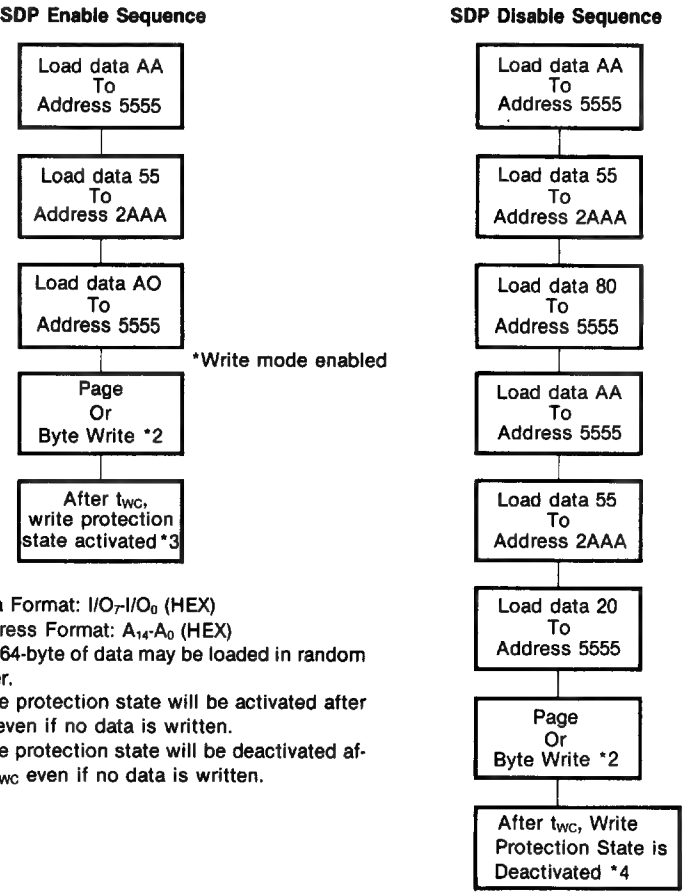
The KM28C256 also provides toggle bit at I/O_6 to determine the end of a write cycle. During the write cycle, subsequent attempts to read the EEPROM will toggle I/O_6 from '1' to '0' and '0' to '1'. Once the write cycle is complete, the toggling will stop and valid data will be read.

ENDURANCE AND DATA RETENTION

The KM28C256 is designed for applications requiring up to 100,000 write cycles per byte and ten years of data retention. This means that each byte can be reliably written 100,000 times without degrading device operation, and that the features an on-chip Error Checking and Correction scheme that can detect and correct any single bit failure in a byte. And hence, significant improvements in the endurance and data retention characteristics are achieved.

4

SOFTWARE DATA PROTECTION ALGORITHM

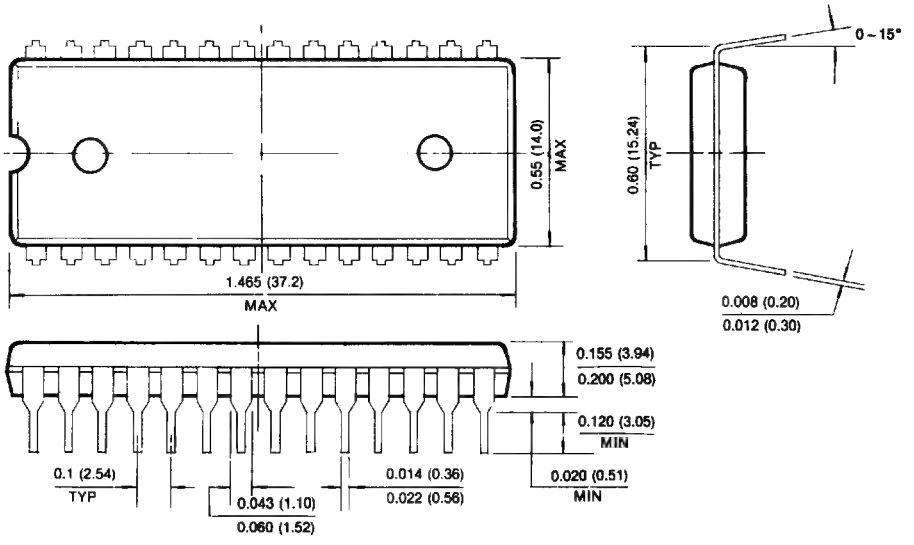


Notes 1. Data Format: I/O_7-I/O_0 (HEX)
Address Format: A_{14}-A_0 (HEX)
2. 1 to 64-byte of data may be loaded in random order.
3. Write protection state will be activated after t_{WC} even if no data is written.
4. Write protection state will be deactivated after t_{WC} even if no data is written.

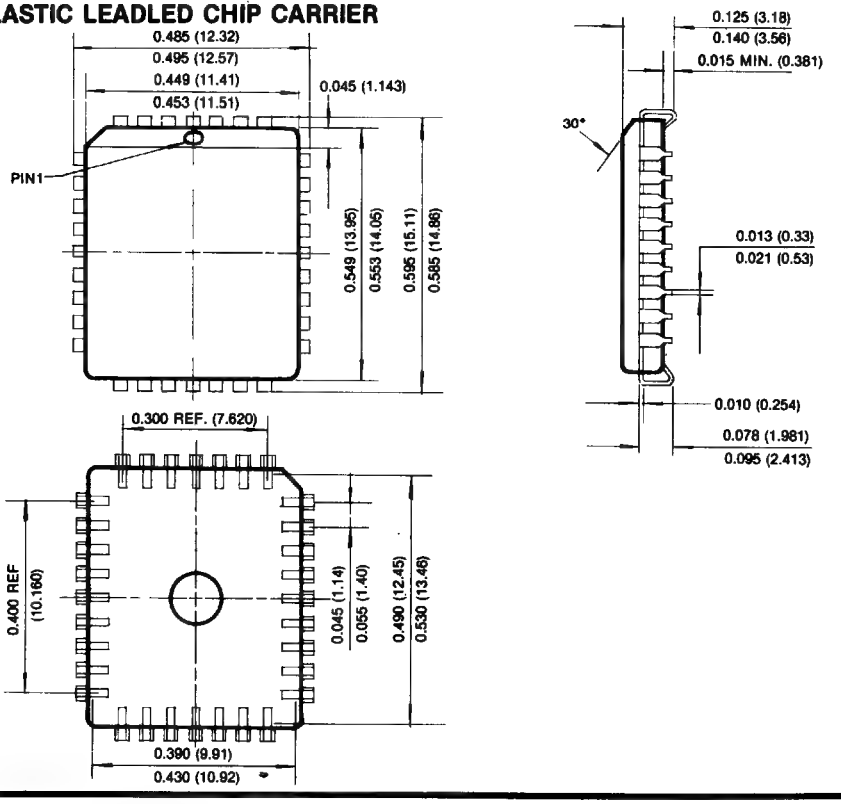
PACKAGE DIMENSIONS

28 LEAD PLASTIC DUAL IN LINE PACKAGE

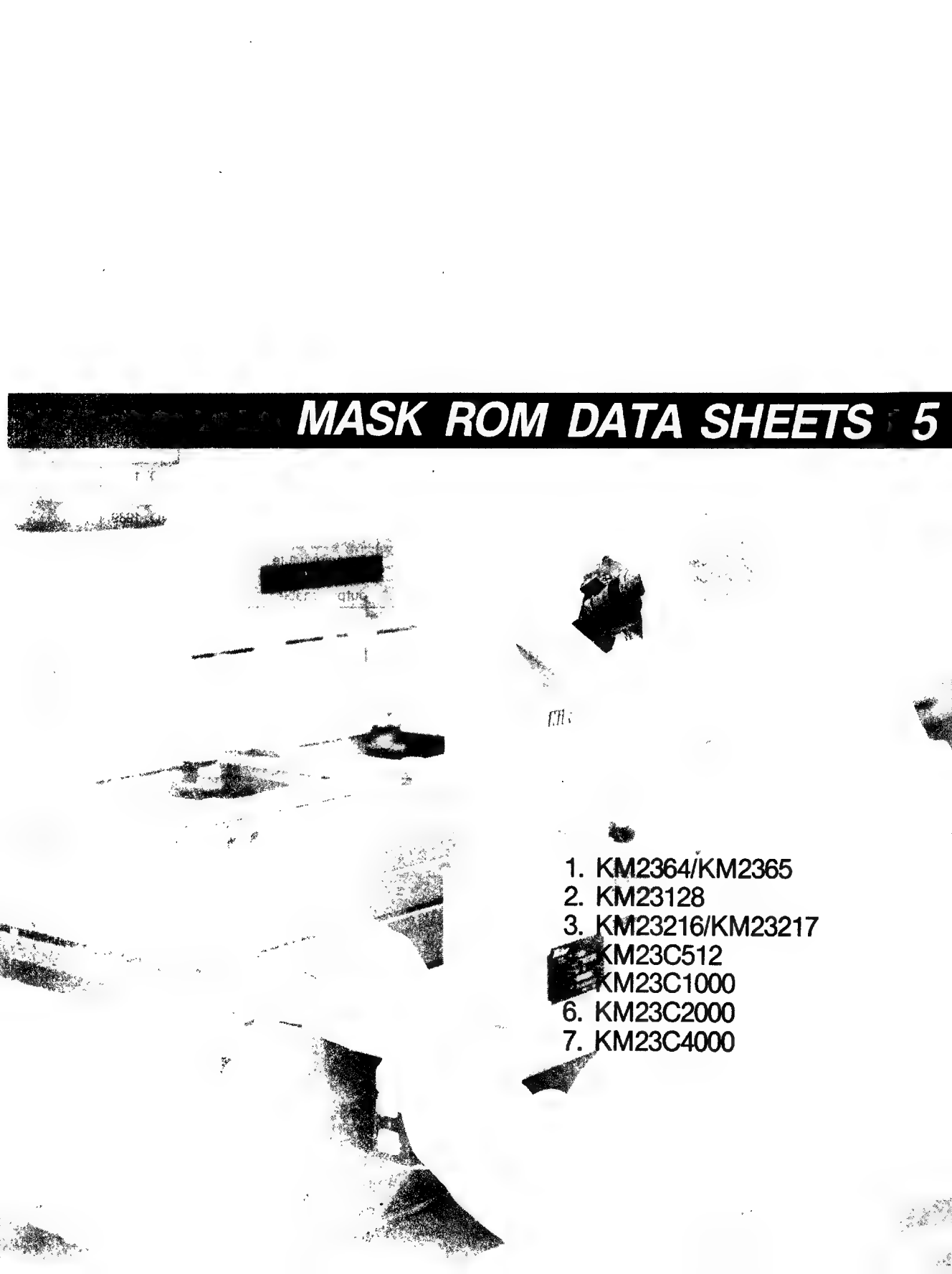
Units: Inches (millimeters)



32 PIN PLASTIC LEADLED CHIP CARRIER



MASK ROM DATA SHEETS 5



1. KM2364/KM2365
2. KM23128
3. KM23216/KM23217
4. KM23C512
5. KM23C1000
6. KM23C2000
7. KM23C4000

Mask ROM

Capacity	Part Number	Organization	Speed (ns)	Technology	Features	Packages	Remark
6K bit	KM2364	8K×8	250	NMOS	—	24 DIP	
	KM2365	8K×8	250	NMOS	Programmable chip select	28 DIP	Now
128K bit	KM23128	16K×8	250	NMOS	Programmable chip select	28 DIP	Now
256K bit	KM23256	32K×8	250	NMOS	Programmable chip select	28 DIP	Now
	KM23257	32K×8	250	NMOS	Programmable chip select	28 DIP	Now
512K bit	KM23C512	64K×8	250	CMOS	Programmable output enable	28 DIP	4Q, 1989
1M bit	KM23C1000	128K×8	200	CMOS	Programmable chip select	28 DIP	4Q, 1989
4M bit	KM23C4000-15	512K×8	150	CMOS	Programmable	28 DIP	4Q, 1989
	KM23C4000-20	512K×8	200	CMOS	chip select &	28 DIP	4Q, 1989
	KM23C4000-25	512K×8	250	CMOS	output enable	28 DIP	4Q, 1989

8K x 8 Bit Mask ROM

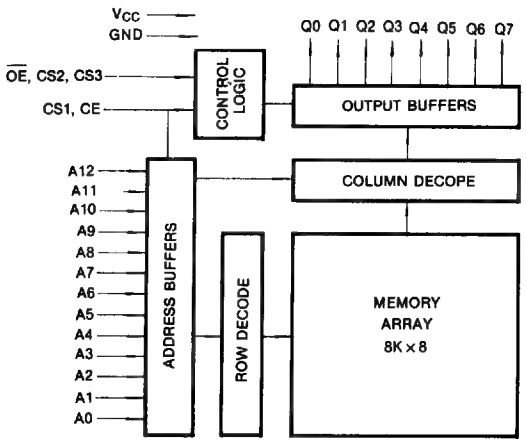
FEATURES

- **2364/65: Non-power down**
- **2364S/65S: Automatic power down**
- **Fully static operation**
- **Silicon gate NMOS technology**
- **Maximum access time**
  2364/65-20: 200 ns
  2364/65-25: 250 ns
  2364/65-30: 300 ns
- **Programmable chip selects**
- **3-State outputs**
- **Fully TTL compatible**
- **Single ±10% 5 volt supply**
- **Pin compatible with 2564 EPROM's**
- **Available in 3 temperature ranges**
  2364/65 (Commercial): 0°C to 70°C
  2364I/65I (Industrial): −40°C to 85°C
  2364HR/65HR (Military): −55°C to 125°C

GENERAL DESCRIPTION

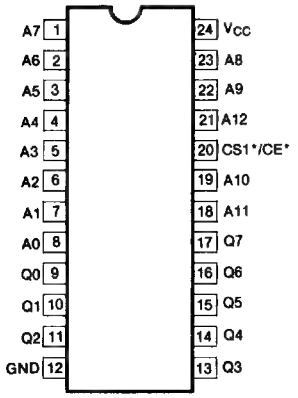
The KM2365/65 are mask programmable read only memories with 8K word by 8 bit organizations. Designed for ease of use, these devices require only a 5-volt supply, are TTL compatible, and because of their totally static (asynchronous) operation require no clock. These memory devices are available in two versions. The 2364/65 are non-power down versions where the active level of chip selects CS1 (on the 2364), and CS2 and CS3 (on the 2365) are programmable and defined by the user to facilitate system memory expansion. The 2364S and 2365S are standby versions offering an automatic power-down feature controlled by the chip enable CE input. When CE goes high, the device automatically powers down and remains in a low power standby mode as long as CE remains high. Also to provide easier system implementation, the active level of chip enable CE (on the 2364S), and chip selects CS2 and CS3 (on the 2365S) is programmable. The KM2364 is packaged in a 24 pin DIP, and the 2365 is packaged in a 28 pin DIP, both with industry standard byte-wide JEDEC pin-outs. Optionally, the 2365 is available in a space saving 28 pin surface mounted plastic leaded chip carrier.

FUNCTIONAL BLOCK DIAGRAM

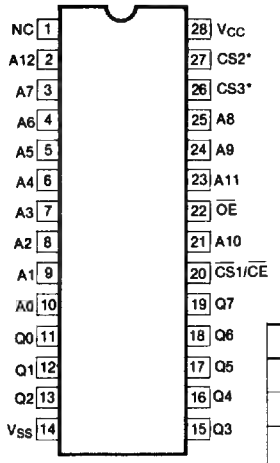


PIN CONFIGURATION

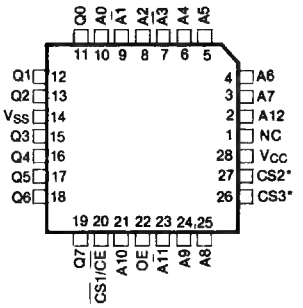
KM2364/S



KM2365/S



*Active Level (Hi, Low or Don't Care) defined by user.



Pin Name	Pin Function
A_0-A_{12}	Address Inputs
Q_0-Q_7	Data Outputs
CS1, $\overline{CS1}$ CS2, CS3	Programmable Chip Select
CE, $\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
V_{CC}	5V ± 10% Supply Voltage

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Voltage on Any Pin with Respect to Ground	V_{CC}	−0.5 to +7V	V
Storage Temperature	T_{stg}	−65 to +150	°C

Stresses above "absolute maximum ratings" may result in damage to the device. Functional operation of devices at the "absolute maximum ratings" or above the recommended operating conditions stipulated elsewhere in this specification is not implied.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	KM2364/65			KM2364I/65I			KM2364HR/65HR			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Supply Voltage*	V_{CC}	4.5	5.0	5.5	4.5	5.0	5.5	4.5	5.0	5.5	Volts
Input High Level Voltage	V_{IH}	2.0		V_{CC}	2.0		V_{CC}	2.2		V_{CC}	Volts
Input Low Level Voltage	V_{IL}	−0.5		0.8	−0.5		0.8	−0.5		0.8	Volts
Operating Ambient Temperature	T_A	0		70	−40		85	−55		125	°C

*V_{CC} must be applied at least 100μs before proper device operation is achieved.

STATIC ELECTRICAL CHARACTERISTICS OVER RECOMMENDED OPERATING CONDITIONS (UNLESS OTHERWISE NOTED)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Input Leakage Current	I_{IN}	V_{IN} = 0V to V_{CC} max			10	μA
Output Leakage Current	I_O	V_O = 0.2 to V_{CC} max Chip Deselected			± 10	μA
Output High Voltage	V_{OH}	I_{OH} = −200μA	2.4			Volts
Output Low Voltage	V_{OL}	I_{OL} = 3.2mA			0.4	Volts
Supply Current-Active	I_{CC}	Outputs Open			60	mA
Supply Current-Standby	I_{SB}*	Chip Deselected			10	μA

*Applies to KM2364S/65S Power Down Versions only.

5

CAPACITANCE (Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Input Capacitance	C_{IN}	All pins except pin under test are tied to ground			7	pF
Output Capacitance	C_O				12.5	pF

Notes: Characteristics are the same for all Operating Temperature Ranges.

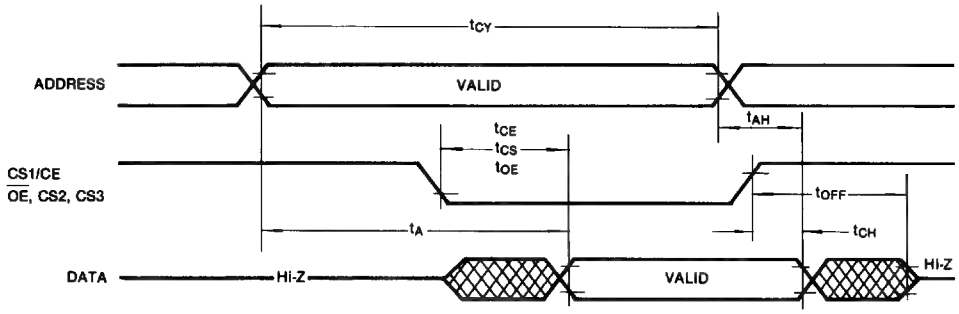
AC CHARACTERISTICS

AC CHARACTERISTICS OVER RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	2364/65-20, 2364I/65I-20, 2364HR/65HR-20		2364/65-25, 2364I/65I-25, 2364HR/65HR-25		2364/65-30, 2364I/65I-35, 2364HR/65HR-30		Units
		Min	Max	Min	Max	Min	Max	
Cycle Time	t_{CY}	200			250		300	ns
Address Access Time	t_A		300	200		250		ns
Chip Enable Access Time	t_{CE}	200			250		300	ns
Chip Select Access Time	t_{CS}		150	100		120		ns
Chip Select to Data Off (Hi Z)	t_{OFF}		150	100		120		ns
Data Hold Time from Control	t_{CH}	0			0		0	ns
Data Hold Time from Address	t_{AH}	0				0		ns

TIMING DIAGRAMS

AC WAVEFORMS

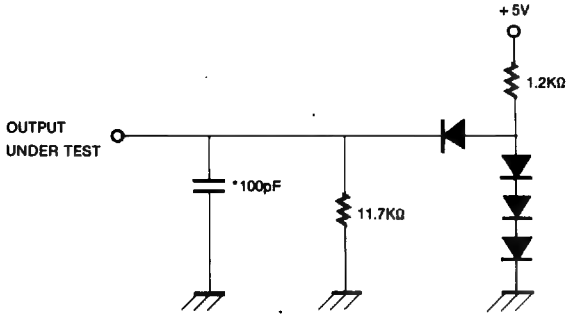


The chip select line is assumed to be active low.

AC CONDITION OF TESTS

Input Pulse Levels ..... 0.8 Volts to 2.0 Volts
Input Rise & Fall Times ..... 10 ns
Output Timing Levels ..... 0.8 Volts to 2.0 Volts

AC TEST LOAD CIRCUIT

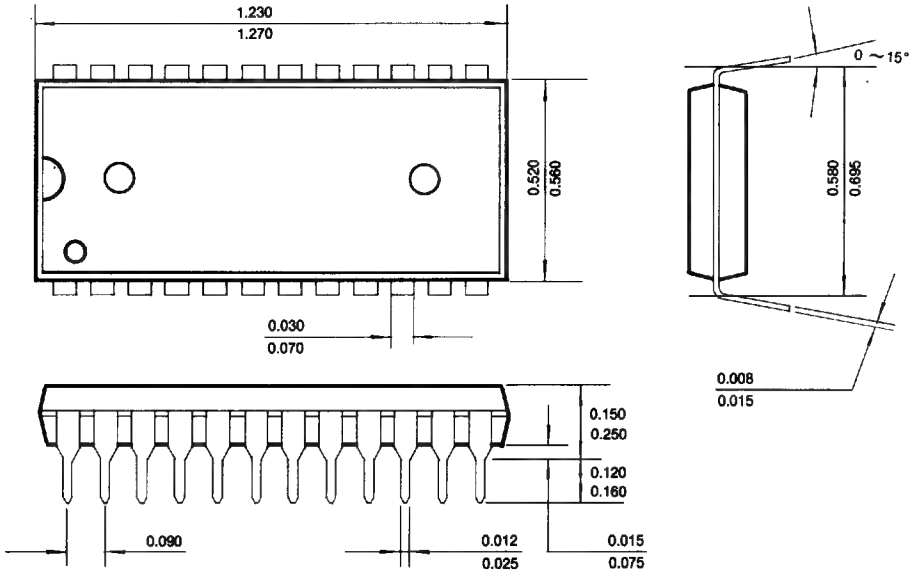


*includes jig capacitance.
All diodes 1N3064 or equivalent.

PACKAGE DIMENSIONS (Continued)

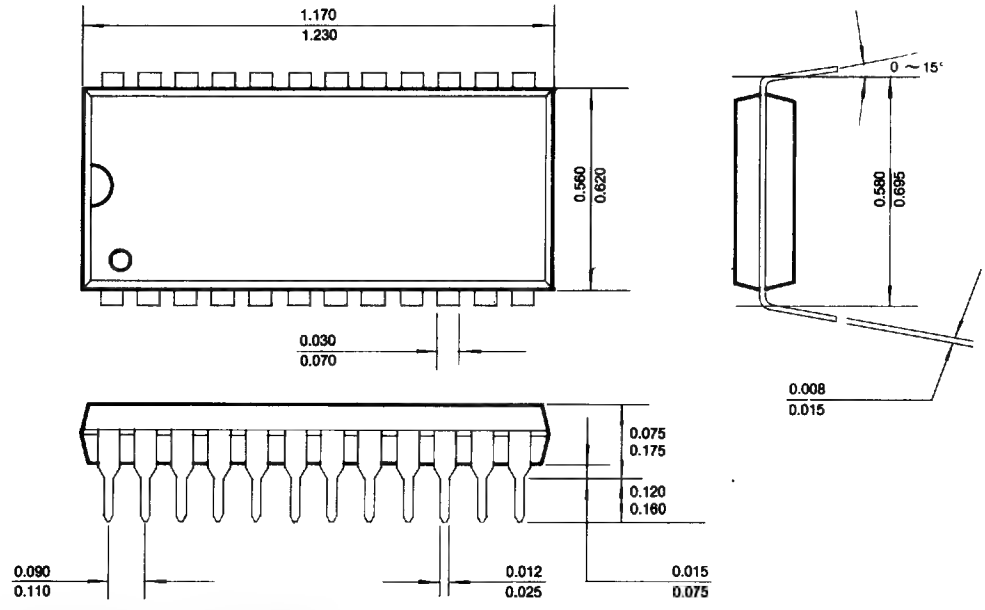
24 LEAD PLASTIC DUAL IN LINE PACKAGE

Unit: Inches



24 LEAD CERAMIC DUAL IN LINE PACKAGE

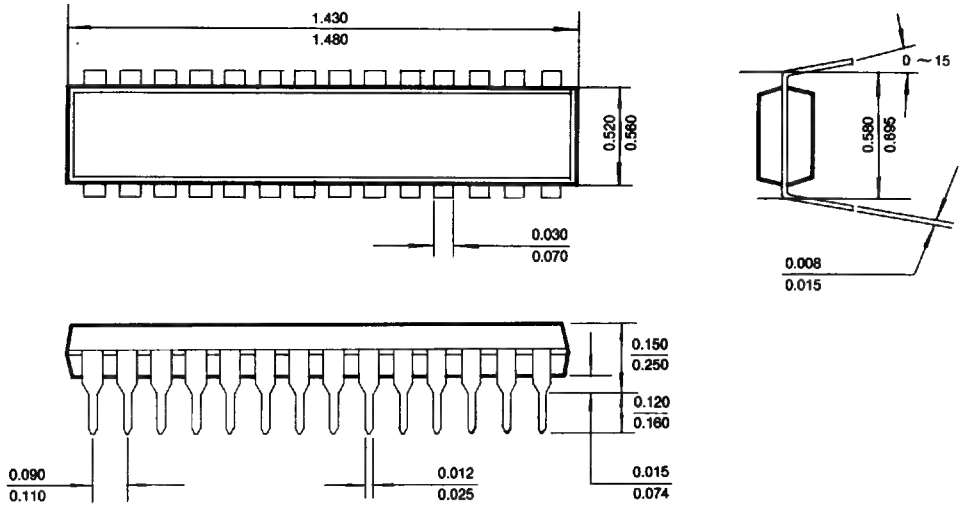
Unit: Inches



PACKAGE DIMENSIONS

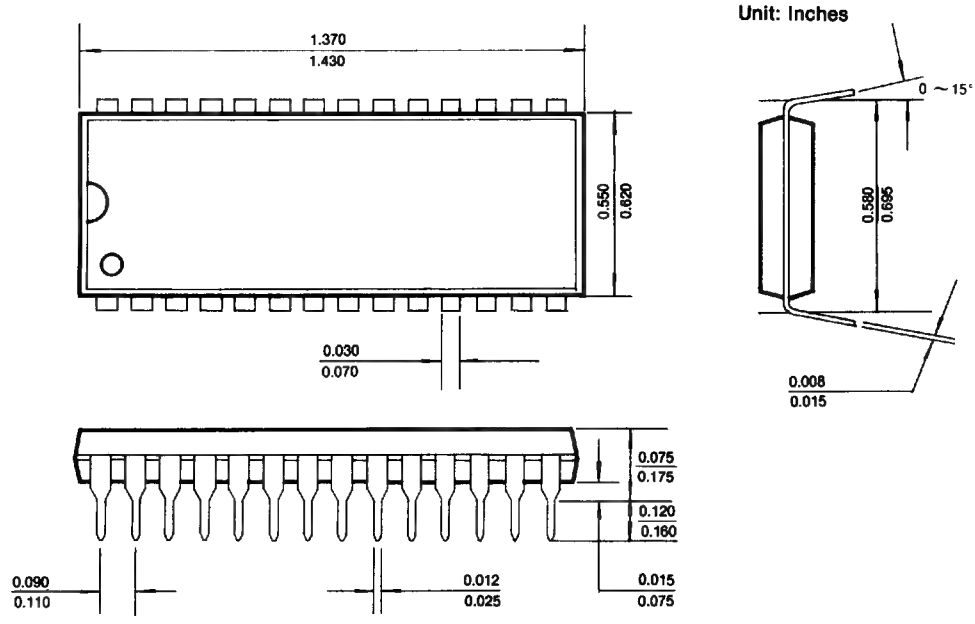
28 LEAD PLASTIC DUAL IN LINE PACKAGE

Unit: Inches



28 LEAD CERAMIC DUAL IN LINE PACKAGE

Unit: Inches



16K x 8 Bit Mask ROM

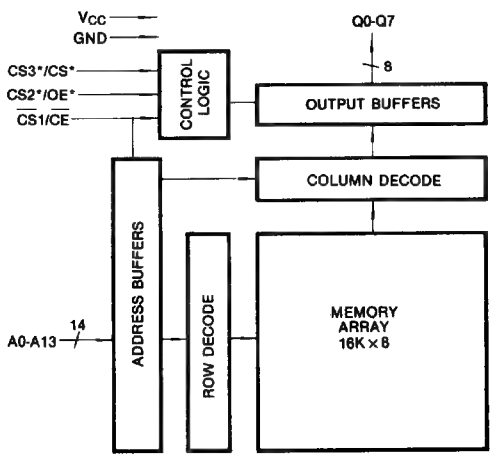
FEATURES

- **23128: Non-power down**
- **23128S: Automatic power down**
- **Fully static operation**
- **Silicon gate NMOS technology**
- **Maximum access time**
  23128/23128S-15: 150 ns
  23128/23128S-20: 200 ns
  23128/23128S-25: 250 ns
- **Fully TTL compatible**
- **5 volt only operation**
- **Byte-wide industry standard JEDEC pin-out**
- **Available in three temperature ranges**
  23128 (Commercial): 0°C to 70°C
  23128I (Industrial): −40°C to 85°C
  23128HR (Military): −55°C to 125°C

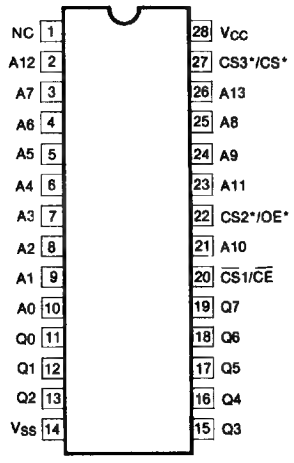
GENERAL DESCRIPTION

The KM23128 is a mask programmable read-only-memories with a 16K word by 8 bit organizations. Designed for ease of use, this device requires only a 5 volt supply, is TTL compatible, and because of its totally static (asynchronous) operation, requires no clock. This memory device is available in two versions. The KM23128 is non-power down version where the active level of chip selects CS2 and CS3 is programmable and is defined by the user to facilitate system memory expansion. The KM23128S offers an automatic power down feature (standby) controlled by the chip enable CE input. When CE goes high, the device automatically powers down and remains in a low power standby mode as long as CE remains high. Also, on the 23128S, the active level of chip select CS and output enable OE is programmable, thereby providing easier system implementation. The KM23128 is packaged in a 28 pin DIP with an industry standard bytewide JEDEC pin-out. Optionally, this device is available in a space saving 28 pin surface mounted plastic leaded chip carrier.

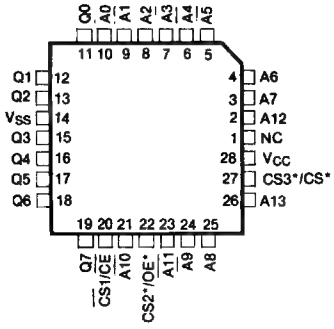
FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



*Programmable Active High or Low



Pin Name	Pin Function
A_0-A_{13}	Address Inputs
Q_0-Q_7	Data Outputs
$\overline{CS}1$, CS2 CS3, CS	Chip Selects
NC	No Connection
$\overline{CE}$	Chip Enable
OE	Output Enable
V_{CC}	5V ± 10% Power Supply
V_{SS}	Ground

Note: 23128 Only: Chip Selects $\overline{CS}1$, CS2 and CS3 are normally AND'd, ie, $(\overline{CS}1 \cdot CS2 \cdot CS3)$. At the option of the user, $\overline{CS}1$ and CS2 may be internally OR'd and then AND'd with CS3 ie, $[(\overline{CS}1 + CS2) \cdot CS3]$

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Voltage on Any Pin with Respect to Ground	V_{CC}	−0.5 to +7V	V
Storage Temperature	T_{stg}	−65 to +150	°C

Stresses above "absolute maximum ratings" may result in damage to the device. Functional operation of devices at the "absolute maximum ratings" or above the recommended operating conditions stipulated elsewhere in this specification is not implied.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	KM23128			KM23128I			KM23128HR			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Supply Voltage*	V_{CC}	4.5	5.0	5.5	4.5	5.0	5.5	4.5	5.0	5.5	Volts
Input High Level Voltage	V_{IH}	2.0		V_{CC}	2.0		V_{CC}	2.2		V_{CC}	Volts
Input Low Level Voltage	V_{IL}	−0.5		0.8	−0.5		0.8	−0.5		0.8	Volts
Operating Ambient Temperature	T_A	0		70	−40		85	−55		125	°C

*V_{CC} must be applied at least 100μs before proper device operation is achieved.

STATIC ELECTRICAL CHARACTERISTICS OVER RECOMMENDED OPERATING CONDITIONS (UNLESS OTHERWISE NOTED)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Input Leakage Current	I_{IN}	V_{IN} = 0V to V_{CC} max			10	μA
Output Leakage Current	I_O	V_O = 0.2 to V_{CC} max Chip Deselected			± 10	μA
Output High Voltage	V_{OH}	I_{OH} = −200μA	2.4			Volts
Output Low Voltage	V_{OL}	I_{OL} = 3.2mA			0.4	Volts
Supply Current-Active	I_{CC}	Outputs Open			75	mA
Supply Current-Standby	I_{SB}*	Chip Deselected			10	μA

*Applies to KM23128S Power Down Versions only.

5

CAPACITANCE (Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Input Capacitance	C_{IN}	All pins except pin under test are tied to ground			7.0	pF
Output Capacitance	C_O				12.5	pF

Notes: Characteristics are the same for all Operating Temperature Ranges.

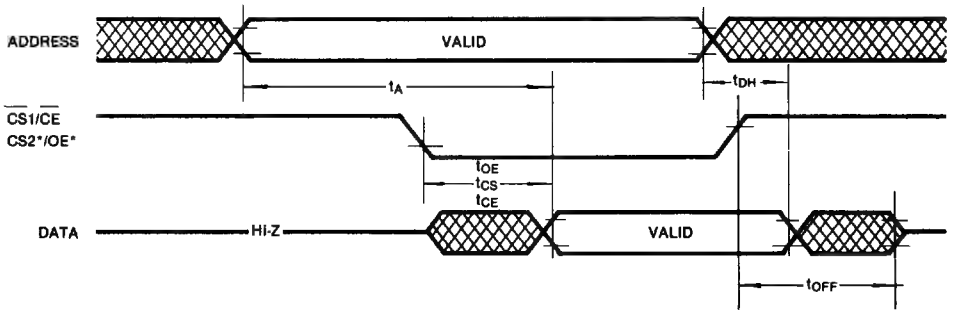
AC CHARACTERISTICS

AC CHARACTERISTICS OVER RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	23128-15 23128I-15		23128-20 23128I-20		23128-25, 23128I-25, 23128HR-25		Units
		Min	Max	Min	Max	Min	Max	
Address Access Time	t_A		150		200		250	ns
Chip Enable Access Time	t_{CE}		150		200		250	ns
Chip Select Access Time	t_{CS}		75		100		120	ns
Output Enable Access Time	t_{OE}		75		100		120	ns
Data Hold Time	t_{DH}	0		0		0		ns
CS Active to Data High Impedance	t_{OFF}		75		100		120	ns

TIMING DIAGRAMS

AC WAVEFORMS

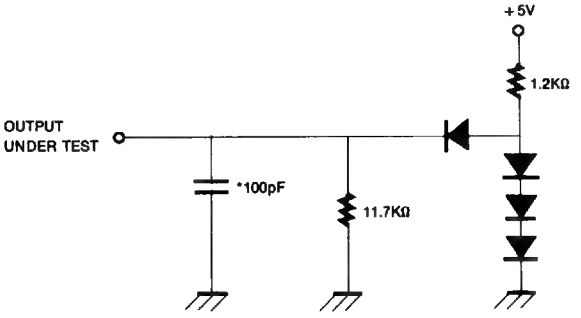


* Programmable chip selects CS, CS2 and CS3 and output Enable OE are assumed to be active low for this example

AC CONDITIONS OF TEST

Input Pulse Levels ..... 0.8 volts to 2.0 volts
Input Rise & Fall Times ..... 10 ns
Output Timing Levels ..... 0.8 volts to 2.0 volts

AC TEST LOAD CIRCUIT

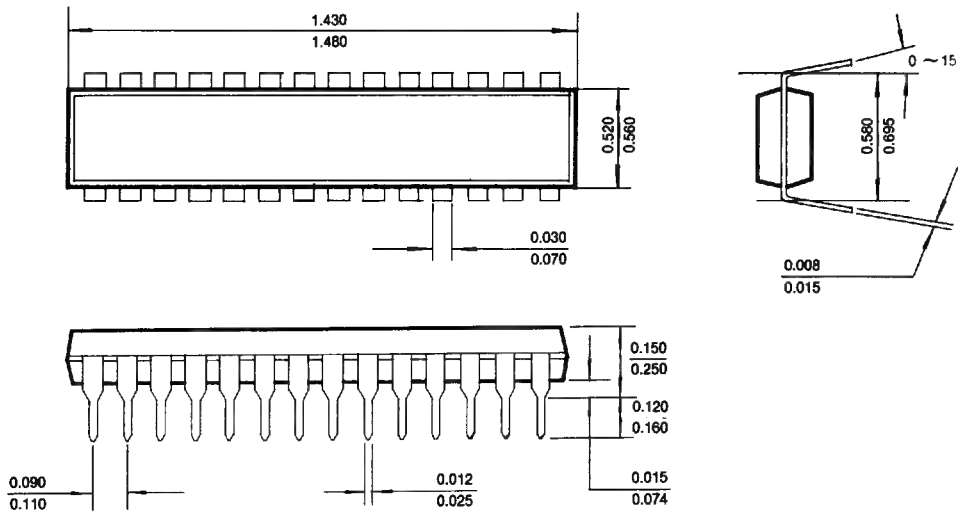


* Includes jig capacitance.
All diodes 1N3064 or equivalent.

PACKAGE DIMENSIONS

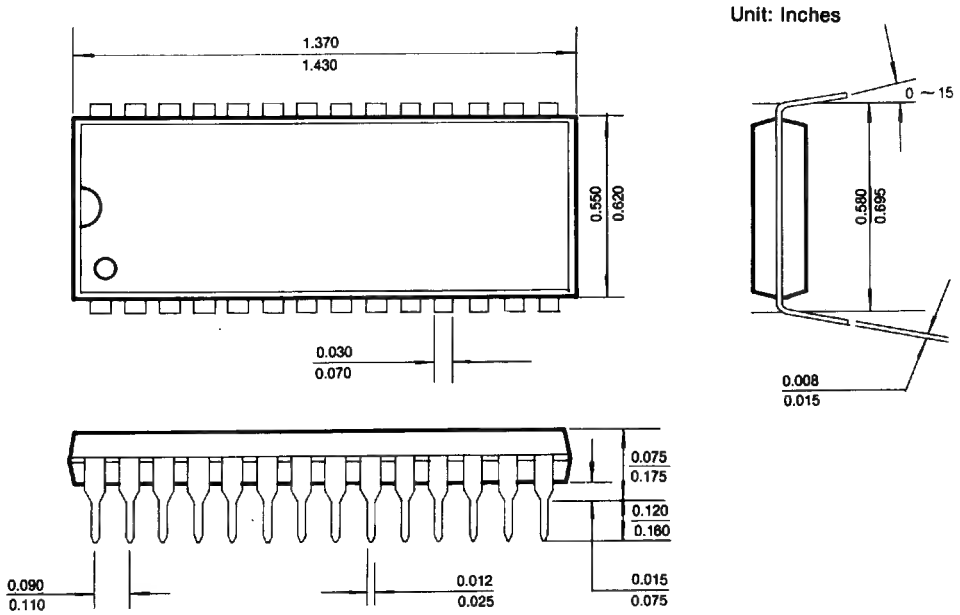
28 LEAD PLASTIC DUAL IN LINE PACKAGE

Unit: Inches



28 LEAD CERAMIC DUAL IN LINE PACKAGE

Unit: Inches



32K x 8 Bit Mask ROM

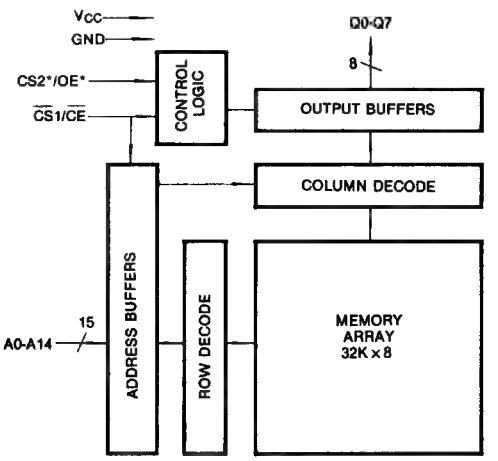
FEATURES

- **23256/57: Non-power down**
- **23256S/57S: Automatic power down**
- **Fully static operation**
- **Silicon gate NMOS technology**
- **Maximum access time**
  23256/57-15: 150 ns
  23256/57-20: 200 ns
  23256/57-25: 250 ns
- **Pin compatible with 27256 EPROMS**
- **Fully TTL compatible**
- **5 volt only operation**
- **Byte-wide industry standard JEDEC pin-out**
- **Available in three temperature ranges**
  23256/57 (Commercial): 0°C to 70°C
  23256I/57I (Industrial): −40°C to 85°C
  23256HR/57HR (Military): −55°C to 125°C

GENERAL DESCRIPTION

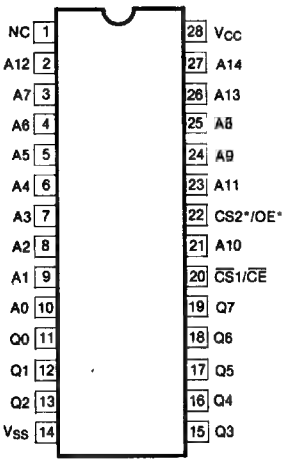
The KM23256/57 are mask programmable read only memories with 32K word by 8 bit organizations. Designed for ease of use, these devices require only a 5-volt supply, are TTL compatible, and because of their totally static (asynchronous) operation require no clock. These memory devices are available in two versions. The KM23256/57 are non-power down versions where the active level of chip select CS2 is programmable and is defined by the user to facilitate system memory expansion. The KM23256S and KM23257S are standby versions offering an automatic power-down feature controlled by the chip enable CE input. When CE goes high, the device automatically powers down and remains in a low power standby mode as long as CE remains high. Also, on the KM23256S and 23257S, the active level of output enable OE is programmable, thereby providing easier system implementation. The KM23256 is packaged in a 28 pin DIP with an industry standard byte-wide JEDEC pin-out. The 23257 is packaged in a 28 pin DIP with an alternate pin-out where pin 1 = A14 and pin 27 = NC. Optionally these devices are available in a space saving 28 pin surface mounted plastic leaded chip carrier.

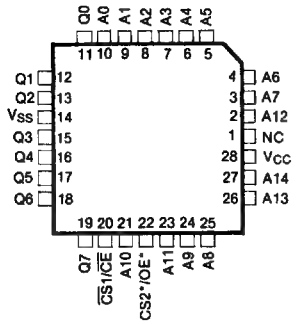
FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION

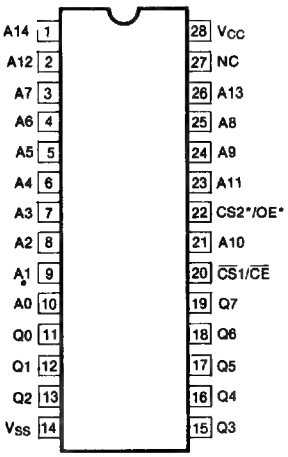
KM23256/S

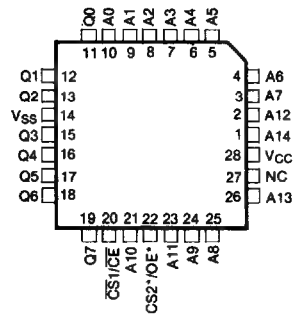




Note: 23256/57 only. Chip selects $\overline{CS}1$ and CS2 are normally AND'd, but may be internally OR'd at the option of the user

KM23257/S





*Programmable Active High, Low or Don't Care

Pin Name	Pin Function
A_0-A_{14}	Address Inputs
Q_0-Q_7	Data Outputs
$\overline{CS}1$, CS2	Chip Select
NC	No Connection
OE	Output Enable
$\overline{CE}$	Chip Enable
V_{CC}	5V ± 10% Power Supply

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Voltage on Any Pin with Respect to Ground	V_{CC}	−0.5 to +7V	V
Storage Temperature	T_{stg}	−65 to +150	°C

Stresses above "absolute maximum ratings" may result in damage to the device. Functional operation of devices at the "absolute maximum ratings" or above the recommended operating conditions stipulated elsewhere in this specification is not implied.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	KM23256/57			KM23256I/57I			KM23256HR/57HR			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Supply Voltage*	V_{CC}	4.5	5.0	5.5	4.5	5.0	5.5	4.5	5.0	5.5	Volts
Input High Level Voltage	V_{IH}	2.0		V_{CC}	2.0		V_{CC}	2.2		V_{CC}	Volts
Input Low Level Voltage	V_{IL}	−0.5		0.8	−0.5		0.8	−0.5		0.8	Volts
Operating Ambient Temperature	T_A	0		70	−40		85	−55		125	°C

*V_{CC} must be applied at least 100μs before proper device operation is achieved.

STATIC ELECTRICAL CHARACTERISTICS OVER RECOMMENDED OPERATING CONDITIONS (UNLESS OTHERWISE NOTED)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Input Leakage Current	I_{IN}	V_{IN} = 0V to V_{CC} max			10	μA
Output Leakage Current	I_O	V_O = 0.2 to V_{CC} max Chip Deselected			±10	μA
Output High Voltage	V_{OH}	I_{OH} = −200μA	2.4			Volts
Output Low Voltage	V_{OL}	I_{OL} = 3.2mA			0.4	Volts
Supply Current-Active	I_{CC}	Outputs Open			75	mA
Supply Current-Standby	I_{SB}*	Chip Deselected			10	μA

*Applies to 23256S/57S Power Down Versions only.

CAPACITANCE' (Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Input Capacitance	C_{IN}	All pins except pin under test are tied to ground			7.0	pF
Output Capacitance	C_O				12.5	pF

Notes: 1. Characteristics are the same for all Operating Temperature Ranges.

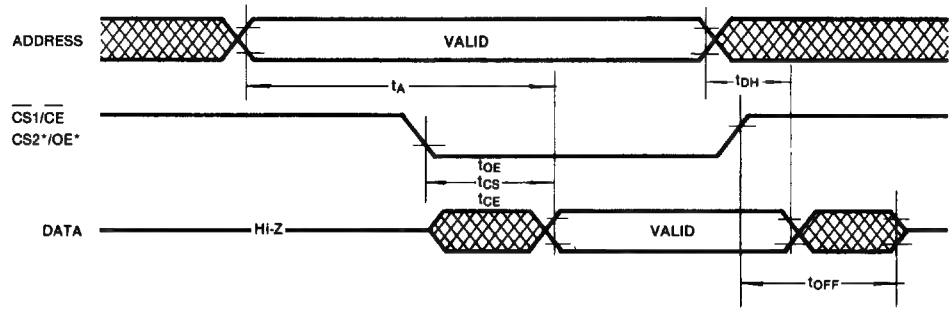
AC CHARACTERISTICS OVER RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	23256/57-15 23256I/57I-15		23256/57-20 23256I/57I-20		23256/57-25 23256I/57I-25		23256HR-27 23257HR-27		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Address Access Time	t_A		150		200		250		275	ns
Chip Enable Access Time	t_{CE}		150		200		250		275	ns
Chip Select Access Time	t_{CS}		80		100		120		135	ns
Output Enable Access Time	t_{OE}		80		100		120		135	ns
Data Hold Time	t_{DH}	0		0		0		0		ns
CS Active to Data High Impedance	t_{OFF}		80		100		120		135	ns

5

TIMING DIAGRAMS

AC WAVEFORMS

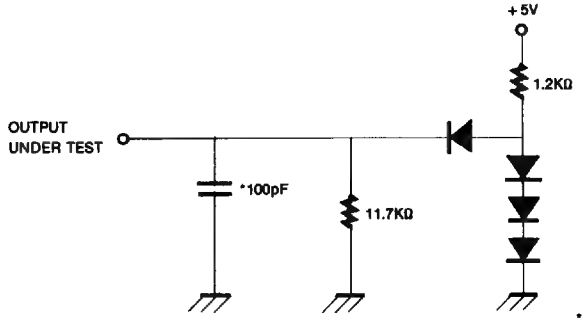


* Programmable chip select CS2 and output enable OE are assumed to be active low for this example

AC CONDITIONS OF TEST

Input Pulse Levels ..... 0.8 volts to 2.0 volts
Input Rise & Fall Times ..... 10 ns
Output Timing Levels ..... 0.8 volts to 2.0 volts

AC TEST LOAD CIRCUIT

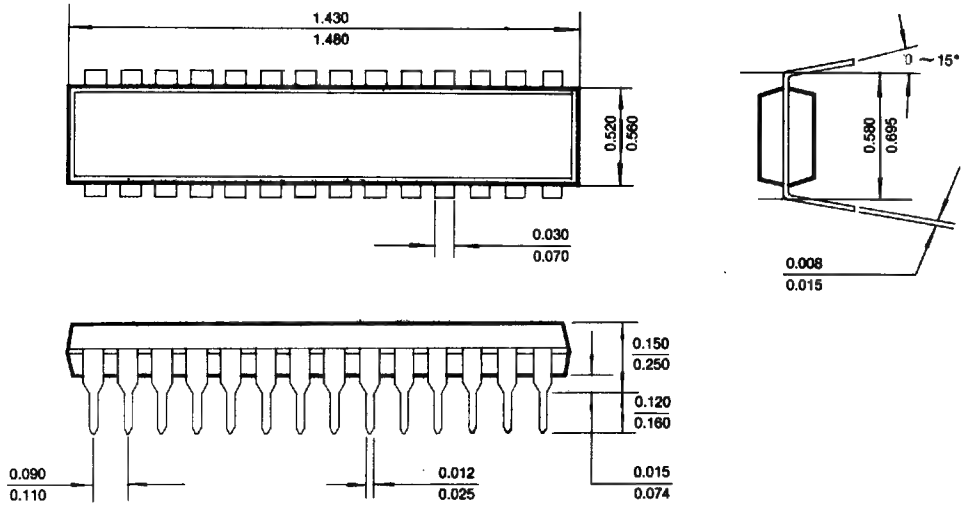


* includes jig capacitance.
All diodes 1N3064 or equivalent.

PACKAGE DIMENSIONS

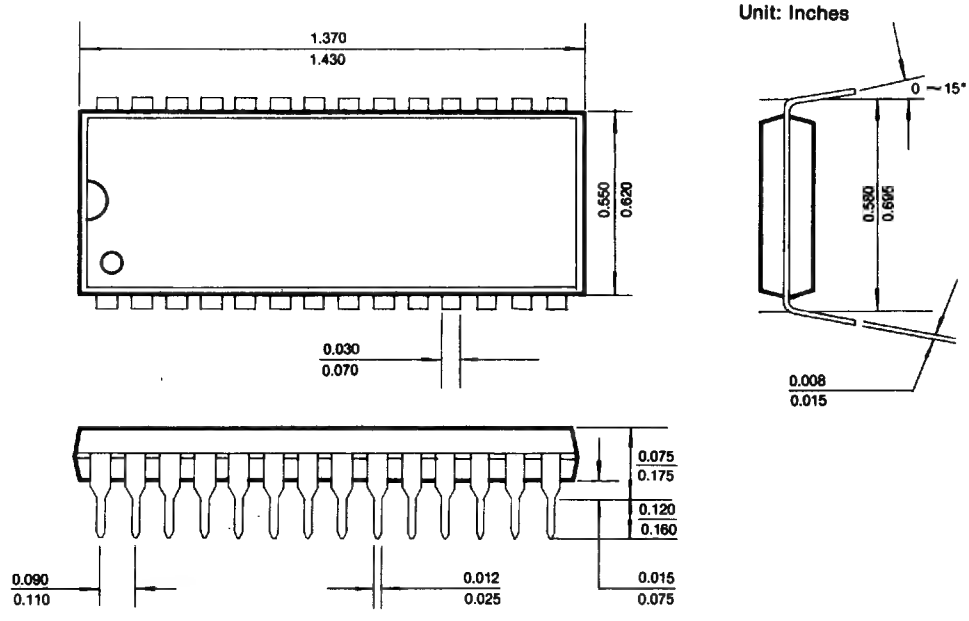
28 LEAD PLASTIC DUAL IN LINE PACKAGE

Unit: Inches



28 LEAD CERAMIC DUAL IN LINE PACKAGE

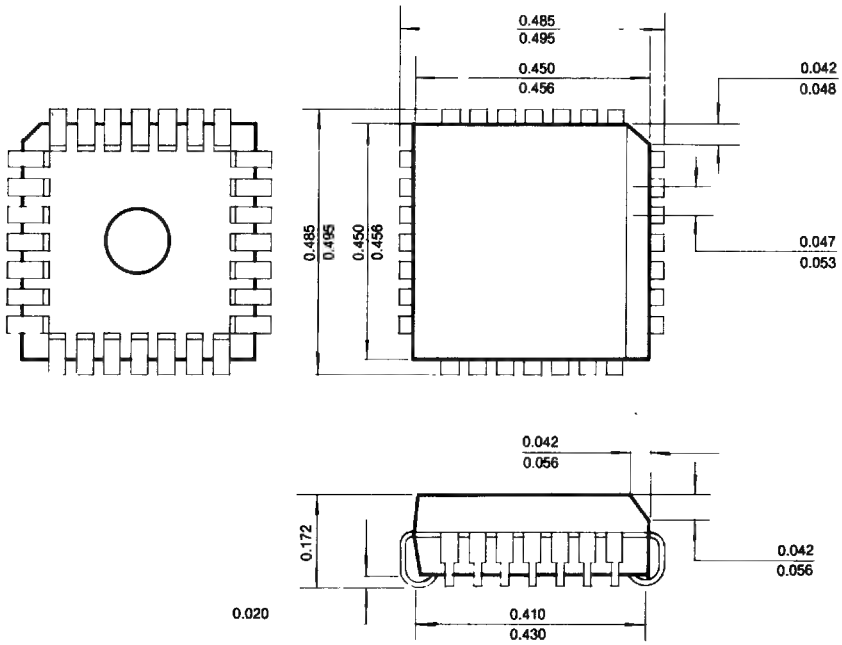
Unit: Inches



PACKAGE DIMENSIONS (Continued)

28 PIN PLASTIC LEADED CHIP CARRIER

Unit: Inches



64K x 8 Bit Mask ROM

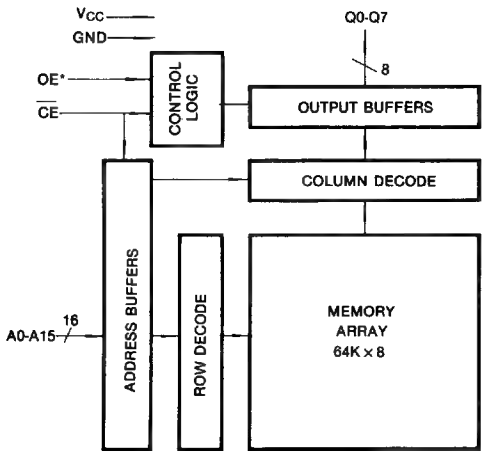
FEATURES

- **Fully static operation**
- **Silicon gate CMOS technology**
- **Maximum access time**
  23C512-15: 150 ns
  23C512-20: 200 ns
  23C512-25: 250 ns
- **Fully TTL compatible**
- **5 volt only operation**
- **Byte-wide industry standard JEDEC pin-out**
- **Available in two temperature ranges**
  23C512 (Commercial): 0°C to 70°C
  23C512I (Industrial): −40°C to 85°C

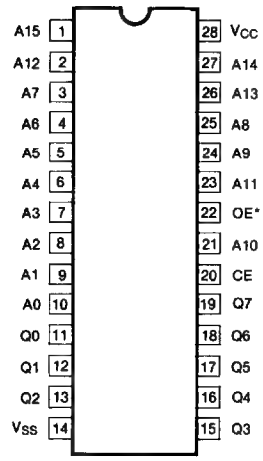
GENERAL DESCRIPTION

The KM23C512 is a mask programmable read-only-memories with a 64K word by 8 bit organizations. Designed for ease of use, this device requires only a 5 volt power supply, is TTL compatible, and because of its totally static (asynchronous) operation, requires no clock. This CMOS ROM offers very low power dissipation in the operational mode and has an automatic power down feature that significantly reduces power consumption in the standby mode. The active level of output enable OE is programmable, thereby providing easier system implementation. The KM23C512 is packaged in a 28 pin DIP with an industry standard byte-wide JEDEC pin-out. Optionally, this device is available in a space saving 32 pin surface mounted plastic leaded chip carrier.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



*Programmable output Enable
High, Low or Don't Care

Pin Name	Pin Function
A_0-A_{15}	Address Inputs
Q_0-Q_7	Data Outputs
OE	Output Enable
$\overline{CE}$	Chip Enable
V_{CC}	5V ± 10% Supply Voltage
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Voltage on Any Pin with Respect to Ground	V_{CC}	−0.5 to +7V	V
Storage Temperature	T_{stg}	−65 to +150	°C

Stresses above "absolute maximum ratings" may result in damage to the device. Functional operation of devices at the "absolute maximum ratings" or above the recommended operating conditions stipulated elsewhere in this specification is not implied.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	23C512			23C512I			Units
		Min	Typ	Max	Min	Typ	Max	
Supply Voltage*	V_{CC}	4.5	5.0	5.5	4.5	5.0	5.5	Volts
Input High Level Voltage	V_{IH}	2.0		V_{CC}	2.0		V_{CC}	Volts
Input Low Level Voltage	V_{IL}	−0.3		0.8	−0.3		0.8	Volts
Operating Ambient Temperature	T_A	0		70	−40		85	°C

*V_{CC} must be applied at least 100μs before proper device operation is achieved.

STATIC ELECTRICAL CHARACTERISTICS OVER RECOMMENDED OPERATING CONDITIONS (UNLESS OTHERWISE NOTED)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Input Leakage Current	I_{IN}	V_{IN} = 0V to V_{CC} max			10	μA
Output Leakage Current	I_O	V_O = 0.2 to V_{CC} max Chip Deselected			±10	μA
Output High Voltage	V_{OH}	I_{OH} = −200μA	2.4			Volts
Output Low Voltage	V_{OL}	I_{OL} = 3.2mA			0.4	Volts
Supply Current-Active	$I_{CC}2$	Outputs Open			40	mA
Supply Current-Standby	$I_{SB}3$	Chip Deselected			40	μA

CAPACITANCE[1] (Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Input Capacitance	C_{IN}	All pins except pin under test			10.0	pF
Output Capacitance	C_O	are tied to ground			12.5	pF

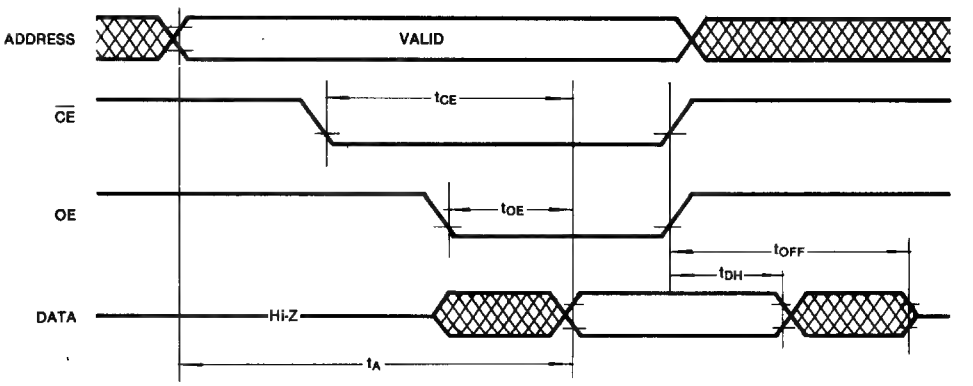
Notes: 1. Characteristics are the same for both Commercial and Industrial Operating Temperature Ranges.
2. Current is proportional to cycle rate. I_{CC} is measured at the specified minimum cycle time. Data outputs open.
$V_{IL} = V_{SS}$, $V_{IH} = V_{CC}$
3. $CE \geq V_{CC} - 0.3V$ or $CE \leq V_{SS} + 0.3V$

AC CHARACTERISTICS OVER RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	23C512-15		23C512-20		23C512-25		Units
		Min	Max	Min	Max	Min	Max	
Address Access Time	t_A		150		200		250	ns
Chip Enable Access Time	t_{CE}		150		200		250	ns
Output Enable Access Time	t_{OE}		75		100		125	ns
Data Hold Time	t_{DH}	0		0		0		ns
CS Active to Data High Impedance	t_{OFF}		80		80		80	ns

TIMING DIAGRAMS

AC WAVEFORMS

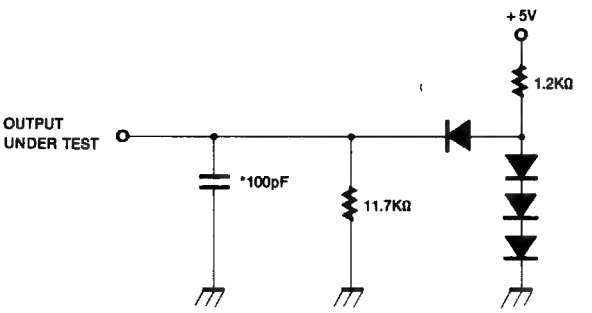


* Programmable output enable is assumed to be active low.

AC CONDITIONS OF TEST

Input Pulse Levels ..... 0.8 volts to 2.0 volts
Input Rise & Fall Times ..... 10 ns
Output Timing Levels ..... 0.8 volts to 2.0 volts

AC TEST LOAD CIRCUIT

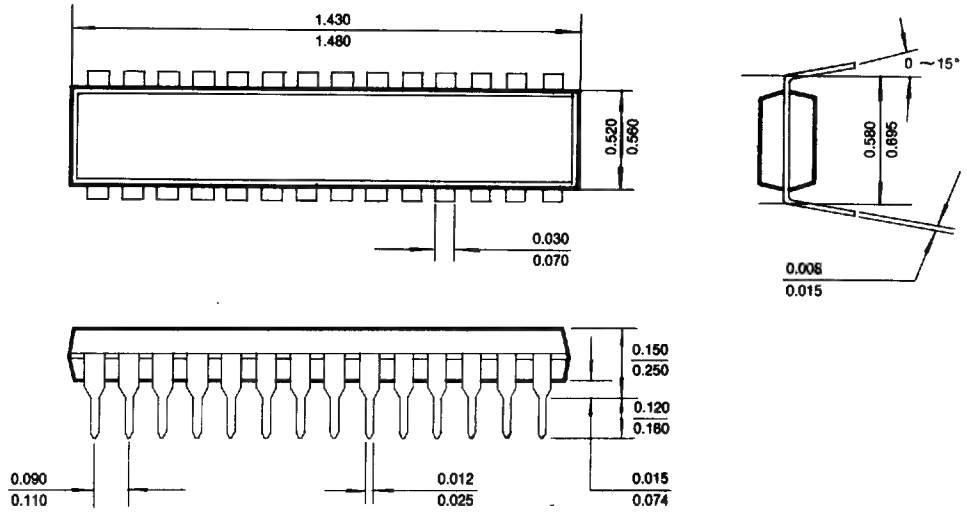


* Includes jig capacitance.
All diodes 1N3064 or equivalent.

PACKAGE DIMENSIONS

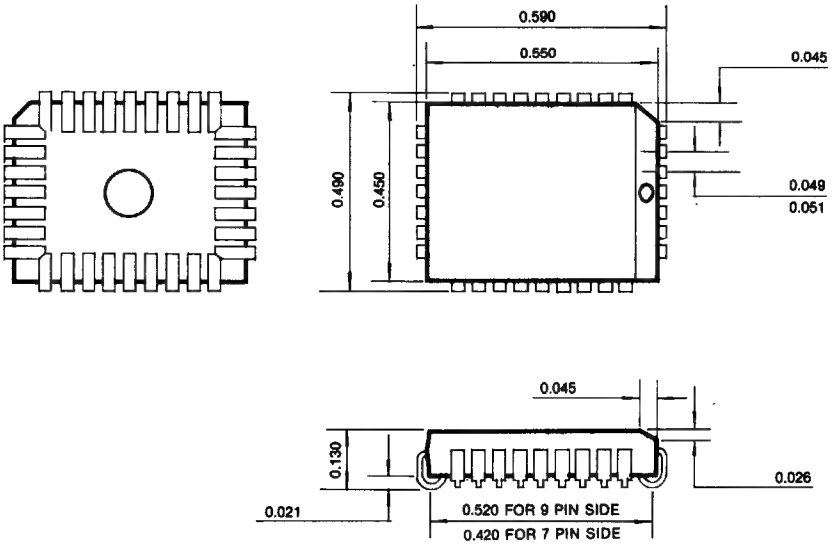
28 LEAD PLASTIC DUAL IN LINE PACKAGE

Unit: Inches



32 PIN PLASTIC LEADED CHIP CARRIER

Unit: Inches



*All dimensions are in inches with ±0.005 tolerance.

128K x 8 Bit Mask ROM

FEATURES

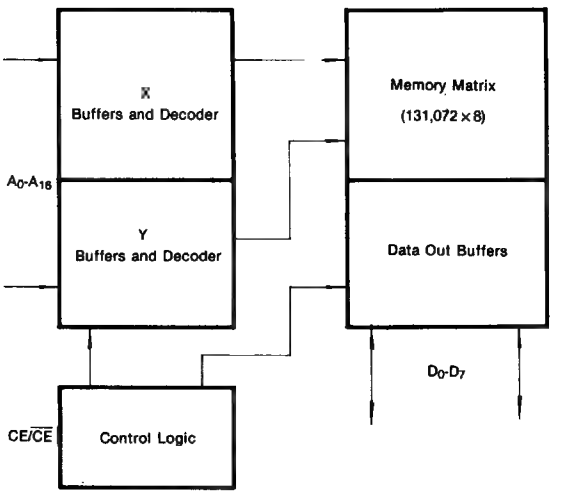
- **131,072 x 8 bit organization**
- **Fully static operation**
- **Fast access time: 150ns (max.)**
- **All inputs and outputs TTL compatible**
- **Programmable chip select**
- **28 Pin DIP (JEDEC standard)**

GENERAL DESCRIPTION

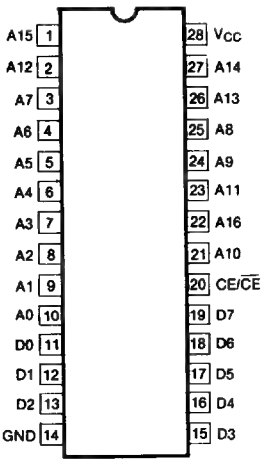
The KM23C1000 is fully static mask programmable ROM organized as 131,072 x 8 bit by using silicon-gate CMOS process technology.

The KM23C1000 provides polarity programmable CE buffer as user option mode.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Pin Name	Pin Function
A_0-A_{16}	Address Inputs
D_0-D_7	Data Outputs
CE/$\overline{CE}$	Chip Enable
V_{CC}	+5V
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Voltage On Any Pin Relative to V_{SS}	V_{IN}	−0.3 to +7.0	V
Temperature Under Bias	T_{bias}	−10 to +85	°C
Storage Temperature	T_{stg}	−55 to +150	°C

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, Ta = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Units
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V
Input High Voltage, all Inputs	V_{IH}	2.2	—	V_{CC} + 0.3	V
Input Low Voltage, all inputs	V_{IL}	−0.3	—	0.8	V

DC AND OPERATING CHARACTERISTICS
(Recommended operating conditions otherwise noted.)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Operating Current	I_{CC}	$\overline{CE}$ = V_{IL} f = 6.7MHz	—	30	mA
		f = 4.0MHz	—	25	mA
Standby Current (TTL)	I_{SB1}	$\overline{CE}$ = V_{IH}, all I/O's = open	—	1	mA
Standby Current (CMOS)	I_{SB2}	$\overline{CE}$ = V_{CC}, all I/O's = open	—	100	μA
Input Leakage Current	IL_I	V_{IN} = 0 to V_{CC}	—	10	μA
Output Leakage Current	IL_O	V_{OUT} = 0 to V_{CC}	—	10	μA
Output High Voltage Level	V_{OH}	I_{OH} = −1.0mA	2.4	V_{CC} − 0.3	V
Output Low Voltage Level	V_{OL}	I_{OL} = 3.2mA	—	0.4	V

CAPACITANCE (Ta = 25°C, f = 1.0MHz)

Parameter	Symbol	Test Condition	Min	Max	Unit
Output Capacitance	C_{OUT}	V_{OUT} = 0V	—	8.0	pF
Input Capacitance	C_{IN}	V_{IN} = 0V	—	10.0	pF

Notes: Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

$\overline{CE}$/CE	Mode	I/O	Power
L/H	Standby	High-z	Standby
H/L	Operating	High-z	Active
	Operating	D_{OUT}	Active

AC CHARACTERISTICS

(Ta = 0° to +70°C, V_{CC} = 5V ± 10%, unless otherwise noted)

TEST CONDITIONS

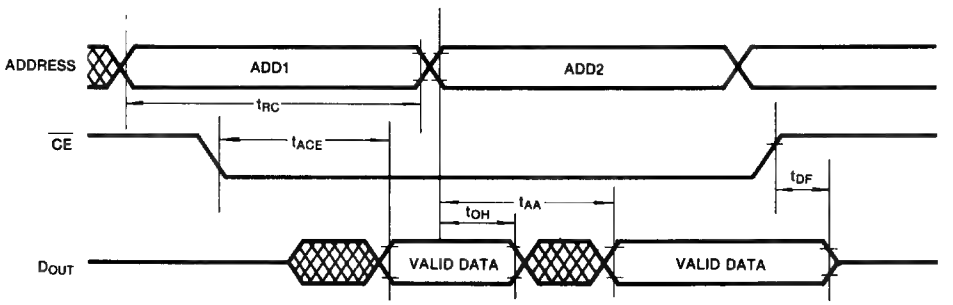
Parameter	Value
Input Pulse Levels	0.6V to 2.4V
Input Rise and Fall Times	10ns
Input and Output Timing Levels	0.8V and 2.0V
Output Load	1 TTL GATE and C_L = 100pF

READ CYCLE

Parameter	Symbol	23C1000-15		23C1000-20		23C1000-25		Units
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	150		200		250		ns
Chip Enable Access Time	t_{ACE}		150		200		250	ns
Address Access Time	t_{AA}		150		200		250	ns
Chip Disable to Output High-Z	t_{DF}		60		70		80	ns
Output Hold from Address Change	t_{OH}	10		10		10		ns

TIMING DIAGRAM

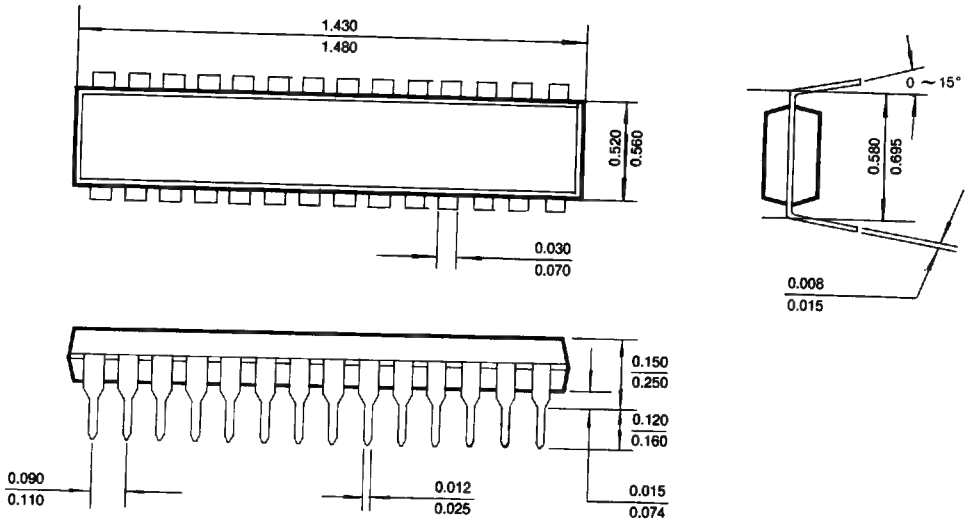
READ



PACKAGE DIMENSIONS

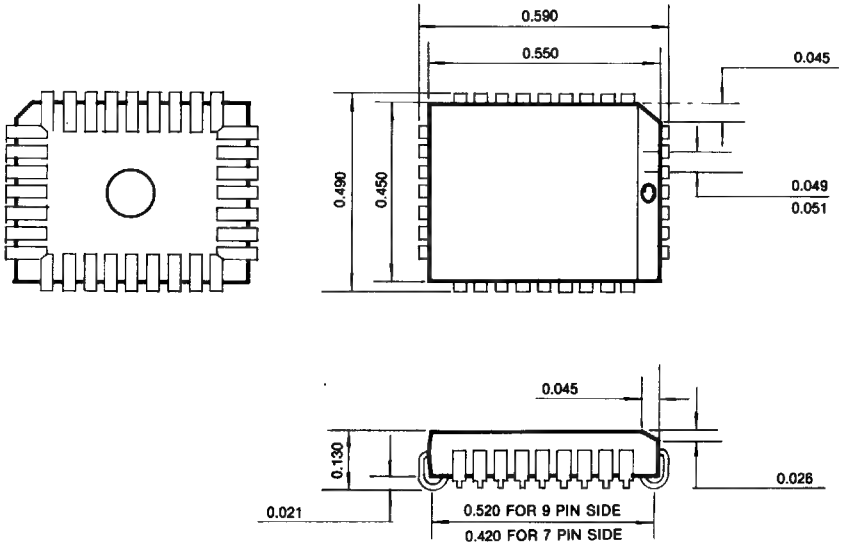
28 LEAD PLASTIC DUAL IN LINE PACKAGE

Unit: Inches



32 PIN PLASTIC LEADED CHIP CARRIER

Unit: Inches



*All dimensions are in inches with ±0.005 tolerance.

256K x 8 Bit Mask ROM

FEATURES

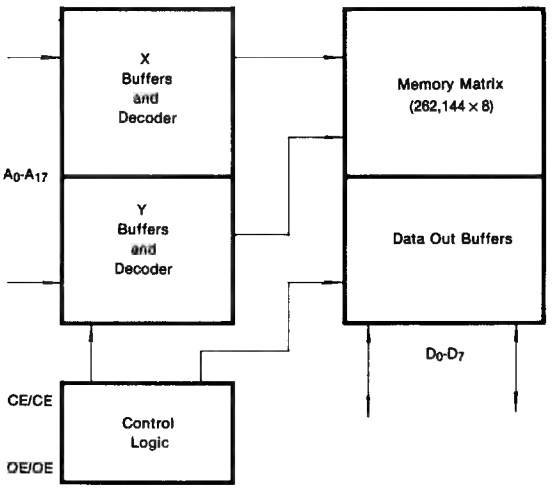
- **262,144 x 8 bit organization**
- **Fully static operation**
- **Fast access time: 150ns (max.)**
- **All inputs and outputs TTL compatible**
- **Programmable chip select**
- **32 Pin DIP (JEDEC standard)**

GENERAL DESCRIPTION

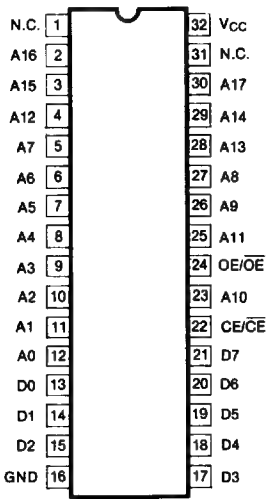
The KM23C2000 is fully static mask programmable ROM organized as 262,144 x 8 bit by using silicon-gate CMOS process technology.

The KM23C2000 provides polarity programmable CE and OE buffer as user option mode.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Pin Name	Pin Function
A_0-A_{17}	Address Inputs
D_0-D_7	Data Outputs
CE/$\overline{CE}$	Chip Enable
OE/$\overline{OE}$	Output Enable
V_{CC}	+5V
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Voltage On Any Pin Relative to V_{SS}	V_{IN}	−0.3 to +7.0	V
Temperature Under Bias	T_{bias}	−10 to +85	°C
Storage Temperature	T_{stg}	−55 to +150	°C

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, Ta = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Units
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V
Input High Voltage, all Inputs	V_{IH}	2.2	—	$V_{CC}+0.3$	V
Input Low Voltage, all inputs	V_{IL}	−0.3	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions otherwise noted.)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Operating Current	I_{CC}	$\overline{CE}=\overline{OE}=V_{IL}$ f = 6.7MHz	—	40	mA
		f = 4.0MHz	—	30	mA
Standby Current (TTL)	I_{SB1}	$\overline{CE}=V_{IH}$, all I/O's = open	—	1	mA
Standby Current (CMOS)	I_{SB2}	$\overline{CE}=V_{CC}$, all I/O's = open	—	100	μA
Input Leakage Current	IL_I	$V_{IN}=0$ to V_{CC}	—	10	μA
Output Leakage Current	IL_O	$V_{OUT}=0$ to V_{CC}	—	10	μA
Output High Voltage Level	V_{OH}	$I_{OH}=-1.0$mA	2.4	$V_{CC}-0.3$	V
Output Low Voltage Level	V_{OL}	$I_{OL}=3.2$mA	—	0.4	V

CAPACITANCE (Ta = 25°C, f = 1.0MHz)

Parameter	Symbol	Test Condition	Min	Max	Unit
Output Capacitance	C_{OUT}	$V_{OUT}=0$V	—	8.0	pF
Input Capacitance	C_{IN}	$V_{IN}=0$V	—	10.0	pF

Notes: Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

CE/$\overline{CE}$	OE/$\overline{OE}$	Mode	I/O	Power
L/H	X	Standby	High-z	Standby
H/L	L/H	Operating	High-z	Active
	H/L	Operating	D_{OUT}	Active

AC CHARACTERISTICS

(Ta = 0° to +70°C, V_{CC} = 5V ± 10%, unless otherwise noted)

TEST CONDITIONS

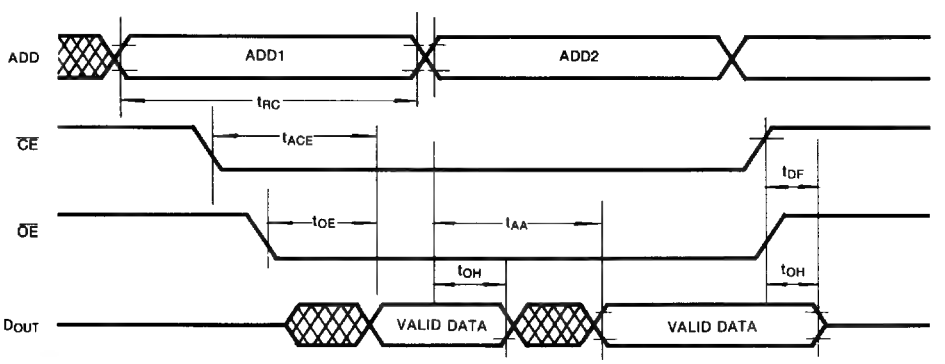
Parameter	Value
Input Pulse Levels	0.6V to 2.4V
Input Rise and Fall Times	10ns
Input and Output Timing Levels	0.8V and 2.0V
Output Load	1 TTL GATE and C_L = 100pF

READ CYCLE

Parameter	Symbol	23C2000-15		23C2000-20		23C2000-25		Units
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	150		200		250		ns
Chip Enable Access Time	t_{ACE}		150		200		250	ns
Address Access Time	t_{AA}		150		200		250	ns
Output Enable Access Time	t_{OE}		70		90		110	ns
Output or Chip Disable to Output High-Z	t_{DF}		60		70		80	ns
Output Hold from Address Change	t_{OH}	10		10		10		ns

TIMING DIAGRAM

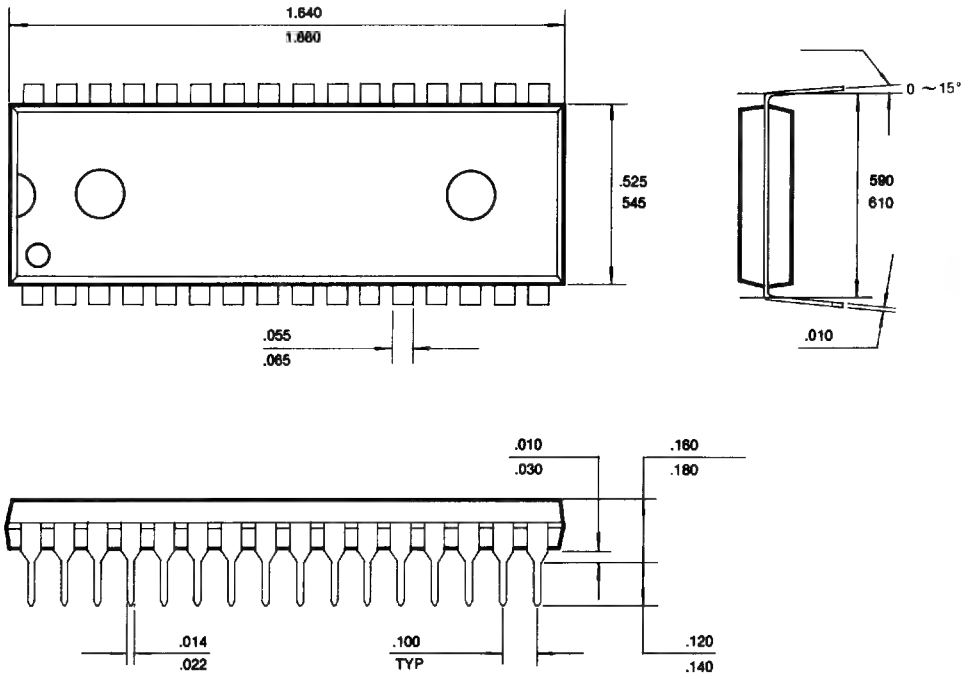
READ



PACKAGE DIMENSIONS

32 LEAD PLASTIC DUAL IN LINE PACKAGE

units: inches



512K x 8 Bit Mask ROM

FEATURES

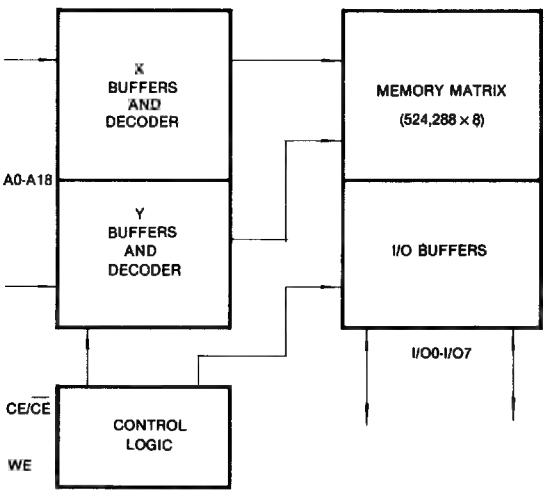
- **524,288 x 8 bit organization**
- **Fully static operation**
- **Fast access time: 150 ns (max.)**
- **All inputs and outputs TTL compatible**
- **Three state outputs**
- **Programmable chip select**
- **Programmable output enable**
- **32-Pin DIP (JEDEC standard)**

GENERAL DESCRIPTION

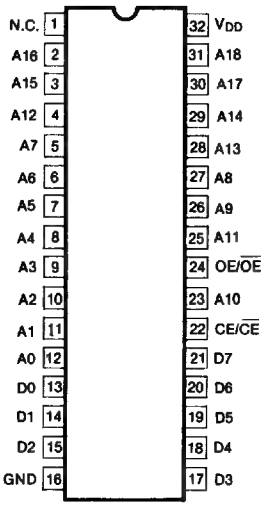
The KM23C4000 is a fully static mask programmable ROM organized as 524,288 x 8 bit by using silicon-gate CMOS process technology.

The KM23C4000 provides polarity programmable CE and OE buffer as user option mode.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Pin Name	Pin Function
A_0-A_{18}	Address Inputs
I/O_0-I/O_7	Data Outputs
CE/$\overline{CE}$	Chip Enable
OE/$\overline{OE}$	Output Enable
V_{CC}	+5V
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}	−0.3 to +7.0	V
Temperature Under Bias	T_{bias}	−10 to +85	°C
Storage Temperature	T_{stg}	−55 to +150	°C

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, Ta = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V
Input High Voltage, All Inputs	V_{IH}	2.2	—	V_{CC} + 0.3	V
Input Low Voltage, All Inputs	V_{IL}	−0.3	—	0.8	V

5

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions otherwise noted.)

Parameter	Symbol	Test Condition	Min	Max	Unit
Operating Current	I_{CC}	CE = OE = V_{IL} f = 6.7MHz f = 4MHz		60 40	mA mA
Standby Current (TTL)	I_{SB1}	CE = V_{IH}, all I/O's = open		1	mA
Standby Current (CMOS)	I_{SB2}	CE = V_{CC}, all I/O's = open		100	μA
Input Leakage Current	I_{LI}	V_{IN} = 0 to V_{CC}		10	μA
Output Leakage Current	I_{LO}	V_{OUT} = 0 to V_{CC}		10	μA
Output High Voltage Level	V_{OH}	I_{OH} = −1.0mA	2.4	V_{CC} + 0.3	V
Output Low Voltage Level	V_{OL}	I_{OL} = 2.0mA		0.4	V

CAPACITANCE (Ta = 25°C, f = 1.0 MHz)

Item	Symbol	Test Condition	Min	Max	Units
Output Capacitance	C_{OUT}	V_{OUT} = 0V		8.0	pF
Input Capacitance	C_{IN}	V_{IN} = 0V		10.0	pF

Note: Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

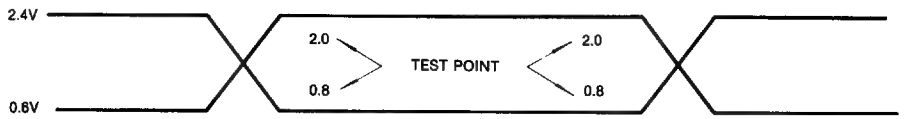
CE/$\overline{CE}$	OE/$\overline{OE}$	Mode	I/O	Power
L/H	X	Standby	High-Z	Standby
H/L	L/H	Operating	High-Z	Active
	H/L	Operating	D_{OUT}	Active

AC CHARACTERISTICS

(Ta = 0°C to +70°C, V_{CC} = 5V + 10%, unless otherwise noted.)

Parameter	Value
Input Pulse Levels	0.6V to 2.4V
Input Rise and Fall Times	10 ns
Input and Output Timing Levels	0.8V and 2.0V
Output Load	1 TTL GATE and C_L = 100 pF

TEST INPUT/OUTPUT WAVEFORM

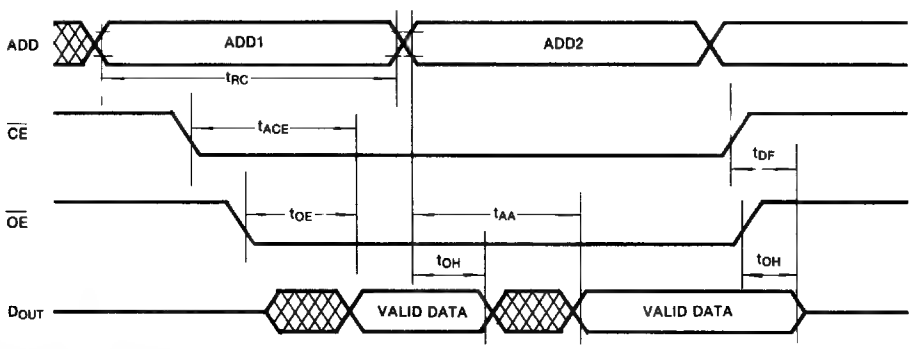


READ CYCLE

Parameter	Symbol	KM23C4000-15		KM23C4000-20		KM23C4000-25		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	150		200		250		ns
Chip Enable Access Time	t_{ACE}		150		200		250	ns
Address Access Time	t_{AA}		150		200		250	ns
Output Enable Access Time	t_{OE}		70		90		110	ns
Output or Chip Disable to Output High-Z	t_{DF}		60		70		80	ns
Output from Address Change	t_{OH}	10		10		10		ns

TIMING DIAGRAM

READ



256K EPROM:

When the customer releases his Mask ROM Data in the form of EPROMs, he should use sixteen 256K EPROM and program data of 16 address blocks of the KM23C4000 to each 256K EPROM. SAMSUNG requires 3 sets, total 48 pcs. of such programmed EPROMs. (Two sets, total 32 pcs. are acceptable.) In addition to the programmed sets. SAMSUNG requires an additional set of blank EPROMs (16 pcs) for supplying customer ROM Data Code Verification.

MSB **LSB**

A18	A17	A16	A15	A14	A13	A12	A11	A10	A09	A08	A07	A06	A05	A04	A03	A02	A01	A00
0	0	0	0	27C256 (NO. 1: 0K to 32K)														
0	0	0	1	27C256 (NO. 2: 32K to 64K)														
0	0	1	0	27C256 (NO. 3: 64K to 96K)														
0	0	1	1	27C256 (NO. 4: 96K to 128K)														
0	1	0	0	27C256 (NO. 5: 128K to 160K)														
0	1	0	1	27C256 (NO. 6: 160K to 192K)														
0	1	1	0	27C256 (NO. 7: 192K to 224K)														
0	1	1	1	27C256 (NO. 8: 224K to 256K)														
1	0	0	0	27C256 (NO. 9: 256K to 288K)														
1	0	0	1	27C256 (NO. 10: 288K to 320K)														
1	0	1	0	27C256 (NO. 11: 320K to 352K)														
1	0	1	1	27C256 (NO. 12: 352K to 384K)														
1	1	0	0	27C256 (NO. 13: 384K to 416K)														
1	1	0	1	27C256 (NO. 14: 416K to 448K)														
1	1	1	0	27C256 (NO. 15: 448K to 480K)														
1	1	1	1	27C256 (NO. 16: 480K to 512K)														

512K EPROM:

When the customer releases his Mask ROM Data in the form of EPROMs, he should use eight 512K EPROM and program data of 8 address blocks of the KM23C4000 to each 512K EPROM. SAMSUNG requires 3 sets, total 24 pcs. of such programmed EPROMs. (Two set, total 16 pcs. are acceptable.) In addition to the programmed sets. SAMSUNG requires an additional set of blank EPROMs (8 pcs) for supplying customer ROM Data Code Verification.

MSB **LSB**

A18	A17	A16	A15	A14	A13	A12	A11	A10	A09	A08	A07	A06	A05	A04	A03	A02	A01	A00
0	0	0		27C512 (NO. 1: 0K to 64K)														
0	0	1		27C512 (NO. 2: 64K to 128K)														
0	1	0		27C512 (NO. 3: 128K to 192K)														
0	1	1		27C512 (NO. 4: 192K to 256K)														
1	0	0		27C512 (NO. 5: 256K to 320K)														
1	0	1		27C512 (NO. 6: 320K to 384K)														
1	1	0		27C512 (NO. 7: 384K to 448K)														
1	1	1		27C512 (NO. 8: 448K to 512K)														

256K EPROM:

When the customer releases his Mask ROM Data in the form of EPROMs, he should use sixteen 256K EPROM and program data of 16 address blocks of the KM23C4000 to each 256K EPROM. SAMSUNG requires 3 sets, total 48 pcs. of such programmed EPROMs. (Two sets, total 32 pcs. are acceptable.) In addition to the programmed sets. SAMSUNG requires an additional set of blank EPROMs (16 pcs) for supplying customer ROM Data Code Verification.

MSB **LSB**

A18	A17	A16	A15	A14	A13	A12	A11	A10	A09	A08	A07	A06	A05	A04	A03	A02	A01	A00
0	0	0	0	27C256 (NO. 1: 0K to 32K)														
0	0	0	1	27C256 (NO. 2: 32K to 64K)														
0	0	1	0	27C256 (NO. 3: 64K to 96K)														
0	0	1	1	27C256 (NO. 4: 96K to 128K)														
0	1	0	0	27C256 (NO. 5: 128K to 160K)														
0	1	0	1	27C256 (NO. 6: 160K to 192K)														
0	1	1	0	27C256 (NO. 7: 192K to 224K)														
0	1	1	1	27C256 (NO. 8: 224K to 256K)														
1	0	0	0	27C256 (NO. 9: 256K to 288K)														
1	0	0	1	27C256 (NO. 10: 288K to 320K)														
1	0	1	0	27C256 (NO. 11: 320K to 352K)														
1	0	1	1	27C256 (NO. 12: 352K to 384K)														
1	1	0	0	27C256 (NO. 13: 384K to 416K)														
1	1	0	1	27C256 (NO. 14: 416K to 448K)														
1	1	1	0	27C256 (NO. 15: 448K to 480K)														
1	1	1	1	27C256 (NO. 16: 480K to 512K)														

MASK ROM Code Data Release by Magnetic Tapes:

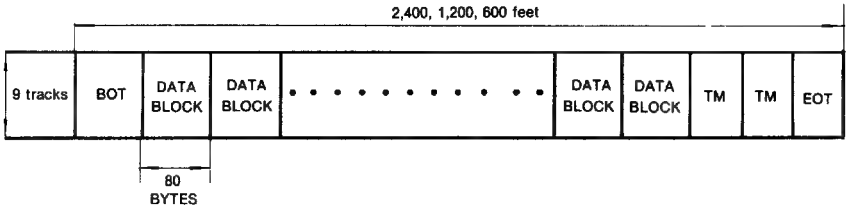
When the customer releases his MASK ROM Code Data in the form of Magnetic Tape (MT), he should use tapes formal like below.

- **Physical Requirements:**

1. Length : 2,400 feet, 1,200 feet, or 600 feet
2. Width : 1/2 inch or 1/4 inch
3. Tracks : 9 tracks
4. Density : 1,600 BPI or 6,250 BPI

- **MT Format:**

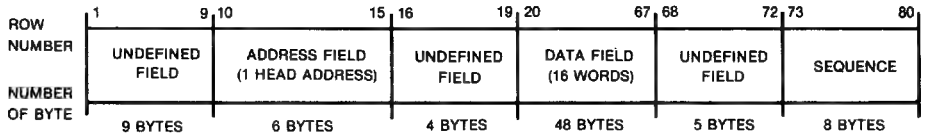
1. Label : No tape mark on the header of tape.
2. Record Size : Single record/record
3. Block Size : Single record/block
4. File : Single file volume
5. Code Used : ASCII code (EBCDIC code also acceptable)



Note: BOT : BEGINNING OF TAPE
EOT : END OF TAPE
TM : TAPE MARK

• **Data Block Format (TBD)**

ex1) Mistubishi Type



Udefined Field (Row 1-9/16-19/68-72): In this field, blanks(b) should be recorded.

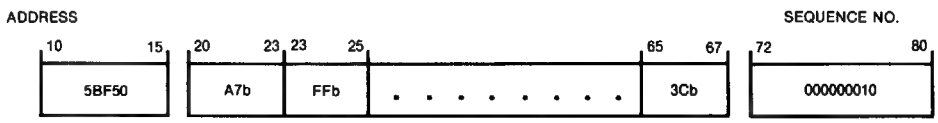
Address Field (Row 10-15): In the address field, the header of 16-word data that follows the address field should be recorded in the form of five digit hexadecimal number following a symbol "#". The corresponding binary address to this hex address in shown in the following example.

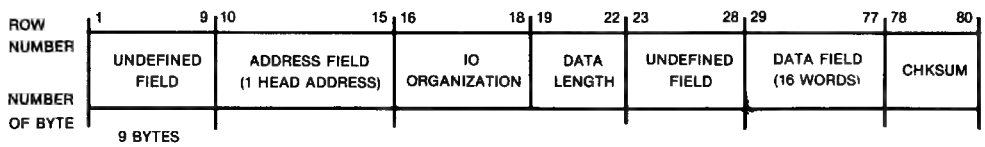
ADDRESS BIT	A18	A17	A16	A15	A14	A13	A12	A11	A10	A09	A08	A07	A06	A05	A04	A03	A02	A01	A00
BINARY ADD.	1	0	1	1	0	1	1	1	1	1	1	0	1	0	1	0	0		
HEX ADD.	5			B				F				5				0			
REC. FORM	5BF50																		

Data Field (Row 20-67): In this field, 16-word data with successive address should be recorded in the form of two digit Hexadecimal numbers followed by a blank (b). (The header data is for the address recorded in the address field.) The corresponding binary data to this hex data is shown in the following example.

DATA BIT	08	07	06	05	04	03	02	01
BINARY DATA								
HEX DATA	A				7			
RECORDED DATA	A7b							

Sequence Number Field (Row 73-80): In this field sequence number of each record (data block) should be recorded in the form of an eight digit decimal number, which must be counted up by tens, all digits to the left of the most significant digit should be zeros, not blanks. Refer to the following example.

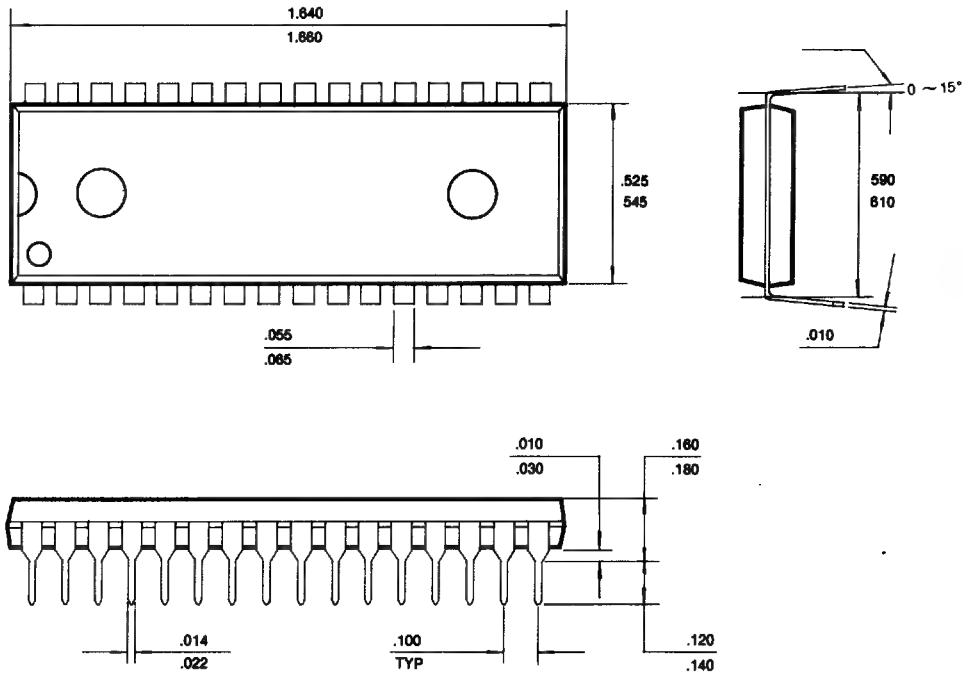




PACKAGE DIMENSIONS

32 LEAD PLASTIC DUAL IN LINE PACKAGE

units: inches



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PRINTED IN KOREA
JUNE, 1989